

IC-ARM-VPX3c

3U VPX LX2080A/LX2160A Arm®-based Single Board Computer

- 3U VPX
- NXP LX2080A/LX2160A Arm® processor
- VITA 65.0 SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16
- 10, 25, 40 and 100 GbE interfaces with KR support
- PCI Express Gen2/3
- Aligned with the SOSA™ Technical Standard



Overview

The **IC-ARM-VPX3c** is a low-power 3U VPX Single Board Computer (SBC) ideal for use in sensor systems, as well as applications needing high multi-threaded performance (target tracking or C4ISR).

Description

The **IC-ARM-VPX3c** is based on a NXP Layerscape® LX2080A/LX2160A multicore communication processor featuring 16 Arm® Cortex®-A72 cores. Layerscape LX2 family provides an excellent efficiency / Thermal Design Power (TDP) ratio with dissipated power as low as 30W for LX2080A and up to 45W for LX2160A. With its hardware accelerator and large caches, this SBC provides outstanding computing performance with powerful packet processing offload and Ethernet controllers.

The **IC-ARM-VPX3c** provides up to 32GB of DDR4-ECC, M.2 slot, eMMC, xSRAM and SATA3 storage solution interfaces, allowing system designers to meet large centralized system topology requirements and handle scenarios with heavy traffic on specific backplane segments.

The **IC-ARM-VPX3c** provides:

- 10/25/40/100 Gigabit Ethernet Data Plane
- PCI Express Gen2/3 Expansion Plane
- 10 Gigabit Ethernet Control Plane

The board meets the 25 gigabit-per-second Ethernet interfaces on a 3U VPX system backplane specified by the Sensor Open Systems Architecture (SOSA™) working group.

With its embedded Ethernet retimers with autonomous KR link training, the **IC-ARM-VPX3c** interfaces are immediately available under UBoot firmware. No specific driver is needed to support backplane's communications.

This 3U VPX module is compliant with the following VITA 65.0 OpenVPX Slot profile:

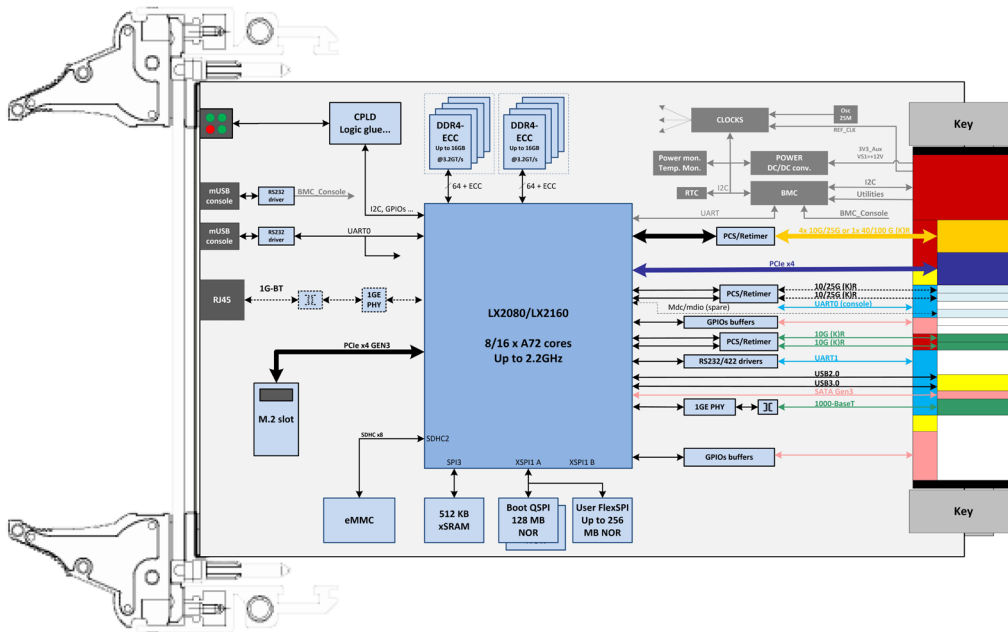
- SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16

The **IC-ARM-VPX3c** is compliant with the VITA 46.0 standard 3U module definitions. It is available in air-cooled and conduction-cooled versions. (1.5" AFT version possible. Please consult us). Front and back L2 maintenance covers are available for conduction-cooled models.

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Block Diagram



Main features

VPX connector interfaces

• Data Plane (P1)

- 1 * 40GBASE-KR4 (E8) or 1 * 100GBASE-KR4 (E18)
- 4 * 10GBASE-KR (4E7)
- 4 * 25GBASE-KR (4E8)

• Expansion plane (P1)

- 1 * PCIe Gen2/3 x4 port (P3F)

• Control Plane (P1 & P2)

- 2 * 10GBASE-KR (2E7)
- 1 * 1GBASE-T port (E3)

• Storage (P2)

- 1 * SATA3 Gen3 (S3)

• Serial ports (P1 & P2)

- 1 * RS232 UART (P1)
 - maintenance port
 - support for both LVCMOS and RS-232 voltage levels
- 1 * RS232 (M3) / RS422 UART (M4) (P2)

• USB (P2)

- 1 * USB2.0 / USB 3.1 (U2)
- 1 * USB2.0 (U1)
- Dedicated power supply pins on P1 and P2

• GPIOs (P1 & P2)

- 1 * USB2.0 / USB 3.1 (G1)

The **IC-ARM-VPX3c** is aligned with the SOSA™ Technical Standard to provide high interoperability in new modular systems. A simple software configuration provides the flexibility to switch between the SOSA™ Alternate Module Profile Schemes (AMPS) listed below:

MODA3-16.2.15-1-F2C-(E8/E18/4E7/4E8)(P3F)(2E7-E3)(S3-N-U2-U1-M3/M4-G1)<N>

Payload type		Physical definition				Backplane Copper Protocol/Speed/Width definition																XMC	
Payload card type	VITA 65 Slot profile	Vita 65 Alternate Naming Structure			Depth, cooling, pitch		Data Plane		Expansion Plane		Control Plane		CPU Interface/Misc								SOSA Only	XMC overlay	
							FP	EP1	UTP	TP	STR	VID01	USB01	USB02	SER01	GPIO		<					
																			A	>			
3U	I/O intensive	MODA3	-	16.2.15-1	-	F1C F2C	-	(E8 E18)	(P3F)	(2E7 E3)	(S3 - N -	U2 -	U1 -	M3 M4	-	G1)	N	>				

Hardware features

NXP Layerscape® LX2080A/LX2160A

- up to 2.2 GHz
- up to 32 GB DDR4-ECC
- 128MB Quad SPI NOR Flash
- 512 KB xSRAM
- eMMC
- All protected by NVMRO

Board Management Controller

- VITA 46.11-2015 hardware compliant
- STM32 µ-controller with security features
- RTC with supercap backup
- DC and Thermal sensors

- M.2 slot socket with PCIe Gen3 x4 interface

Software features

BMC

- VITA46.11 IPMC
 - TIER-2 IPMI
 - Redundant IPMB
- Power-on Built-In Test
 - On-board hardware components
 - Accessible from the OS
- Human Machine Interface
 - Devices management
 - Health management
 - Password
 - Log
- Over-temperature board protection

Firmware

- U-Boot Firmware
 - Based on NXP UBoot sources
 - Integrated and tested by IC R&D team
- Boot options
 - U-Boot shell
 - Storage devices (HDD, USB, CD, DVD)
 - Network
- Power-on Built-In Tests (PBIT)
 - On-board hardware components
 - Add-on connectivities (VPX PCIe, SATA disks, USB devices...)
 - Results accessible from the OS

OS Support

- Supported Linux distributions
 - Yocto
- BSP Features
 - Standard or Preemp-RT kernel (Yocto only)
 - BMC drivers
 - IC Control Node driver
 - Board information (P/N, S/N, PBIT results...)
 - IBIT/CBIT (Integrated/Continuous)
 - Other utilities

Please consult us for other Linux distributions and VxWorks®.

Accessories

Console cable

A dedicated SUBD-9 to mini-USB cable allows to connect standard RS-232 port to front-panel CPU and BMC console ports.

Engineering kit

Interface Concept has developed this tool to provide a high-density access to program/debug multiple target types like CPLDs, FPGAs, Processors, and Microcontrollers... used on IC products. It handles multiple interfaces like JTAG, I2C, SPI, COP, emulation bus, GPIO for factory programming as well as user's debugging.

Rear Transition Modules

Rear Transition Module - RTM131

3U VPX, 1" pitch wide according to VITA 46.0 Designed to be used with **IC-ARM-VPX3c** SBC with RS-232 or LVTTTL CPU console port on backplane.

• Front panel accesses

- CPU console port
- BMC console port
- 1 * QSFP+ connector
- 2 * SFP+ connectors
- 1 * RJ45 for 1GBASE-T port

• Internal accesses

- 1 * M.2 Socket (x4 M-Keyed slot)
- 1 * MSATA slot
- 1 * eUSB slot (USB 3.0 support)
- 1 * Vertical USB type A (USB 2.0 only)
- 1 * HE10-10 connector for 8 CPU's GPIOs
- 1 * HE10-10 connector for 1 RS-232 port
- 1 * HE10-10 connector for 1 RS-422/485 port



RTM131

Rear Transition Module - RTM145

3U VPX, 1" pitch wide according to VITA 46.0 Designed to be used with **IC-ARM-VPX3c** SBC. It features a 25/100G PHY on data plane to provide robust QSFP access.

• Front panel accesses

- CPU console port
- BMC console port
- 1 * QSFP+ connector for Data Plane
- 2 * SFP+ connectors for Control Plane
- 1 * RJ45 for 1/10GBASE-T port

• Internal accesses

- 1 * M.2 SATA slot
- 1 * Vertical USB type A (USB 2.0 only)



RTM145

• Embedded logic

- I2C bridge to (Q)SFP status/control signals

Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 71°C at the thermal interface (+) or 85° C (+)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (+)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (+)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(+) : Temperature grades are subject to availability according to IC products. Please consult us.

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For more information, please contact:



3, rue Félix Le Dantec
29000 QUIMPER
Tel. +33 (0)2 98 57 30 30
Fax. +33 (0)2 98 57 30 00
info@interfaceconcept.com