IC-FEP-VPX3h

3U VPX VITA 66.5 FPGA board with FMC+ Site

- *3U VPX - VITA 66.5*
- *1 * AMD Versal™ FPGA*
- *2 * DDR4 banks (up to 8GB each)*
- *1 * FMC+ site (VITA 57.4)*
- *SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11*
- *Aligned with the SOSA™ Technical Standard*

The **IC-FEP-VPX3h** 3U VPX board is based on an AMD Versal™ FPGA, a combination of adaptable processing and acceleration engines with programmable logic and configurable connectivity. These high-performance capabilities enable customized and heterogeneous hardware solutions for a wide array of applications. Such solutions provide a higher performance/watt ratio over conventional FPGAs, CPUs, and GPUs.

Description

The **IC-FEP-VPX3h** can support :

AI Edge VE1752: adaptive technology platform that combines high AI inference performance, low latency, and power efficiency for edge applications.

AI Core VC1702/VC1802/VC1902: high-compute series with medium density programmable logic and connectivity capability coupled with AI and DSP acceleration engines.

Prime VM1502/VM1802: mid-range series with medium density programmable logic, signal processing, and connectivity capability.

Depending on the selected target, the **IC-FEP-VPX3h** can provide:

- GTY from 25Gb/s up to 32 Gb/s,
- 40G/100G multirate Ethernet Mac hard IP

SOSA™ Sensor Open Systems Architecture MEMBER

The Data Plane Fat Pipe supports connection to a Versal™ MRMAC controller, supporting up to 100GB Ethernet directly connected to the internal NoC.

The two Fat Pipes of the Expansion Plane connected to GTY supporting AMD PCIe Gen4 hard IP and DMA subsystem provide a rich set of options for high performance data transfer between the **IC-FEP-VPX3h** and external devices.

They can be used as two PCIe Gen4 ports or merged to reach the 128GT/s of a PCIe x8 link.

Behind the GTYs connected to the FMC, it is possible to attach the 2 Hard IP PCIe and/or the 3 Hard IP MRMAC to provide very high speed interfaces : PCI Gen4 x4 and 100GB Ethernet.

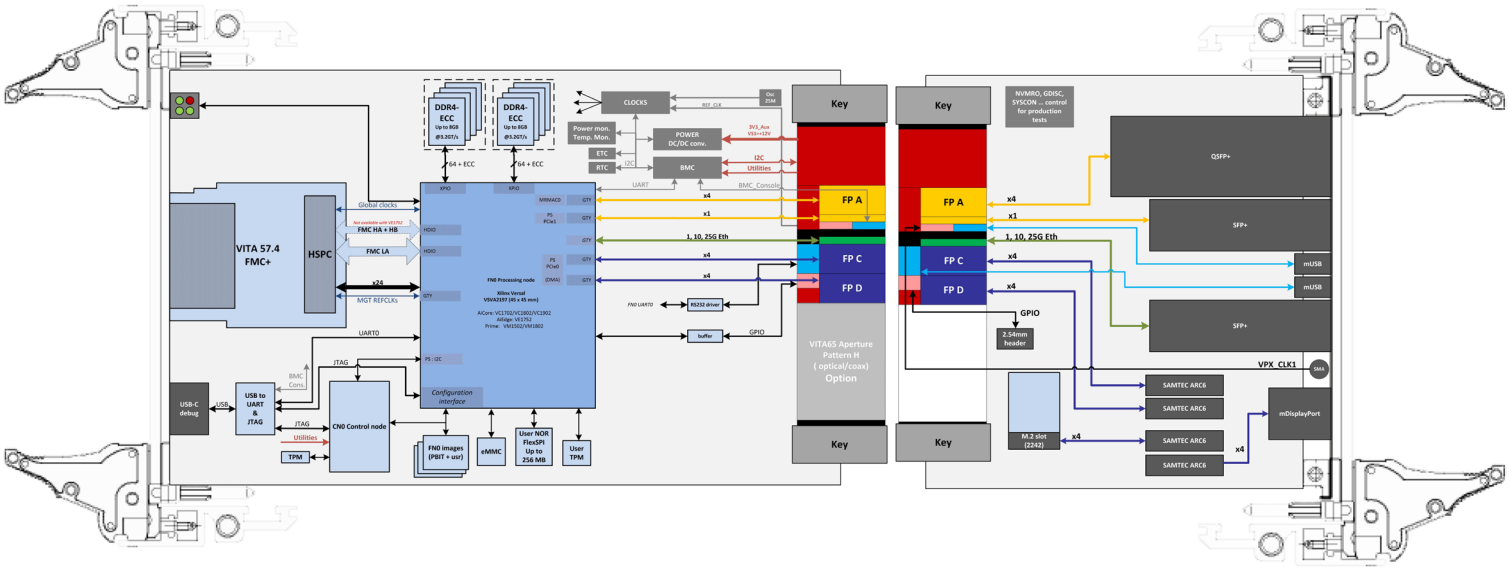
The FMC+ site of the **IC-FEP-VPX3h** is compliant with the FPGA Mezzanine Card standard (VITA 57.4), supporting plugin FMC modules provided by IC or developed by users.

The FMC+ site can be used for usual front connection or the report of the IOs (analog or optical) on the rear VITA 65 plug-in modules on P2.

With its FMC+ slot and the modularity of the rear VITA 65 plug-in modules, the **IC-FEP-VPX3h** allows to create optimized solutions for data processing with analog conversion, optical data transfer or a mix of both.

The **IC-FEP-VPX3h** and other IC building blocks (Intel® and PowerPC SBCs, Ethernet Switches & Routers, FMC) running our Signal Processing Reference Design are the ideal platforms to users who are willing to streamline development by concentrating their efforts on their most strategical tasks.

Block Diagram



Main features

Processing Unit

- AMD Versal™ AI Core, AI Edge or Prime
- 2 * banks of DDR4: 64-bit wide, up to 8GB each
- 3 * SPI flash (bitstreams storage)
- 1 * 256 MBytes of FlexSPI flash (User Data storage)
- 1 * eMMC module

FMC+ VITA 57.4 interfaces

- 6 * GTH x4 links
- up to 80 differential pairs(*)
- 6 reference clocks

(*) depending on FPGA models

BMC

- VITA 46.11-2015 hardware compliant
- RTC with supercap backup
- DC and Thermal sensors

Accessories

- Rear Transition Module (block diagram above)

Interface features

P0 connector

- VS3, 3V3_AUX, VS1 (+12V for FMC)
- REF_CLK
- I2C bus, utilities (SYSRESET, NVMRO, GAx)

P1connector

- 1 * Fat Pipe (Data plane) supporting MR-MAC instantiation
- 1 * Ultra Thin Pipe (Data plane)
- 2 * Fat Pipe (Expansion plane) supporting CPM4 instantiation
- 1 * Ultra Thin Pipe supporting 1G/10G/25G Ethernet (Control Plane)
- 1 * RS232 port

P2A and P2B connectors (VITA 66.5)

can be populated with (option)

- VITA 66.5 Style C or
- VITA 66.5 Style D connectors

On-board firmware

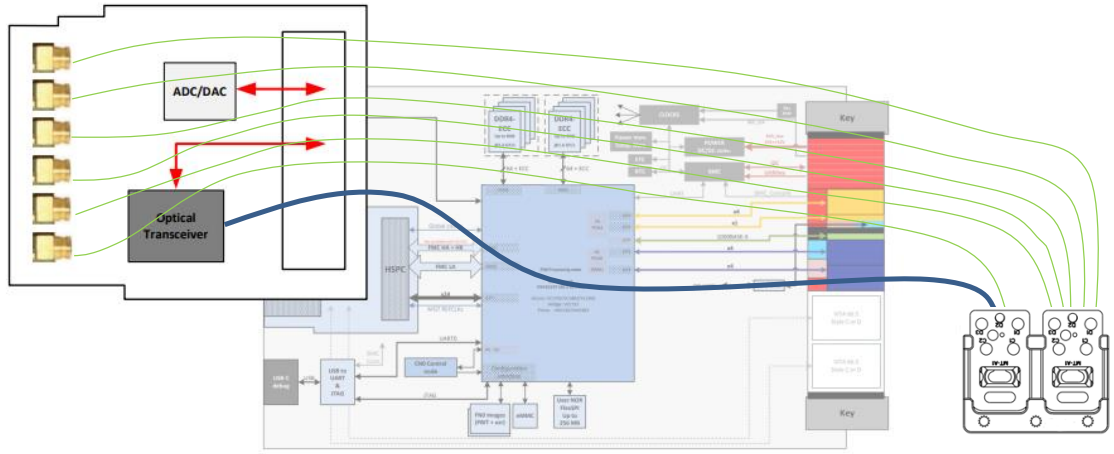
The **IC-FEP-VPX3h** hardware platform is compatible with AMD development tools Vivado™, AMD SmartLynq+ high-speed debug probe, etc.

Interface Concept provides

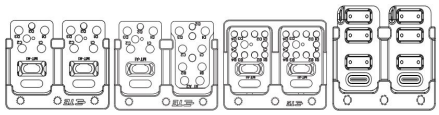
- VHDL code for system services (DDR4, PCIe, Aurora, IC FMC interfaces, etc.) and reference designs such as PCIe DMA Engine, signal capture & processing, etc.
- Host drivers for our CPU (Linux, VxWorks)

Customers can implement their own real-time applications with the capability to integrate existing Open Source code or third-party IP cores.

Case study



Thanks to the modularity of the supported VITA 65 plug-in modules (here below) and its FMC+ slot, it is possible to build FMC mezzanines optimized for customer's applications. Designs under consideration. Please consult us.



Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 71°C or 85° C (*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : Temperature grades are subject to availability according to IC products. Please consult us.

All information contained herein is subject to change without notice.

For more information, please contact:

INTERFACE CONCEPT
ADVANCED ELECTRONIC SOLUTIONS

3, rue Félix Le Dantec
29000 QUIMPER
Tel. +33 (0)2 98 57 30 30
Fax. +33 (0)2 98 57 30 00
info@interfaceconcept.com