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OpenVPX Backplanes Technical Reference Guide

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ARCHITECTURE

For more than a dacade OpenVPX has been the go-to form factor for rugged, high-performance computing in both defense and rugged commercial applications. OpenVPX, and its larger suite of associated VPX-related standards defines system level interoperability for multi-vendor, multi-module, integrated systems environments. The OpenVPX standard defines clear interoperability points necessary for integration from module to module, module to backplane and backplane to chassis.

OpenVPX purpose:

- Control and manage the assignment of OpenVPX pins to functional planes in an interoperable architecture
- To get a high-degree of interoperability, while leaving room for sensor- /application-specific augmentation
- To make the process of developing OpenVPX-based solutions from the lab to the field much more efficient in cost, time, quality, and repeatability

OpenVPX provides a descriptive language for identifying slot and module requirements and backplanes' capability. It also provides with the part number configuration more information on the control and fabric planes, including the signal speeds.

VITA FAMILY OF STANDARDS

The VITA trade association provides members with the ability to develop and design products based on open standards. The VITA Standards Organization (VSO) is an ANSI-accredited group that provides members with a means to work together to define and develop key computer specifications such as the family of VPX standards, which include those listed below. Elma is a key contributor to several of the Working Groups within VITA.

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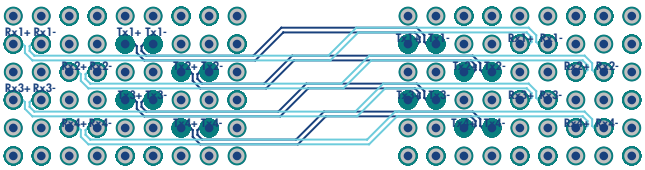
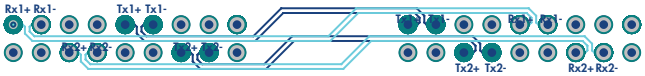
CONTACT US

PIPES: FAT, THIN, ULTRA THIN



Fat Pipe: A channel that is comprised of four links (4 Tx pairs + 4 Rx pairs) is being referred to as a Fat Pipe or by use of the x4 nomenclature. 100GBASE-KR4 and 40GBASE-KR4, 10GBASE-KX4, 10GBase-BX4, 10GBASE-T, PCIe-x4, sRIO-x4, Infiniband-x4



Thin Pipe: A channel that is comprised of two links (2 Tx pairs + 2 Rx pairs) is now being referred to as a Thin Pipe or by use of the x2 nomenclature. 10/100/1000BASE-T, PCIe-x2, sRIO-x2, Infiniband-x2

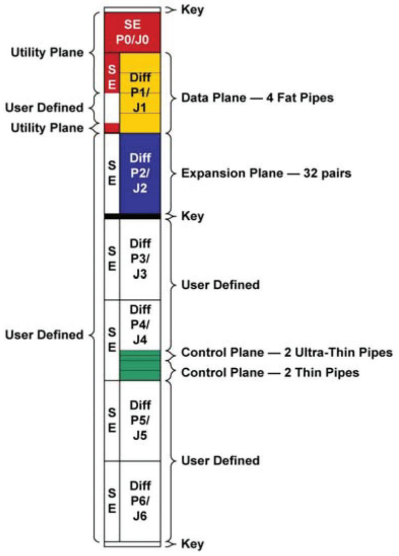
Ultra-thin Pipe: A channel that is comprised of one link (1 Tx pair + 1 Rx pair) is now being referred to as an Ultra Thin Pipe or by use of the x1 nomenclature. 10GBASE-KR, 1GBASE-KX, PCIe-x1, sRIO-x1, Infiniband-x1a

SLOT PROFILES

VITA 65 defines OpenVPX in terms of four types of Profiles: Slot Profiles, Backplane Profiles, Module Profiles and Chassis Profiles. Slot Profiles have a type, board size and clock variation. Slots have rows that are defined to support a variety of Pipe sizes or module apertures. Slot Profiles define where pipes or apertures are located and also indicated user defined wafer locations.

Backplane Profiles define how the Slots are interconnected. Backplane Profiles also define the bandwidth capability of the Pipes. Module Profiles indicate which Pipes or Apertures are supported and the signaling protocol and data rate associated with each Pipe. A Module Profile are fully compatible with a single Slot Profile but can be used in Slots that do not fully support all the defined channels.

The system integrator must ensure that pipes that are connected together in a backplane have modules that support the same signaling protocols. The chart below indicates how the various features of a Slot Profile are described.



SLTU y – PAY - nXnXnX-1X.x.x-n

Board Size
U = 3 or 6

y = Clock variations
- p = parallel termination
- s = series termination
- x = radial - not defined
- Omitted field = bussed

Slot type
- PAY = payload
- STO = storage
- PER = peripheral
- SWH = switch
- TIM = timing

n = # pipes or connector patterns

VITA 65 Sections 10 or 14

n = a line in the Slot Profile spreadsheet identifying specific connector aperture pattern (if any) and RF or optical module population (if any)

X = Type of Pipes or Aperture

Pipes (number of diff. pairs or discrete fibers
- S = Single Pipe (1)
- U = Ultra-thin (2)
- T = Thin (4)
- F = Fat (8)
- M = Ten (10)
- W = Twelve (12)
- D = Double (16)
- Q = Quad (32)
- O = Octal (64)

Connector aperture name (Connector Module size)
- A = 66.1 (full)
- B = 66.2 (full)
- C = 66.3 (full)
- E = 66.4/ 67.1/ 67.3A (half)
- G = 67.2/ 67.3B (full)
- H = 67.3C (full new)
- J = 67.3D (half new)
- K = 67.3E (full+half new)

Note: That order of Pipes is from top to bottom in the physical slot

CHALLENGING ENVIRONMENTS

OpenVPX systems are often deployed in harsh environments across a range of defense and industrial applications where excessive shock, vibration and high ambient temperatures are common.

AMPS - THE ALTERNATE MODULE PROFILE SCHEME

An important tool for defining what protocols and capabilities an individual plug-in card can support is the Alternate Module Profile Scheme, or AMPS. AMPS was developed in response to what was seen as an explosion of options being captured in VITA 65.1, which was resulting in a ballooning document that many were finding increasingly difficult to work with. VNX+ will adopt the AMPS approach for defining supported protocols for defined communications ports.

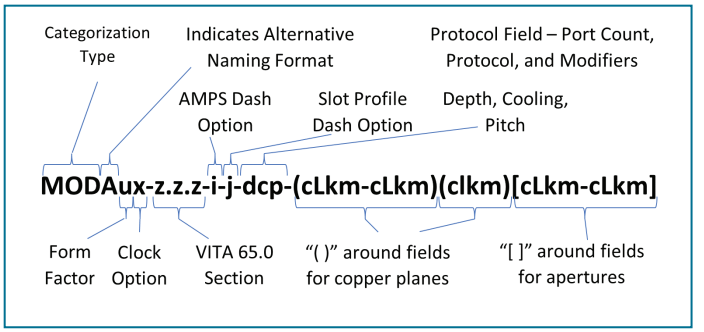


Figure 1: AMPS String Template

AMPS is a string built using the template in Figure 1. The supplier builds a string for their particular VPX plug-in card by filling the strings with the appropriate code in each field of the template. The early part of the string describes the general data about the card including the size (3U or 6U), VITA 65.0 section, and the slot profile "dash" option (indicating the aperture fill block pattern). The rest of the string is used to describe various communications ports found in the slot profile, what protocols the plug-in card supports, and any modifiers that are needed to describe the particular capabilities of each port.

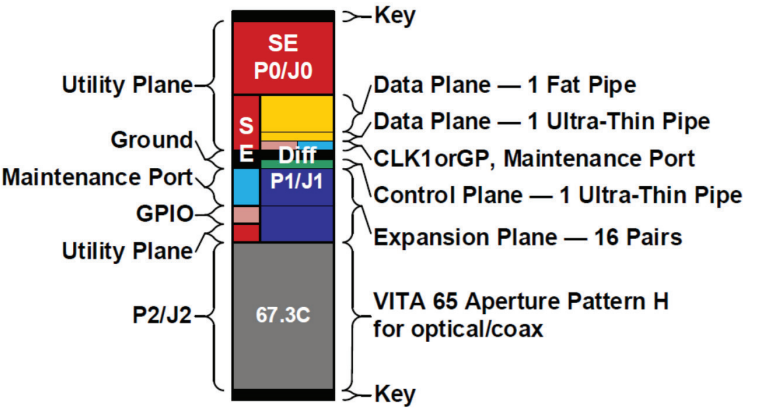


Figure 2: SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n slot profile

An example of an AMPS string for a sample SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-1 Payload card is:

MODA3p-16.6.11-1-4-F2C-(E8-E7)(P3F-A2F)(E7)(N-G5)

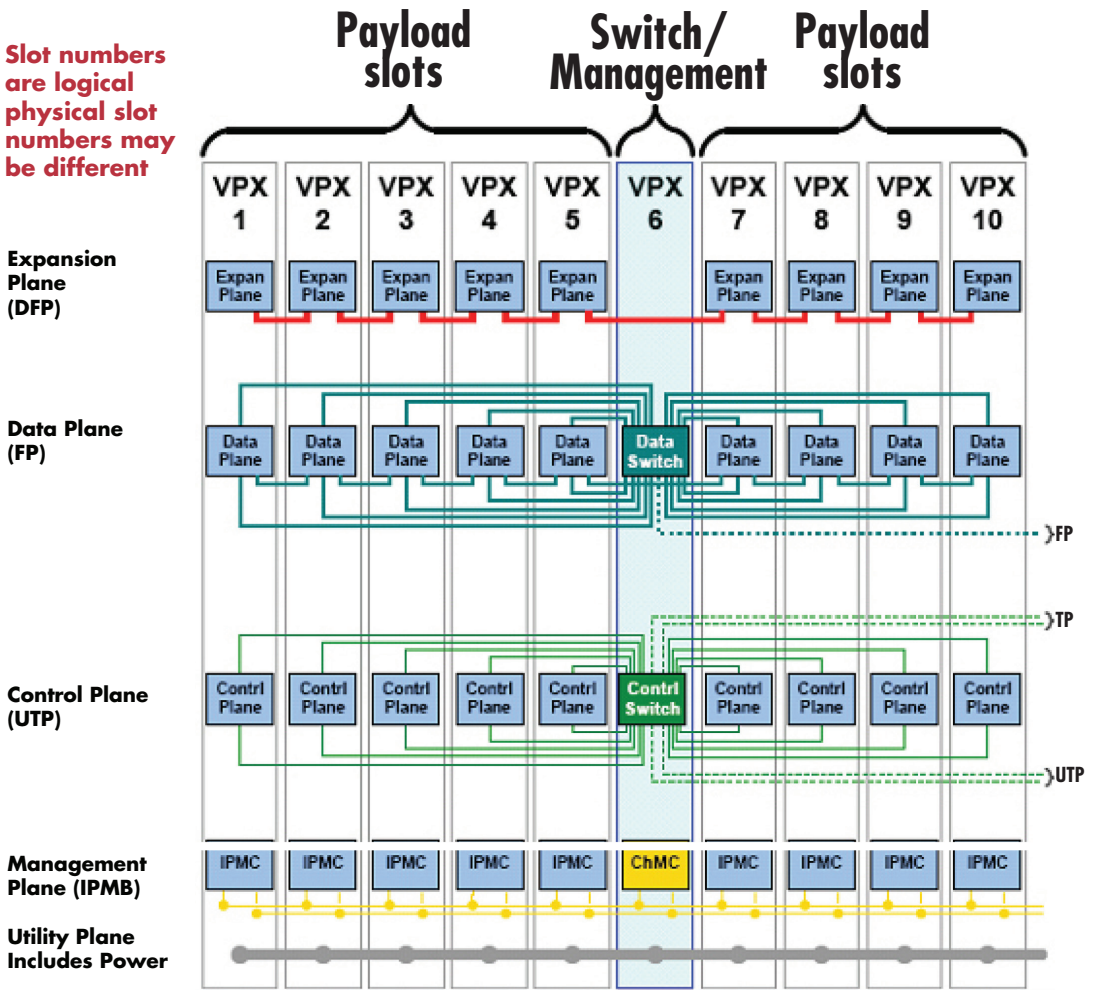
Which says that this card supports:

- Slot profile SLT3p-PAY-1F1U1S1S1U1U2F1H-14.6.11-4, module profile MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-4
- Module is full depth (160mm), 1.0 inch pitch, and VITA 48.2 cooling (conduction cooled)
- Data Plane has DP01 with 40GBASE-KR4 (with full autonegotiation rules as per VITA 65.0 section 5.1.8)
  DPutp01 with 40GBASE-KR4 (with with the same rules as per VITA 65.0 section 5.1.7)
- Expansion Plane has EP00 to EP03 with PCIe Gen 3 (with full rules as per 5.3.3.3)
  EO04 to EP07 with Aurora (section 5.1.7)
- GPIO1 is no-connect
- CLK is implemented as per section 5.15.5

If the board were configured for fixed DP01 configurations (that is, non autonegotiation) of 100GBASE-KR4 or 40GBASE-KR4, then the AMPS string would change to: MODA3p-16.6.11-1-4-F2C-(E18/E8-E7)(P3F-A2F)(E7)(N-G5)
For more information on AMPS strings please refer to the VITA 65.0 standard document.

TOPOLOGIES

The backplane configuration examples show the connectivity across the backplane for various planes. This includes the routing topology across the data plane and the connections across the expansion, control, management and utility planes. They also provide an illustration of the slot types, whether payload, switch or legacy bus slots.



DATA RATES

As signal speeds increase, backplane design can influence signal integrity (SI) - every trace, layer separation, turn bend, via, via transition,etc. Elma's signal integrity analysis and simulations consider every element in the channel to ensure optimal performance.

We focus on each feature individually to model the complete channel and optimize the return loss for each. Once modeled, they are concatenated together along with the trace and connector models to create the complete channel.

Today's critical high-speed systems require nothing less than reliable, repeatable solutions - every time.

UTILITY SIGNALS

J0/P0 Pin/Signal	Description
Vs1	High Voltage Power Input 1 Voltage specified in VITA 65. Capability per VITA 46.0 Table 4-5
Vs2	High Voltage Power Input 2 Voltage specified differently for 3U or 6U in VITA 65. Capability per VITA 46.0 Table 4-5
Vs3	Low Voltage Power Input 3 Voltage specified in VITA 65. Capability per VITA 46.0 Table 4-5
GA[4:0]*, GAP*	Geographical Address Inputs 0-4, Parity. Grounded in each slot per VITA 46.0 Table 7-1.
SM[3:0]	System Management connections bussed per Phillips Semiconductor I2C-Bus Specification, Version 2.1, January 2000
AUX_CLK+/-	Optional auxiliary reference clock (see ANSI/VITA 65) matched better than 8.5 pS and differentially terminated to 130 Ohms ± 10%. Often used for 1PPS precision clock.
3.3V_AUX	3.3V Auxiliary power, System Management, 1.0 A per slot.
+/- 12V_AUX	Auxiliary Power Supplies, 1.0 A per slot.
SYSRESET*	System Reset, bussed to all slots & terminated w 5% 220-ohm pull-up resistors to 3.3V AUX & 1.8K-ohm pull-down to GND or equiv.
REF_CLK+/-	Reference Clock 25 or 100 MHz matched better than 8.5 pS and differentially terminated at each end with a resistor of 61.9 Ohms ± 1%.
NVMRO	Non-Volatile Memory Read Only, bussed to all slots and pulled to 3.3V_AUX through 5% 220 ohm resistor
TCK, TMS, TRST*, TDI, TDO	JTAG Signals, not bussed or terminated on the backplane.
No Pad	The construction of the connector wafer is such that there is no circuit pad in this location

JJ1/P1 Pin/Signal	Description
GDiscrete1	Optional single ended general purpose I/O signal, bussed to each slot.
P1-VBAT	Battery Voltage, Bussed, 3V +/- 15% source on the backplane.
SYS_CON*	When grounded the backplane the SYS_CON mode is set. Implemented in by a jumper at any slot to be so designated.
MaskableReset*	Optional local reset input to Plug-In Module in addition to global SYSRESET*. Implemented as "opt-in" via jumper at each slot.

VITA 65.0 Table 3.7-2 Utility Plane Signals on J0

	Row i
1	GDiscrete1
2	GND
3	P1-VBAT
4	GND
5	SYS_CON*
6	GND
7	Reserved
8	GND
9	UD
10	GND
11	UD
12	GND
13	UD
14	GND
15	MaskableReset*
16	GND

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_ CLK-	REF_ CLK+	GND	GND	AUX_ CLK-	AUX_CLK+	GND	GND

← UD pins in Row i can be assigned by Slot Profiles in Sections 10 and 14.

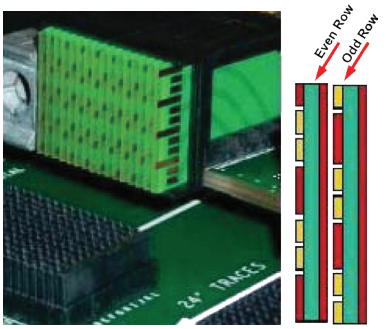
The pairs on Rows a thru h are assigned by Slot Profiles in Sections 10 and 14.

BACKPLANE AND DAUGHTER CARD PINOUT CHART

This chart shows the specification pinout of both the backplane and daughter card for J2-J6. Note the differences between the plug-in module and the backplane (even and odd pins) for Row E and Row B. Although the number of rows is different, the connector arrangement allows single-ended signals in these areas. The backplane and daugther card connectors mate without issue.

	Row G	Row F	Row E		Row D	Row C	Row B		Row A
			Even	Odd			Even	Odd	
Back-plane J2-J6	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	SEwafer1	GND	GND-J2	LN0-TD-	LN0-TD+	GND	GND-J2	LN0-RD-	LN0-RD+
2	GND	LN1-TD-	LN1-TD+	GND-J2	GND	LN1-RD-	LN1-RD+	GND-J2	GND
3	SEwafer3	GND	GND-J2	LN2-TD-	LN2-TD+	GND	GND-J2	LN2-RD-	LN2-RD+
4	GND	LN3-TD-	LN3-TD+	GND-J2	GND	LN3-RD-	LN3-RD+	GND-J2	GND
5	SEwafer5	GND	GND-J2	LN4-TD-	LN4-TD+	GND	GND-J2	LN4-RD-	LN4-RD+
6	GND	LN5-TD-	LN5-TD+	GND-J2	GND	LN5-RD-	LN5-RD+	GND-J2	GND
7	SEwafer7	GND	GND-J2	LN6-TD-	LN6-TD+	GND	GND-J2	LN6-RD-	LN6-RD+
8	GND	LN7-TD-	LN7-TD+	GND-J2	GND	LN7-RD-	LN7-RD+	GND-J2	GND
9	SEwafer9	GND	GND-J2	LN8-TD-	LN8-TD+	GND	GND-J2	LN8-RD-	LN8-RD+
10	GND	LN9-TD-	LN9-TD+	GND-J2	GND	LN9-RD-	LN9-RD+	GND-J2	GND
11	SEwafer11	GND	GND-J2	LN10-TD-	LN10-TD+	GND	GND-J2	LN10-RD-	LN10-RD+
12	GND	LN11-TD-	LN11-TD+	GND-J2	GND	LN11-RD-	LN11-RD+	GND-J2	GND
13	SEwafer13	GND	GND-J2	LN12-TD-	LN12-TD+	GND	GND-J2	LN12-RD-	LN12-RD+
14	GND	LN13-TD-	LN13-TD+	GND-J2	GND	LN13-RD-	LN13-RD+	GND-J2	GND
15	SEwafer15	GND	GND-J2	LN14-TD-	LN14-TD+	GND	GND-J2	LN14-RD-	LN14-RD+
16	GND	LN15-TD-	LN15-TD+	GND-J2	GND	LN15-RD-	LN15-RD+	GND-J2	GND

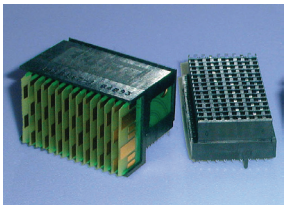
OPENVPX CONNECTOR



With the exception of J0 rows 1-6, OpenVPX daughter card connectors are constructed of alternating even and odd wafer elements. As a result of this design, the odd wafer rows have a SE pin in daughter card column "g" that corresponds to backplane wafer column "i".

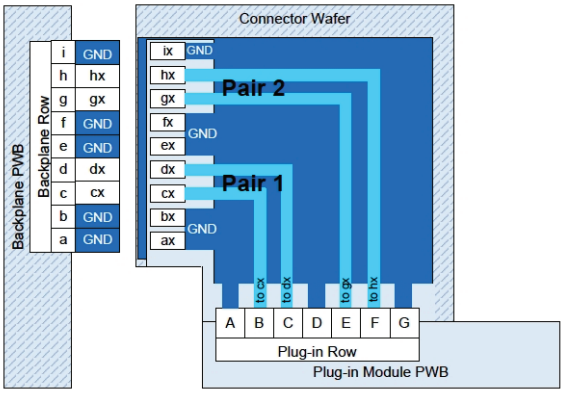
Elma provides backplanes with connectors in accordance with ANSI-VITA 46. Backplanes can also be assembled with backplane connectors in accordance with ANSI-VITA 60 or 63 connectors or a combination of slots fitted with VITA 46, 60 or 63 connectors as they are all footprint compatible, though not intermateable.

CHARACTERISTICS

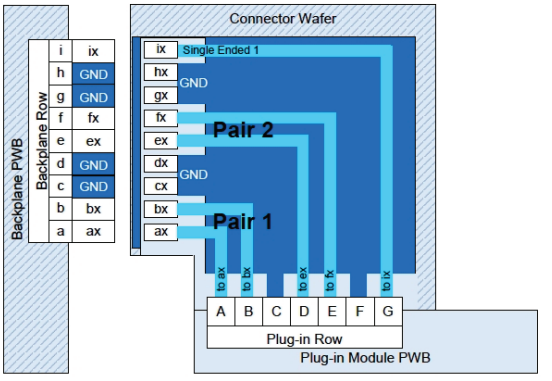


Operating Voltage:	50 Volts AC peak or DC
Current:	1 amp at <30°C (single circuit, free air)
Temperature:	-55°C to 105°C
Insulation resistance:	1000 megohms minimum
Temperature rise vs. current:	30°C maximum temperature at 1 amp load,

ODD AND EVEN WAFER DESIGN



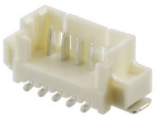
VITA 46 Wafer - Even Differential Pair

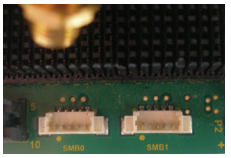


VITA 46 Wafer - Odd Differential Pair

INTELLIGENT PLATFORM MANAGEMENT INTERFACE (IPMB) - SMT

All of Elma's OpenVPX backplanes include at least one SMT connector for the Intelligent Platform Management Interface (IPMB).





Number of Positions:	5
Number of Rows:	1
Operating Temperature:	85.0°C (max)
Contact Material:	Phosphor Bronze
Flammability Rating:	UL 94 V-0
Gender:	Male
Current Rating:	1.3A at @ 30°C rise
Mfg Part Number:	Molex PicoBlade(tm) 53398-0571

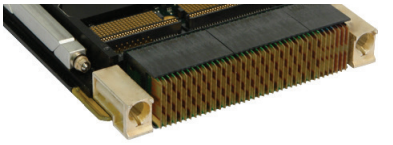
KEYING GUIDE

OpenVPX alignment and module keying is accomplished by the use of pins on the backplane and sockets on the daughter card. The pins have a flat side that can be oriented in five different positions: 0, 45, 90, 270 or 315 degrees. In standard development backplanes, each slot has a unique key combination.

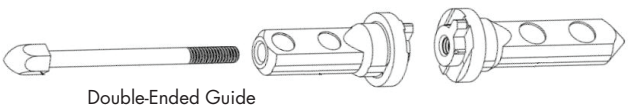
The chart below gives the recommended keying arrangement for 3U or 6U backplanes. Additionally, the key receptacle on the daughter card has electrical contacts so that the keying is part of the OpenVPX safety ground system. The backplane key orientation can be changed by the user, and a daughter card receptacle key can be a full circle without a flat, which allows a daughter card to be placed over backplane keys of any orientation. Double-ended backplane guide modules provide RTM keying and alignment.

Backplane Slot*	Voltage Key Position 1	Key Position 2	Key Position 3
Slot 1	315	270	270
Slot 2	315	315	270
Slot 3	315	0	270
Slot 4	315	45	270
Slot 5	315	90	270
Slot 6	315	270	315
Slot 7	315	315	315
Slot 8	315	0	315
Slot 9	315	45	315
Slot 10	315	90	315
Slot 11	315	270	0
Slot 12	315	315	0
Slot 13	315	0	0
Slot 14	315	45	0
Slot 15	315	90	0
Slot 16	315	270	45
Slot 17	315	315	45
Slot 18	315	0	45
Slot 19	315	45	45
Slot 20	315	90	45
Slot 21	315	270	90
Slot 22	315	315	90
		Backplane	FTM RTM
Front Module		1469491-C	1469492-C
Front Rear Double Key*		1410956-C	1469492-C
* Double ended for backplane. FTM and RTM use same			

Keying Pin



Keying Guide



Double-Ended Guide

OPENVPX - AVAILABLE POWER & VOLTAGE ASSIGNMENTS

The chart below gives maximum power per OpenVPX slot based upon VITA 46 and profiles defined in VITA 65.

Voltage Level	3U watts/slot	6U watts/slot	per wafer due to connector limits
Only 3V	69	N/A	23 Amps†
Only 5V	115	115	23 Amps†
Only 12V*	276	384	23 Amps† (3U), 16 Amps‡ (6U)
VS1, VS2, and VS3	240	348	12 Amps§
Only 48v per VITA 46	N/A	768	16 Amps‡ (VS1 and VS2)

Note: †= 1 power wafer used, ‡=2 power wafers used, §=3 power wafers used

The assignment of voltages on VS1, VS2 and VS3 is different for 3U and 6U cards. In addition, more voltage options are alowed for VS1 and VS2 in VITA 46 than are currently defined within VITA 65.

SIGNAL ASSIGNMENTS FOR THE J0 CONNECTOR PER VITA 46.0 AND VITA 65

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET'	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1'	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	TMS	TMS	TRST*
8	GND	REF_CLKK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

3U POWER ASSIGNMENTS FOR THE J0 CONNECTOR PER VITA 65

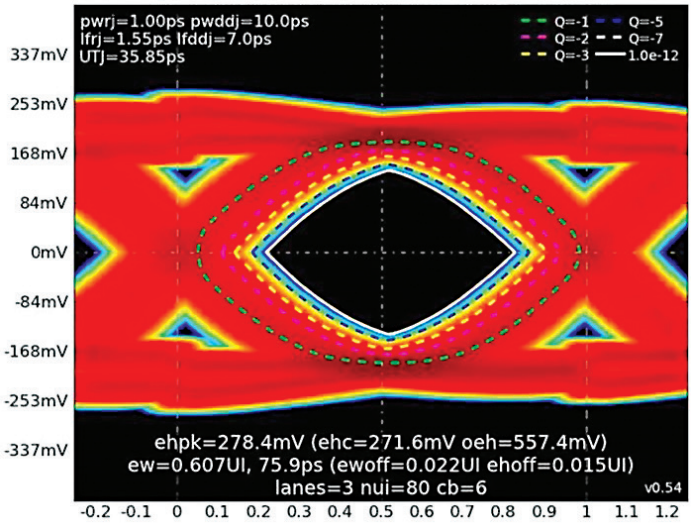
	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	12V	12V	12V	12V	No Pad*	3V	3V	3V	3V
2	12V	12V	12V	12V	No Pad*	3V	3V	3V	3V
3	5V	5V	5V	5V	No Pad*	5V	5V	5V	5V
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET'	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1'	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	TMS	TMS	TRST*
8	GND	REF_CLKK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

6U POWER ASSIGNMENTS FOR THE J0 CONNECTOR PER VITA 65

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	12V	12V	12V	12V	No Pad*	12V	12V	12V	12V
2	12V	12V	12V	12V	No Pad*	12V	12V	12V	12V
3	5V	5V	5V	5V	No Pad*	5V	5V	5V	5V
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET'	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1'	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	TMS	TMS	TRST*
8	GND	REF_CLKK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

OPENVPX SIGNAL INTEGRITY CONSIDERATIONS

With OpenVPX backplanes pushing the speed envelope, every feature of the design can influence signal integrity – every trace, layer separation, turn bend, via, via transition, etc. Elma's signal integrity analysis and simulations look at the entire channel in order to ensure optimal performance.



Our simulation is very detailed, looking closely at each element in the channel. We focus on each of the various structures and launches, along with lossy trace models, to model the complete channel as accurately as possible. By focusing on each structure individually, we can optimize the return loss for each. Once the structures are modeled, they are concatenated together along with the lossy trace models and connector models to create the complete channel. When there are four complete coupled channels modeled - 2 TX and 2 RX - we utilize a connector model that also has four pairs. Transmission lines are created in W-element tabular format using RLGC, a 2D Field Solver. The fitted attenuation, IL, ILD, RL and ICR will be compared to the channel requirements. We use symmetry and algebraically add noise components to account for the total noise in the system. This total noise includes the coupled noise generated in the connector via fields as well as the connectors themselves.

We generate S-parameter models and run the simulation in Ansoft HFSS. For instance, when dealing with a typically thick 30-layer N4000-13EPSI backplane design, we need to ensure compliance to the stringent 10 or 25 Gbps KR frequency domain requirements. For each simulation, four complete channels (2-TX and 2-RX) are modeled. These channels are coupled together in the connector via footprints as well as the connector models to account for the total noise generated. We start by modeling the worst-case channel parameters. This would include a channel being routed on the lowest backplane layer (L28) in the stack. We will use the largest multilane connector model available. For PCIe Gen3 or Gen4 analysis, SEASIM is the preferred tool for channel performance. If problems are encountered, specific recommendations for resolving those problems are recommended and verified via additional simulation.

QUALITY BEGINS & ENDS WITH THE CUSTOMER

This is reflected throughout Elma. Our quality procedures meet ISO 9001 & AS9100C standards, ensuring that we meet the most rigorous requirements.

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