AA1404002-E6-OPC

Avaya/Nortel® AA1404002-E6 Compatible TAA 40GBase-LX4 QSFP+ Transceiver (SMF, 1270nm to 1330nm, 150m, LC, DOM)

Features

- SFF-8436 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free

Applications:

- 40GBase Ethernet
- Access and Enterprise

Product Description

This Avaya/Nortel® AA1404002-E6 compatible QSFP+ transceiver provides 40GBase-LX4 throughput up to 150m over single-mode fiber (SMF) using a wavelength of 1270nm to 1330nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Avaya/Nortel® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	TS	-40		85	°C
Operating Temperature	Top	0		70	°C
Power Supply Voltage	Vcc	-0.5		3.6	V
Relative Humidity	Rh	0		85	%
Damage Threshold, each Lane	THd	4.5			dBm

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	T_{OP}	0		70	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance (OM3 MMF)	D_{MMF}			150	m
Link Distance (SMF)	D_{SMF}			2	km

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Consumption				3.5	W	
Supply Current	Icc			1.1	A	
Transceiver Power-on Initialization Time				2000	ms	1
Transmitter (each lane)						
Single-ended Input Voltage Tolerance (Note 2)		-0.3		4.0	V	Referred to TP1 signal common
AC Common mode Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	190		700	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Differential Input Return Loss	See IEEE 802.3ba 86A.4.11				dB	10MHz-11.1GHz
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye Mask Coordinates {X1, X2, Y1, Y2}	0.11, 0.31 95, 350				UI mV	Hit Ratio = $5x10^{-5}$
Receiver (each lane)						
Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss	See IEEE 802.3ba 86A.4.2.1				dB	10MHz-11.1GHz
Common-mode Output Return Loss	See IEEE 802.3ba 86A.4.2.2				dB	10MHz-11.1GHz
Output Transition Time		28			ps	20% to 80%
J2 Jitter Output	Jo2			0.42	UI	
J9 Jitter Output	Jo9			0.65	UI	
Eye Mask Coordinates {X1, X2, Y1, Y2}	0.29, 0.5 150, 425				UI mV	Hit Ratio = $5x10^{-5}$

Notes:

1. Power-on initialization time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.

2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

Optical Characteristics

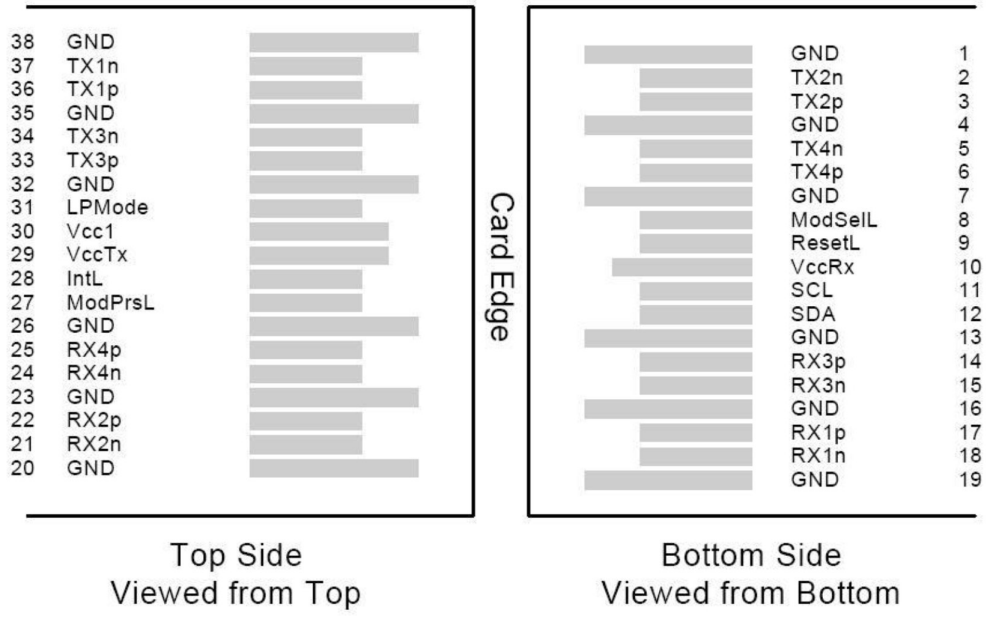
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Total Average Launch Power (for SMF)	P_T, SMF			8.3	dBm	
Total Average Launch Power (for MMF)	P_T, MMF			9.5	dBm	
Average Launch Power, each Lane (for SMF)	P_{AVG}, SMF	-7.0		2.3	dBm	
Average Launch Power, each Lane (for MMF)	P_{AVG}, MMF	-5.0		3.5	dBm	
OMA, each Lane (for SMF)	P_{OMA}, SMF	-6.0		3.5	dBm	1
OMA, each Lane (for MMF)	P_{OMA}, MMF	-4.0		4.5	dBm	
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			6.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-6.8			dBm	
TDP, each Lane	TDP			2.6	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	12dB reflection
Transmitter Reflectance	R_T			-12	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}	{0.23, 0.34, 0.43, 0.27, 0.35, 0.4}					
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	TH_d	4.5			dBm	2
Total Average Receive Power (for SMF)				8.3	dBm	
Total Average Receive Power (for MMF)				9.5	dBm	
Average Receive Power, each Lane (for SMF)		-11.7		2.3	dBm	
Average Receive Power, each Lane (for MMF)		-7.0		3.5	dBm	
Receiver Reflectance	R_R			-26	dB	

Receive Power (OMA), each Lane (for SMF)				3.5	dBm	
Receive Power (OMA), each Lane (for MMF)				4.5	dBm	
Receiver Sensitivity (OMA), each Lane (for SMF)	SEN_{SMF}			-11.5	dBm	
Receiver Sensitivity (OMA), each Lane (for MMF)	SEN_{MMF}			-10.5	dBm	
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			7.5	dB	
LOS Assert	LOSA	-28			dBm	
LOS Deassert	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			12.3	GHz	

Notes:

1. Even if the TDP < 0.8 dB, the OMA min must exceed the minimum value specified here.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Electrical Pin-out Details



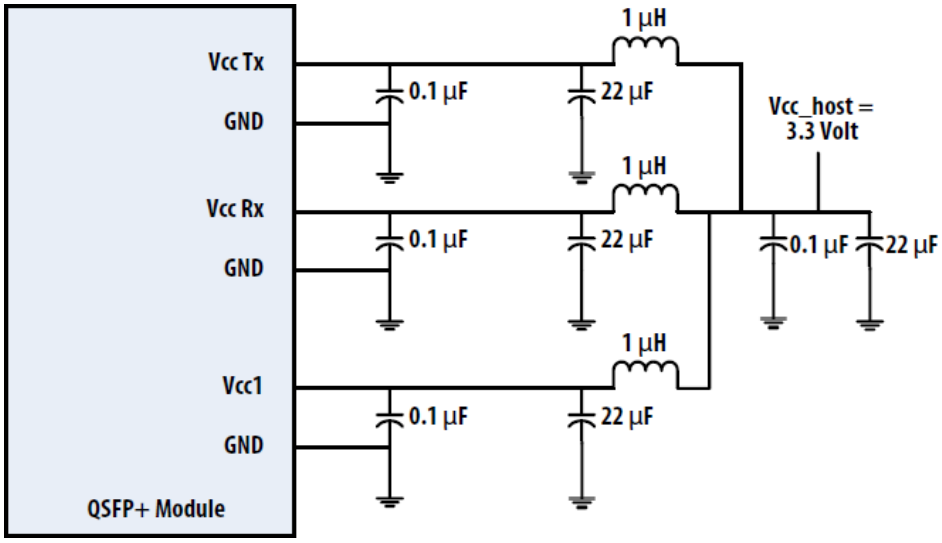
Pin Descriptions

Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Recommended Power Supply Filter



Mechanical Specifications