SFP-10GB-DW-C-S5-I-C-OPC

Cisco® Compatible TAA 10GBase-DWDM SFP+ Transceiver (Smart-Tunable, 80km, LC, DOM, -40 to 85C)

Features

- SFF-8432 and SFF-8472 Compliance
- Duplex LC Connector
- Smart-Tunable
- Operating Temperature -40 to 85 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead-free

Applications:

- 10x Gigabit Ethernet over DWDM
- 8x/10x Fibre Channel
- Access, Metro and Enterprise

Product Description

This Cisco® compatible SFP+ transceiver provides 10GBase-DWDM throughput up to 80km over single-mode fiber (SMF) using an smart-tunable wavelength of 1530nm to 1565nm via an LC connector. It can operate at temperatures between -40 and 85C. It is guaranteed to be 100% compatible with the equivalent Cisco® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

ITU Channel Wavelength Guide

ITU Channel	Frequency (THz)	Center Wavelength (nm)	ITU Channel	Frequency (THz)	Center Wavelength (nm)
13.5	191.35	1566.72	**37.5**	193.75	1547.32
14	191.40	1566.31	**38**	193.80	1546.92
14.5	191.45	1565.90	**38.5**	193.85	1546.52
15	191.50	1565.50	**39**	193.90	1546.12
15.5	191.55	1565.09	**39.5**	193.95	1545.72
16	191.60	1564.68	**40**	194.00	1545.32
16.5	191.65	1564.27	**40.5**	194.05	1544.92
17	191.70	1563.86	**41**	194.10	1544.53
17.5	191.75	1563.45	**41.5**	194.15	1544.13
18	191.80	1563.05	**42**	194.20	1543.73
18.5	191.85	1562.64	**42.5**	194.25	1543.33
19	191.90	1562.23	**43**	194.30	1542.94
19.5	191.95	1561.83	**43.5**	194.35	1542.54
20	192.00	1561.42	**44**	194.40	1542.14
20.5	192.05	1561.01	**44.5**	194.45	1541.75
21	192.10	1560.61	**45**	194.50	1541.35
21.5	192.15	1560.20	**45.5**	194.55	1540.95
22	192.20	1559.79	**46**	194.60	1540.56
22.5	192.25	1559.39	**46.5**	194.65	1540.16
23	192.30	1558.98	**47**	194.70	1539.77
23.5	192.35	1558.58	**47.5**	194.75	1539.37
24	192.40	1558.17	**48**	194.80	1538.98
24.5	192.45	1557.77	**48.5**	194.85	1538.58
25	192.50	1557.36	**49**	194.90	1538.19
25.5	192.55	1556.96	**49.5**	194.95	1537.79
26	192.60	1556.56	**50**	195.00	1537.40
26.5	192.65	1556.15	**50.5**	195.05	1537.00
27	192.70	1555.75	**51**	195.10	1536.61
27.5	192.75	1555.34	**51.5**	195.15	1536.22
28	192.80	1554.94	**52**	195.20	1535.82
28.5	192.85	1554.54	**52.5**	195.25	1535.43
29	192.90	1554.13	**53**	195.30	1535.04
29.5	192.95	1553.73	**53.5**	195.35	1534.64
30	193.00	1553.33	**54**	195.40	1534.25
30.5	193.05	1552.93	**54.5**	195.45	1533.86
31	193.10	1552.52	**55**	195.50	1533.47
31.5	193.15	1552.12	**55.5**	195.55	1533.07
32	193.20	1551.72	**56**	195.60	1532.68
32.5	193.25	1551.32	**56.5**	195.65	1532.29
33	193.30	1550.92	**57**	195.70	1531.90
33.5	193.35	1550.52	**57.5**	195.75	1531.51
34	193.40	1550.12	**58**	195.80	1531.12
34.5	193.45	1549.72	**58.5**	195.85	1530.72
35	193.50	1549.32	**59**	195.90	1530.33
35.5	193.55	1548.91	**59.5**	195.95	1529.94

35.5	193.55	1548.91	**59.5**	195.95	1529.94
36	193.60	1548.52	**60**	196.00	1529.55
36.5	193.65	1548.11	**60.5**	196.05	1529.16
37	193.70	1547.72	**61**	196.10	1528.77

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Maximum Supply Voltage	Vcc	0	3.6	V	+3.3V
Optical Receiver Input	P_{IMAX}		5	dBm	Average
Operating Case Temperature	Tc	-40	85	°C	
Storage Temperature	T_{stg}	-40	85	°C	
ESD SFI pins	ESD1		1	kV	HBM
ESD except for SFI pins	ESD2		2	kV	HBM
Data Rate	DR	1.2	11.3	Gbps	NRZ

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	+3.3V
Supply Current	Icc			0.73	A	
Power Consumption	PDS			2.3	W	
Low Speed Control Pin Logic Levels						
Host Vcc Range	Host_Vcc	3.14		3.47	V	with ± 5% variation
TX_Fault, RX_LOS	VOL	0.0		0.4	V	Note 1
	VOH	Vcc-0.5		Vcc+0.3	V	Note 1
TX_Disable	VIL	-0.3		0.8	V	Pulled up with 10kΩ to VccT in the module
	VIH	2.0		VccT +0.3	V	

Notes:

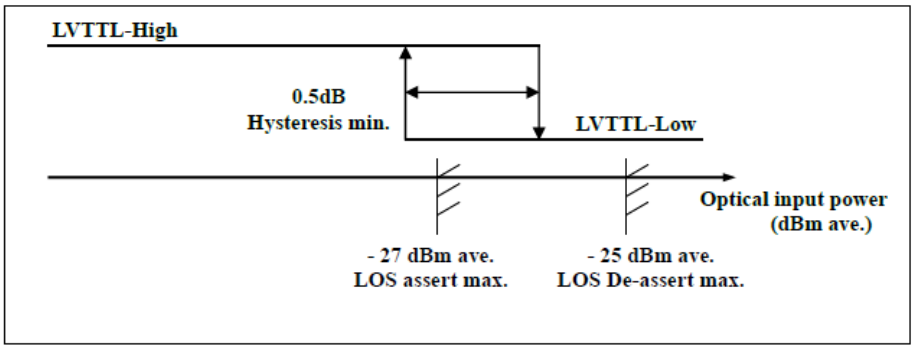
1. Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measures at the Host side of the connector.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Frequency range		191.35		196.10	THz	50GHz grid, 96 channels
Frequency accuracy		-2.5		2.5	GHz	EOL
Optical transmit power	Po	-1		3	dBm	EOL
Shuttered output power				-35	dBm	
Optical power stability	ΔPo	-1		1	dB	All channels, SOL
Side mode suppression	SMSR	35			dB	±2.5nm, modulated
Spectral width	Δλ		0.3	0.5	nm	-20dB, modulated
Extinction ratio	ER	8.2			dB	Filtered, 10.3Gbps
Eye diagram compliance		GR-253, ITU-T G.691				
Mask margin		10			%	
Tuning speed				10	s	warmed-up, from any CH to any other CH
Receiver						
Input operating wavelength		1525		1575	nm	
Minimum Receiver Sensitivity (Back to Back)	P_{rmin}			-24	dBm	10.709Gbps, 1E-12, OSNR>35dB
Minimum receiver sensitivity (-300~+1400ps/nm)	P_{rmin}			-21	dBm	
Maximum input power (overload)	Pro	-7			dBm	
Receiver Reflectance	RL			-27	dB	
LOS Assert		-27.5			dBm	Note 1
LOS De-Assert				-24	dBm	Note 1
LOS Hysteresis		0.1			dB	Note 1
LOS Assert Time				100	us	
LOS De-Assert Time				100	us	

Notes:

1.



SFP+ 2 Wire Interface Requirements

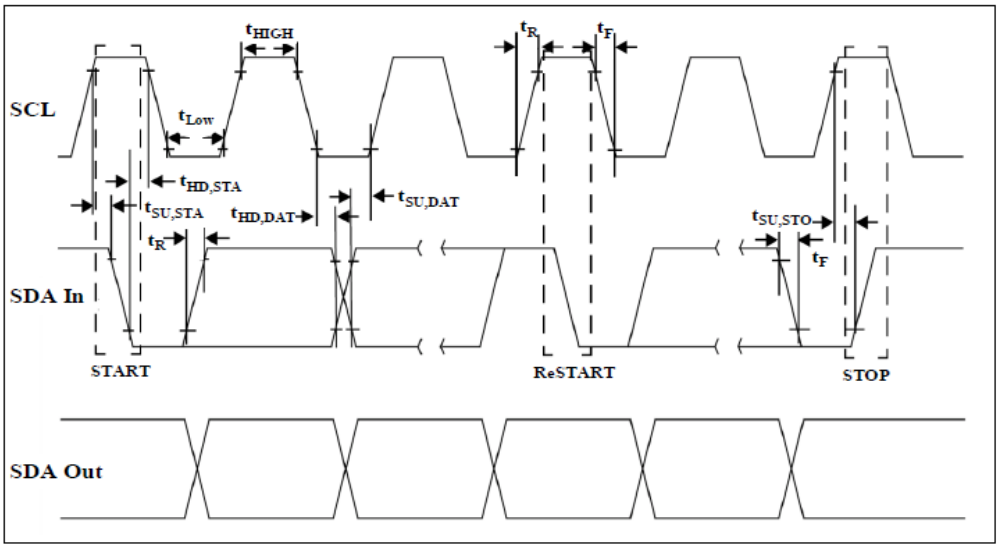
Parameter	Symbol	Min	Max	Unit	Conditions
Timing Requirements					
Clock Frequency	fSCL	100	400	kHz	
Clock Pulse Width Low	tLOW	1.3		µs	
Clock Pulse Width High	tHIGH	0.6		µs	
Time bus free before new transaction can start	tBUF	20		µs	Between STOP and START
START Hold time	tHD,STA	0.6		µs	
START Set-Up time	tSU,STA	0.6		µs	
Data in Hold time	tHD,DAT	0		µs	
Data in Set-Up time	tSU,DAT	0.1		µs	
Input Rise time (100 kHz)	tR,100		1000	ns	Note 1
Input Rise time (400 kHz)	tR,400		300	ns	Note 1
Input Fall time (100 kHz)	tF,100		300	ns	Note 1
Input Fall time (400 kHz)	tF,400		300	ns	Note 1
STOP Set-Up time	tSU,STO	0.6		µs	
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Maximum time the SFP+ may hold the SCL line low before continuing R or W operation
Complete Single or Sequential Write	tWR		40	ms	Complete (up to) 8 Byte Write
Endurance (Write Cycles)		10 k		Cycles	@ Max Operating Temperature
Physical Interface					
SCL and SDA	VOL	0.0	0.40	V	Rpullup[2] pulled to Host_VCC. IOL(max) = 3mA
	VOH	VCC – 0.5	VCC + 0.3	V	Rpullup[2] pulled to Host_VCC.
	VIL	-0.3	VCCT * 0.3	V	
	VIH	VCCT * 0.7	VCCT + 0.5	V	
Input Current on SCL and SDA pins	IL	-10	10	µA	
Capacitance on SCL and SDA pins	Ci[2]		14	pF	
Total bus capacitance for SCL and SDA	Cb[3]		100	pF	At 400 kHz, Rp (max) = 3.0 kΩ At 100 kHz, Rp (max) = 8.0 kΩ
			290	pF	At 400 kHz, Rp (max) = 1.1 kΩ At 100 kHz, Rp (max) = 2.75 kΩ

Notes:

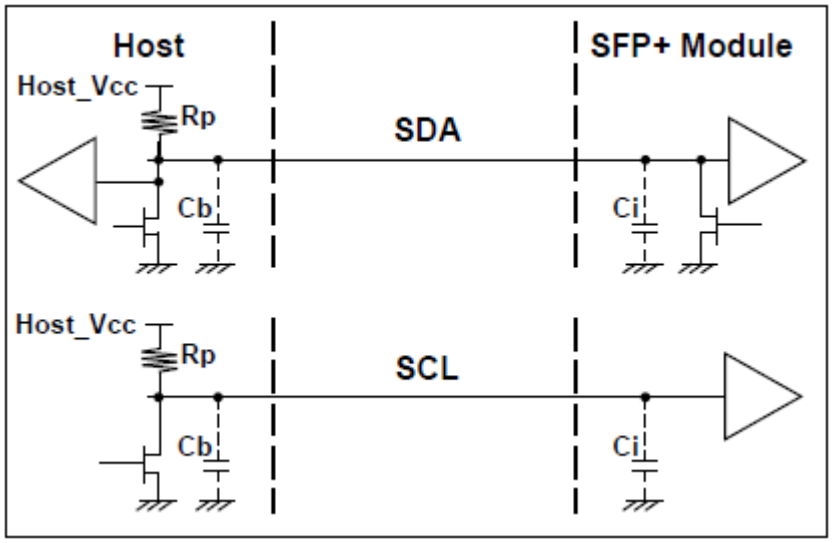
1. From (VIL, MAX -0.15) to (VIH, MIN +0.15)
2. Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measured at the Host side of the connector. VccT/R + 0.5 V nor requires the module to sink more than 3.0mA current

3. Ci is the capacitance looking into the module SCL and SDA pins.
4. Cb is the total bus capacitance on the SCL or SDA bus.

SFP+ Timing Diagram



Physical Interface



SFP+ Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions
Tx_Disable assert time	t_off		100	µs	Rising edge of TX_Disable to fall of output signal below 10% of nominal.
TX_Disable negate time	T_on		2	ms	Falling edge of TX Disable to rise output sognal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_ cooled		90	sec	From power supplies meeting or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level II part during fault recovery is fully operational. Also, from stop bit-low-to-high SDA transition enabling Power Level II until cooled module is fully operational.
Tx_Fault assert for cooled module	Tx_fault_on_ cooled		1	ms	From occurrence of fault to assertion of TX_Fault
Tx_Fault Reset	t_reset	10		µs	Time TX_disable must be held high to reset TX_Fault
RX_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of RX_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of RX_LOS.
Maximum Current Ramp on Power Supply					
Icc instantaneous peak current			800	mA	Note 1,2
Icc sustained peak current			660	mA	Note 1,2

Notes:

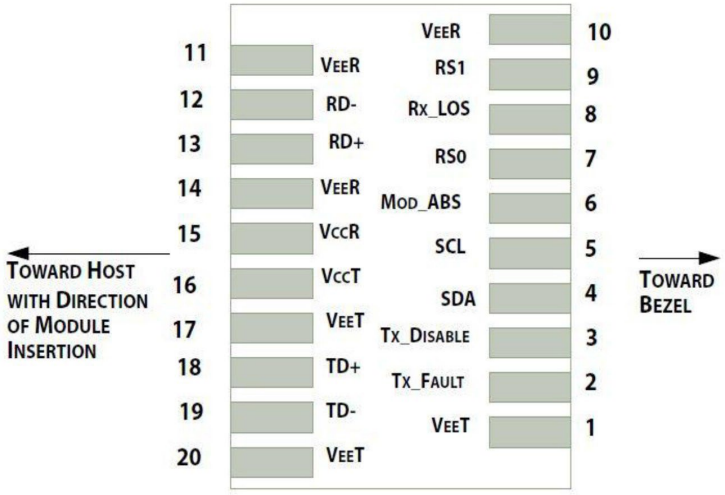
1. The maximum currents are the allowed currents for each power supply VccT or VccR, therefore the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed to specified maximum current capacity of the connector contact for a short period.
2. Not to exceed the sustained peak limit for the more than 50 µs; may exceed this limit for shorter durations.

Pin Descriptions

Pin	Logic	Symbol	Power Sequence Order	Name/Descriptions	Ref.
1		VeeT	1	Module Transmitter Ground.	1
2	LVTTL-O	TX_Fault	3	Module Transmitter Fault.	2
3	LVTTL-I	TX_Disable	3	Transmitter Disable; Turn off laser output.	3
4	LVTTL-I/O	SDA	3	2-Wire Serial Interface Data Line.	
5	LVTTL-I/O	SCL	3	2-Wire Serial Interface Clock.	
6		Mod_Abs	3	Module Absent, connected to VeeT or VeeR in the module.	4
7	LVTTL-I	RS0	3	N/A. 30kΩ pull down inside the module.	
8	LVTTL-O	RX_LOS	3	Receiver Loss of Signal Indicator.	2
9	LVTTL-I	RS1	3	N/A. 30kΩ pull down inside the module.	
10		VeeR	1	Module Receiver Ground.	1
11		VeeR	1	Module Receiver Ground.	1
12	CML-O	RD-	3	Receiver Inverted Data Output(SFI).	
13	CML-O	RD+	3	Receiver Non-Inverted Data Output(SFI).	
14		VeeR	1	Module Receiver Ground.	1
15		VccR	2	Module Receiver 3.3V Supply.	5
16		VccT	2	Module Transmitter 3.3V Supply.	5
17		VeeT	1	Module Transmitter Ground.	1
18	CML-I	TD+	3	Transmitter Non-Inverted Data Output(SFI).	
19	CML-I	TD-	3	Transmitter Inverted Data Output(SFI).	
20		VeeT	1	Module Transmitter Ground.	1

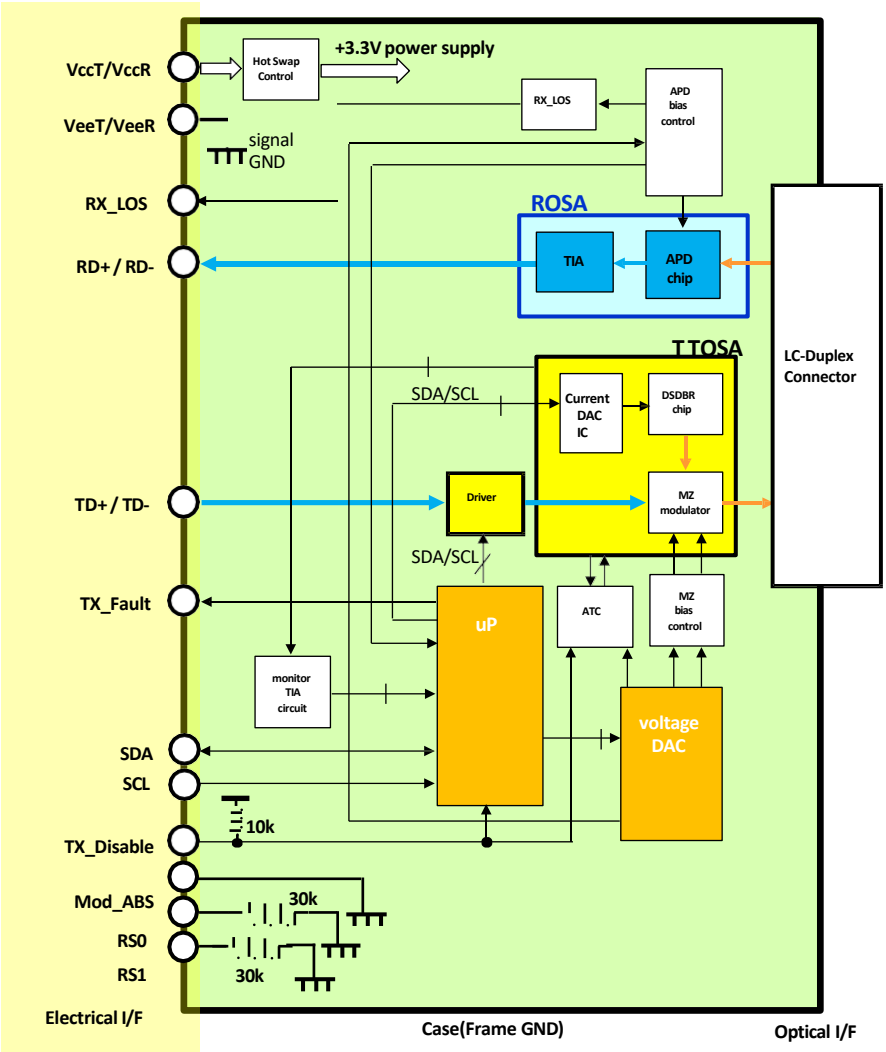
Notes:

1. The module signal ground pins, VeeR and Veet, are isolated from the module case.
2. This pin is an open drain output piN and shall be pulled up with a 4.7k-10kΩ to Host_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5V.
3. This pin is an input pin with 10kohms pull up to VccT in the module.
4. This pin shall be pulled up with 4.7k-10kohhms to Host_Vcc on the host board.
5. Vcct and VccR are tied together inside the module.



Pin-out of connector Block on Host board

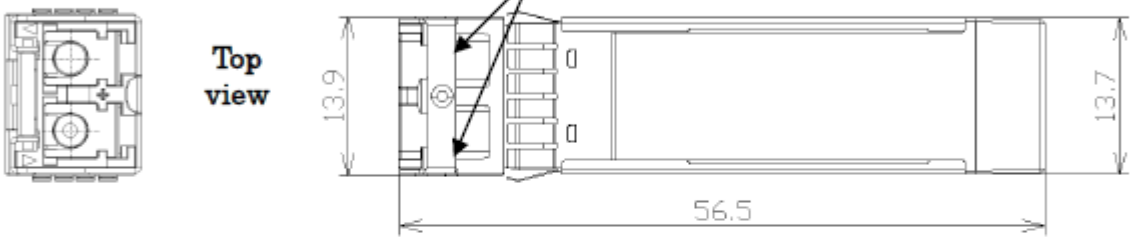
Recommended Circuit Schematic



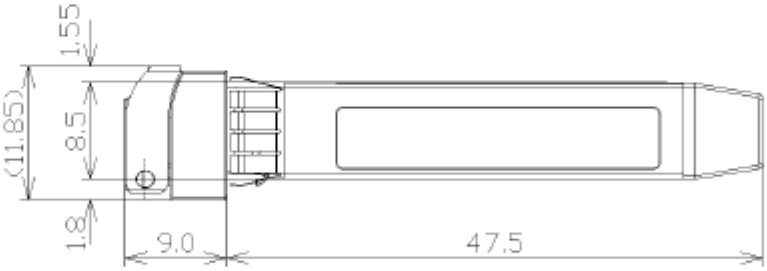
Mechanical Specifications

Side view

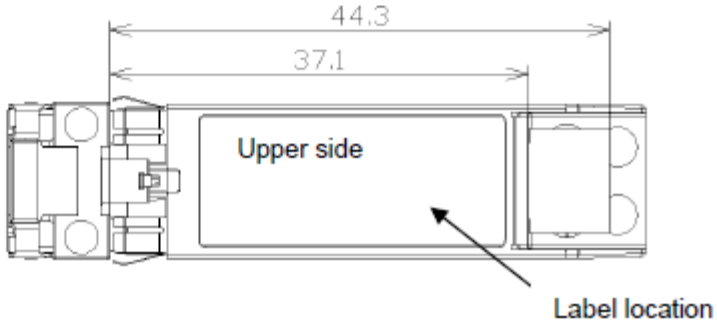
Top view



Side view



Bottom view



OptioConnect
Innovation for the Future of High-Speed Networking

Who We Are
OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do
At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design
Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team
Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

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To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect
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