

### QDD-400G-ZRP-S-OPC

Cisco® QDD-400G-ZRP-S Compatible TAA 400GBase-ZR+ QSFP-DD Transceiver (SMF, Coherent, LC, DOM, OpenZR+)

#### **Features**

- Hot pluggable QSFP-DD footprint (Type 2A)
- Tunable C-band Transmitter
- Coherent Receivers
- Duplex LC connector
- Supports 400/300/200/100Gbps Payload
- Operating Temperature -5 to 80 Celsius
- O-FEC (15%) with 11.6dB Net Coding Gain
- 8x 26.5625GBd PAM4 Serial Electrical Interface
- 4x 25.78125GBd NRZ Serial Electrical Interface
- 2x 26.5625GBd PAM4 Serial Electrical Interface
- RoHS Compliant and Lead-Free



## **Applications:**

- 400GBase Ethernet
- Access and Enterprise

## **Product Description**

This Cisco® QDD-400G-ZRP-S compatible QSFP-DD transceiver provides 400GBase-ZR Open ZR+ throughput over Single-mode fiber (SMF) using a coherent wavelength and using an LC connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

# **Absolute Maximum Ratings**

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Storage Temperature	Ts	-40		85	°C	
Case Operating Temperature	Тор	-5		80	°C	
Relative Humidity (non-condensing)	RH			85	%	
Optical Receiver Overload				1	dBm	1
Line Baud Rate			60.13855		GBd	2, 3, 4
Line Baud Rate			30.06927		GBd	5

# Notes:

- 1. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used
- 2. ZR400-OFEC-16QAM
- 3. ZR300-OFEC-8QAM
- 4. ZR200-OFEC-QPSK
- 5. ZR100-OFEC-QPSK

# **Electrical Characteristics**

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Supply Current	Icc			6	Α	
Power Consumption	PD		18.4	21.3	W	
Power Consumption	PD			1.5	W	1

## Notes:

1. Low power mode

# **Optical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Transmitter						
Average Output Power	Ро	-10	-8.5	-6	dBm	1, 2
Laser Linewidth				300	kHz	
Transmitter VOA Dynamic Range		10			dB	3
Output Power Stability		-1		1	dB	
In-Band OSNR		40			dB/0.1nm	
Out-of-Band OSNR		35			dB/0.1nm	
Frequency Range		191.275		196.125	THz	4
Centre Frequency		ν <sub>T</sub> -1.5	V <sub>T</sub>	ν <sub>T</sub> +1.5	GHz	5
Channel Spacing		6.25			GHz	
Centre Wavelength Range	Τλ	1528.58		1567.34	nm	
Centre Wavelength	Τλ	λΤ -15	λΤ	λΤ +15	pm	
Receiver						
Receiver Operating Wavelength	Rλ	1528.58		1567.34	nm	
Receiver Sensitivity	S			-23	dBm	6, 7
	S			-30	dBm	8
	S			-32	dBm	9
Receiver Overload	P <sub>OL</sub>	1			dBm	10
Receiver Input Power Range		-12		1	dBm	11, 12
		-15		1	dBm	11, 13
		-17		1	dBm	11, 14
		-20		1	dBm	11, 15
Extended Receiver Input Power Range		-15		1	dBm	16
Acquisition Range		-3.6		3.6	GHz	17
Upstream Tx Linewidth				500	kHz	
OSNR Tolerance			21.7	22.7	dB	12
			18.3	19.3	dB	13
			14	15	dB	14
			10.5	11	dB	15
Crosstalk Tolerance				7	dB	18
Chromatic Dispersion Tolerance				26000	ps/nm	12, 19
				50000	ps/nm	13, 14, 19
				80000	ps/nm	15, 19

#### Notes:

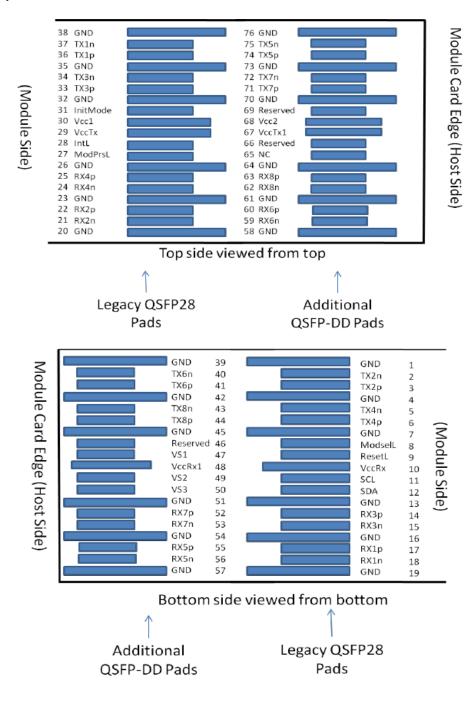
- 1. Output power coupled into a 9/125 μm single mode fibre
- 2. The output power is settable in steps of 0.1 dB within the specified wavelength range
- 3. With Tx VOA attenuation set to minimum
- 4. Per ITU-T G.694.1 DWDM grid definition
- 5. Applies also to LO
- 6. Minimum input power needed to achieve post-FEC BER ≤10-15, ZR400-OFEC-16QAM, OSNR>35dB
- 7. Minimum input power needed to achieve post-FEC BER ≤10-15, ZR300-OFEC-8QAM, OSNR>35dB
- 8. Minimum input power needed to achieve post-FEC BER ≤10-15, ZR200-OFEC-QPSK, OSNR>35dB
- 9. Minimum input power needed to achieve post-FEC BER ≤10-15, ZR100-OFEC-QPSK, OSNR>35dB
- 10. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used
- 11. An input power in this range guarantees optimum OSNR performance
- 12. ZR400-OFEC-16QAM
- 13. ZR300-OFEC-8QAM
- 14. ZR200-OFEC-QPSK
- 15. ZR100-OFEC-QPSK
- 16. With ≤1dB OSNR tolerance degradation
- 17. Frequency offset between received carrier and LO
- 18. Ratio of accumulated crosstalk channels to signal power
- 19. Less than 0.5dB receiver sensitivity penalty compared to OSNR>35dB

# **Pin Descriptions**

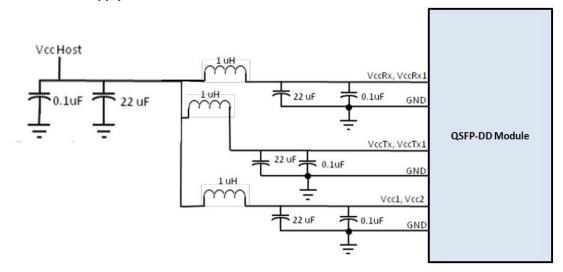
CML-I		escriptions			
Transmitter Inverted Data Input   38	Pin	Logic	Symbol	Name/Descriptions	Plug Sequence
3         CML-I         Tx2p         Transmitter Non-Inverted Data Input         38           4         GND         Ground         18           5         CML-I         Tx4p         Transmitter Inverted Data Input         38           6         CML-I         Tx4p         Transmitter Non-Inverted Data Input         38           7         GND         GRD         Ground         18           8         LVTTL-I         Module Select         38           9         LVTTL-I         Resett         Module Reset         38           10         VCcRX         +3.3V Power Supply Receiver         28           11         LVCMOS-I/O         SCL         2-wire serial interface clock         38           12         LVCMOS-I/O         SDA         2-wire serial interface data         38           12         LVCMOS-I/O         SDA         Receiver Non-Inverted Data Output         38           15         CML-	1		GND	Ground	1B
4         GND         Ground         18           5         CML-I         Tx4n         Transmitter Inverted Data Input         38           6         CML-I         Tx4p         Transmitter Non-Inverted Data Input         38           7         GND         Ground         18           8         LVTIL-I         ModSelL         Module Select         38           9         LVTIL-I         Resett.         Module Reset         38           10         VccRx         +3.3V Power Supply Receiver         28           11         LVCMOS-I/O         SCL         2-wire serial interface dock         38           12         LVCMOS-I/O         SCD         2-wire serial interface dota         38           13         GND         GROD         Ground         18           14         CML-O         Rx3p         Receiver Non-Inverted Data Output         38           15         CML-O         Rx3p         Receiver Non-Inverted Data Output         38           16         GND         Ground         18           17         CML-O         Rx1p         Receiver Non-Inverted Data Output         38           18         CML-O         Rx2n         Receiver Inverted Data Output	2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
5         CML-I         Tx4n         Transmitter Inverted Data Input         38           6         CML-I         Tx4p         Transmitter Non-Inverted Data Input         38           7         GND         Ground         18           8         LVTIL-I         ModSelL         Module Select         38           9         LVTTL-I         ResetL         Module Select         38           10         VccRx         +3.3V Power Supply Receiver         28           11         LVCMOS-I/O         SCL         2-wire serial interface clock         38           12         LVCMOS-I/O         SDA         2-wire serial interface data         38           13         GND         Ground         18           14         CML-O         Rx3p         Receiver Non-Inverted Data Output         38           15         CML-O         Rx3p         Receiver Inverted Data Output         38           16         GND         Ground         18           17         CML-O         Rx1p         Receiver Inverted Data Output         38           18         CML-O         Rx2n         Receiver Inverted Data Output         38           20         GND         Ground         18	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
6         CML-I         Tx4p         Transmitter Non-Inverted Data Input         38           7         GND         Ground         18           8         LVTIL-I         ModSelL         Module Select         38           9         LVTIL-I         ResetL         Module Select         38           10         VCKDX         +3.3V Power Supply Receiver         28           11         LVCMOS-I/O         SCL         2-wire serial interface clock         38           12         LVCMOS-I/O         SDA         2-wire serial interface data         38           13         LVCMOS-I/O         SDA         2-wire serial interface data         38           14         CML-O         Rx3p         Receiver Non-Inverted Data Output         38           15         CML-O         Rx3p         Receiver Inverted Data Output         38           16         GND         Ground         18           17         CML-O         Rx1n         Receiver Inverted Data Output         38           18         CML-O         Rx1n         Receiver Inverted Data Output         38           20         GND         Ground         18           21         CML-O         Rx2p         Receiver Inverte	4		GND	Ground	1B
The color of the	5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
8         LVTTL-I         ModSelL         Module Select         38           9         LVTTL-I         ResetL         Module Reset         38           10         VccRx         +3.3V Power Supply Receiver         28           11         LVCMOS-I/O         SCL         2-wire serial interface dock         3B           12         LVCMOS-I/O         SDA         2-wire serial interface dock         3B           13         GND         Ground         1B           14         CML-O         Rx3p         Receiver Non-Inverted Data Output         3B           15         CML-O         Rx3n         Receiver Inverted Data Output         3B           16         GND         Ground         1B         1B           17         CML-O         Rx1n         Receiver Inverted Data Output         3B           18         CML-O         Rx1n         Receiver Inverted Data Output         3B           20         GND         Ground         1B           21         CML-O         Rx2n         Receiver Inverted Data Output         3B           22         CML-O         Rx4p         Receiver Non-Inverted Data Output         3B           23         GND         Ground         1	6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
1	7		GND	Ground	1B
10	8	LVTTL-I	ModSelL	Module Select	3B
11         LVCMOS-I/O         SCL         2-wire serial interface clock         38           12         LVCMOS-I/O         SDA         2-wire serial interface data         38           13         GND         Ground         18           14         CML-O         Rx3p         Receiver Non-Inverted Data Output         38           15         CML-O         Rx3n         Receiver Inverted Data Output         38           16         GND         Ground         18           17         CML-O         Rx1p         Receiver Inverted Data Output         38           18         CML-O         Rx1n         Receiver Inverted Data Output         38           19         GND         Ground         18           20         GND         Ground         18           21         CML-O         Rx2n         Receiver Inverted Data Output         38           22         CML-O         Rx2p         Receiver Inverted Data Output         38           23         GND         Ground         18           24         CML-O         Rx4p         Receiver Inverted Data Output         38           25         CML-O         Rx4p         Receiver Inverted Data Output         38	9	LVTTL-I	ResetL	Module Reset	3B
12         LVCMOS-I/O         SDA         2-wire serial interface data         38           13         GND         Ground         18           14         CML-O         Rx3p         Receiver Non-Inverted Data Output         38           15         CML-O         Rx3n         Receiver Inverted Data Output         38           16         GND         Ground         1B         38           17         CML-O         Rx1p         Receiver Non-Inverted Data Output         38           18         CML-O         Rx1n         Receiver Inverted Data Output         38           19         GND         Ground         1B           20         GND         Ground         1B           21         CML-O         Rx2n         Receiver Inverted Data Output         38           22         CML-O         Rx2p         Receiver Non-Inverted Data Output         38           23         GND         Ground         1B           24         CML-O         Rx4n         Receiver Inverted Data Output         38           25         CML-O         Rx4p         Receiver Inverted Data Output         38           26         GND         Ground         1B           27 <th>10</th> <th></th> <th>VccRx</th> <th>+3.3V Power Supply Receiver</th> <th>2B</th>	10		VccRx	+3.3V Power Supply Receiver	2B
13	11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
14         CMI-O         Rx3p         Receiver Non-Inverted Data Output         38           15         CMI-O         Rx3n         Receiver Inverted Data Output         38           16         GND         Ground         18           17         CML-O         Rx1p         Receiver Non-Inverted Data Output         38           18         CML-O         Rx1n         Receiver Inverted Data Output         38           19         GND         Ground         18           20         GND         Ground         18           21         CML-O         Rx2n         Receiver Inverted Data Output         38           22         CML-O         Rx2p         Receiver Inverted Data Output         38           23         GND         Ground         18           24         CML-O         Rx4n         Receiver Inverted Data Output         38           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         38           26         GND         Ground         18           27         LVTL-O         ModPrsL         Module Present         38           28         LVTL-O         Intl.         Interrupt         38           29	12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
15         CMI-O         Rx3n         Receiver Inverted Data Output         3B           16         GND         Ground         1B           17         CML-O         Rx1p         Receiver Non-Inverted Data Output         3B           18         CML-O         Rx1n         Receiver Inverted Data Output         3B           19         GND         Ground         1B           20         GND         Ground         1B           21         CML-O         Rx2n         Receiver Inverted Data Output         3B           22         CML-O         Rx2p         Receiver Non-Inverted Data Output         3B           23         GND         Ground         1B           24         CML-O         Rx4n         Receiver Non-Inverted Data Output         3B           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         3B           26         GND         Ground         1B           27         LVTTL-O         ModPrsL         Module Present         3B           28         LVTTL-O         Intl         Interrupt         3B           29         VccTx         +3.3V Power supply ransmitter         2B           30         Vcc1 <th>13</th> <th></th> <th>GND</th> <th>Ground</th> <th>1B</th>	13		GND	Ground	1B
16         GND         Ground         1B           17         CML-O         Rx1p         Receiver Non-Inverted Data Output         3B           18         CML-O         Rx1n         Receiver Inverted Data Output         3B           19         GND         Ground         1B           20         GND         Ground         1B           21         CML-O         Rx2n         Receiver Inverted Data Output         3B           22         CML-O         Rx2p         Receiver Non-Inverted Data Output         3B           23         GND         Ground         1B           24         CML-O         Rx4n         Receiver Inverted Data Output         3B           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         3B           26         GND         Ground         1B           27         LVTTL-O         ModPISL         Module Present         3B           28         LVTTL-O         IntL         Interrupt         2B           29         VccTx         +3.3V Power supply transmitter         2B           30         Vcc1         +3.3V Power supply transmitter         2B           31         LVTTL-I         Initial	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
17         CML-O         Rx1p         Receiver Non-Inverted Data Output         38           18         CML-O         Rx1n         Receiver Inverted Data Output         38           19         GND         Ground         18           20         GND         Ground         18           21         CML-O         Rx2n         Receiver Inverted Data Output         38           22         CML-O         Rx2p         Receiver Non-Inverted Data Output         38           23         GND         Ground         18           24         CML-O         Rx4n         Receiver Non-Inverted Data Output         38           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         38           26         GND         Ground         18           27         LVTIL-O         ModPrsL         Module Present         38           28         LVTIL-O         Intl         Interrupt         38           29         VccTx         +3.3V Power supply transmitter         28           30         Vcc1         +3.3V Power supply         28           31         LVTTL-I         InitiMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	15	CML-O	Rx3n	Receiver Inverted Data Output	3B
18         CML-O         Rx1n         Receiver Inverted Data Output         38           19         GND         Ground         18           20         GND         Ground         18           21         CML-O         Rx2n         Receiver Inverted Data Output         38           22         CML-O         Rx2p         Receiver Non-Inverted Data Output         38           23         GND         Ground         18           24         CML-O         Rx4n         Receiver Inverted Data Output         38           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         38           26         GND         Ground         18           27         LVTTL-O         ModPrsL         Module Present         38           28         LVTTL-O         Intl         Interrupt         38           29         VccTx         +3.3V Power supply transmitter         28           30         Vcc1         +3.3V Power supply         28           31         LVTTL-I         InitiMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE         38           32         GND         Ground         18           33	16	GND	Ground	1B	
19	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
20	18	CML-O	Rx1n	Receiver Inverted Data Output	3B
21         CML-O         Rx2n         Receiver Inverted Data Output         3B           22         CML-O         Rx2p         Receiver Non-Inverted Data Output         3B           23         GND         Ground         1B           24         CML-O         Rx4n         Receiver Inverted Data Output         3B           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         3B           26         GND         Ground         1B           27         LVTTL-O         ModPrsL         Module Present         3B           28         LVTTL-O         IntL         Interrupt         3B           29         VccTx         +3.3V Power supply transmitter         2B           30         Vcc1         +3.3V Power supply transmitter         2B           31         LVTTL-I         InitMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE         3B           32         GND         Ground         1B           33         CML-I         Tx3p         Transmitter Non-Inverted Data Input         3B           34         CML-I         Tx3n         Transmitter Inverted Data Input         3B           35         GND         Grou	19		GND	Ground	1B
22         CML-O         Rx2p         Receiver Non-Inverted Data Output         38           23         GND         Ground         18           24         CML-O         Rx4n         Receiver Inverted Data Output         38           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         38           26         GND         Ground         18           27         LVTTL-O         ModPrsL         Module Present         38           28         LVTTL-O         IntL         Interrupt         38           29         VccTx         +3.3V Power supply transmitter         28           30         Vcc1         +3.3V Power supply         28           31         LVTTL-I         InitMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE         38           32         GND         Ground         18           33         CML-I         Tx3p         Transmitter Non-Inverted Data Input         38           34         CML-I         Tx3n         Transmitter Non-Inverted Data Input         38           35         GND         Ground         18           36         CML-I         Tx1p         Transmitter Non-Inverted Data Input	20		GND	Ground	1B
CML-O	21	CML-O	Rx2n	Receiver Inverted Data Output	3B
24         CML-O         Rx4n         Receiver Inverted Data Output         38           25         CML-O         Rx4p         Receiver Non-Inverted Data Output         38           26         GND         Ground         18           27         LVTTL-O         ModPrsL         Module Present         38           28         LVTTL-O         IntL         Interrupt         38           29         VccTx         +3.3V Power supply transmitter         28           30         Vcc1         +3.3V Power supply         28           31         LVTTL-I         InitMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE           32         GND         Ground         18           33         CML-I         Tx3p         Transmitter Non-Inverted Data Input         38           34         CML-I         Tx3n         Transmitter Inverted Data Input         38           35         GND         Ground         18           36         CML-I         Tx1p         Transmitter Inverted Data Input         38           37         CML-I         Tx1n         Transmitter Inverted Data Input         38           38         GND         Ground         18	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
25         CML-O         Rx4p         Receiver Non-Inverted Data Output         3B           26         GND         Ground         1B           27         LVTTL-O         ModPrsL         Module Present         3B           28         LVTTL-O         IntL         Interrupt         3B           29         VccTx         +3.3V Power supply transmitter         2B           30         Vcc1         +3.3V Power supply         2B           31         LVTTL-I         InitMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE           32         GND         Ground         1B           33         CML-I         Tx3p         Transmitter Non-Inverted Data Input         3B           34         CML-I         Tx3n         Transmitter Inverted Data Input         3B           35         GND         Ground         1B           36         CML-I         Tx1p         Transmitter Non-Inverted Data Input         3B           37         CML-I         Tx1n         Transmitter Inverted Data Input         3B           38         GND         Ground         1B           39         GND         Ground         1A	23		GND	Ground	1B
26         GND         Ground         18           27         LVTTL-O         ModPrsL         Module Present         3B           28         LVTTL-O         IntL         Interrupt         3B           29         VccTx         +3.3V Power supply transmitter         2B           30         Vcc1         +3.3V Power supply         2B           31         LVTTL-I         InitMode         Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE         3B           32         GND         Ground         1B           33         CML-I         Tx3p         Transmitter Non-Inverted Data Input         3B           34         CML-I         Tx3n         Transmitter Inverted Data Input         3B           35         GND         Ground         1B           36         CML-I         Tx1p         Transmitter Non-Inverted Data Input         3B           37         CML-I         Tx1n         Transmitter Inverted Data Input         3B           38         GND         Ground         1B           39         GND         Ground         1A	24	CML-O	Rx4n	Receiver Inverted Data Output	3B
27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B35GNDGround1B36CML-ITx1pTransmitter Non-Inverted Data Input3B37CML-ITx1nTransmitter Inverted Data Input3B38GNDGround1B39GNDGround1A	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
28 LVTTL-O IntL Interrupt 3B  29 VccTx +3.3V Power supply transmitter 2B  30 Vcc1 +3.3V Power supply 2B  31 LVTTL-I InitMode Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE  32 GND Ground 1B  33 CML-I Tx3p Transmitter Non-Inverted Data Input 3B  34 CML-I Tx3n Transmitter Inverted Data Input 3B  35 GND Ground 1B  36 CML-I Tx1p Transmitter Non-Inverted Data Input 3B  37 CML-I Tx1n Transmitter Inverted Data Input 3B  38 GND Ground 1B  39 GND Ground 1B	26		GND	Ground	1B
29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B35GNDGround1B36CML-ITx1pTransmitter Non-Inverted Data Input3B37CML-ITx1nTransmitter Inverted Data Input3B38GNDGround1B39GNDGround1A	27	LVTTL-O	ModPrsL	Module Present	3B
30 Vcc1 +3.3V Power supply 2B  31 LVTTL-I InitMode Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE  32 GND Ground 1B  33 CML-I Tx3p Transmitter Non-Inverted Data Input 3B  34 CML-I Tx3n Transmitter Inverted Data Input 3B  35 GND Ground 1B  36 CML-I Tx1p Transmitter Non-Inverted Data Input 3B  37 CML-I Tx1n Transmitter Inverted Data Input 3B  38 GND Ground 1B  39 GND Ground 1B	28	LVTTL-O	IntL	Interrupt	3B
31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3832GNDGround1833CML-ITx3pTransmitter Non-Inverted Data Input3834CML-ITx3nTransmitter Inverted Data Input3835GNDGround1836CML-ITx1pTransmitter Non-Inverted Data Input3837CML-ITx1nTransmitter Inverted Data Input3838GNDGround1839GNDGround1A	29		VccTx	+3.3V Power supply transmitter	2B
32         GND         Ground         1B           33         CML-I         Tx3p         Transmitter Non-Inverted Data Input         3B           34         CML-I         Tx3n         Transmitter Inverted Data Input         3B           35         GND         Ground         1B           36         CML-I         Tx1p         Transmitter Non-Inverted Data Input         3B           37         CML-I         Tx1n         Transmitter Inverted Data Input         3B           38         GND         Ground         1B           39         GND         Ground         1A	30		Vcc1	+3.3V Power supply	2B
33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B35GNDGround1B36CML-ITx1pTransmitter Non-Inverted Data Input3B37CML-ITx1nTransmitter Inverted Data Input3B38GNDGround1B39GNDGround1A	31	LVTTL-I	InitMode		3B
34         CML-I         Tx3n         Transmitter Inverted Data Input         3B           35         GND         Ground         1B           36         CML-I         Tx1p         Transmitter Non-Inverted Data Input         3B           37         CML-I         Tx1n         Transmitter Inverted Data Input         3B           38         GND         Ground         1B           39         GND         Ground         1A	32		GND	Ground	1B
35         GND         Ground         1B           36         CML-I         Tx1p         Transmitter Non-Inverted Data Input         3B           37         CML-I         Tx1n         Transmitter Inverted Data Input         3B           38         GND         Ground         1B           39         GND         Ground         1A	33	CML-I	Тх3р	Transmitter Non-Inverted Data Input	3B
36     CML-I     Tx1p     Transmitter Non-Inverted Data Input     3B       37     CML-I     Tx1n     Transmitter Inverted Data Input     3B       38     GND     Ground     1B       39     GND     Ground     1A	34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
37         CML-I         Tx1n         Transmitter Inverted Data Input         3B           38         GND         Ground         1B           39         GND         Ground         1A	35		GND	Ground	1B
38         GND         Ground         1B           39         GND         Ground         1A	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
39 GND Ground 1A	37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
	38		GND	Ground	1B
40 CML-I Tx6n Transmitter Inverted Data Input 3A	39		GND	Ground	1A
	40	CML-I	Tx6n	Transmitter Inverted Data Input	3A

41	CML-I	Тх6р	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Тх8р	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
67		GND	Ground	1A
68		NC	No Connect	3A
69		Reserved	For future use	3A
70		VccTx1	3.3V Power Supply	2A
71		Vcc2	3.3V Power Supply	2A
72		Reserved	For Future Use	3A
73		GND	Ground	1A
74	CML-I	Тх7р	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx7n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

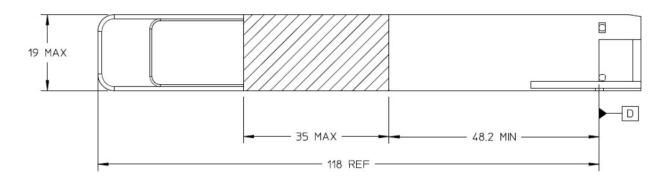
# **Electrical Pad Layout**



# **Recommended Power Supply Filter**



# **Mechanical Specifications**





## **OptioConnect**

# Innovation for the Future of High-Speed Networking

#### Who We Are

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

### What We Do

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our Al-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

### **Smarter Networks by Design**

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

### **Our Team**

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

### **Our Mission**

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

### **Let's Connect**

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward. <a href="https://www.optioconnect.com">www.optioconnect.com</a> | info@optioconnect.com







