S56DD100G-LR-AO

Dell® S56DD100G-LR Compatible TAA 100GBase-LR1 SFP-DD Transceiver (SMF, 1310nm, 10km, LC, DOM, MIS 2.0)

Features

- IEEE 100GBASE-LR Compliant
- SFP-DD MSA compliant
- 100GAUI-2 compliant 2x 26.5625Gbaud
- Single mode Fiber
- Operating Temperature: 0 to 70 Celsius
- Duplex LC Connector
- SFP-DD MIS Management Interface (MIS 2.0)
- Hot Pluggable
- RoHS Compliant and Lead Free
- Excellent ESD Protection

Applications

- 100GBase Ethernet

Product Description

This Dell® S56DD100G-LR compatible SFP-DD transceiver provides 100GBase-LR1 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Dell®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	0		+3.6	V	
Storage Ambient Temperature	Ts	-40		85	°C	
Operating Case Temperature	Tc	0	25	70	°C	
Optical Receiver Input				+5.5	dBm	Average

Notes:

1. Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Electrical Characteristics

Parameter	Symbol/ Test Point	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR			66	mV	10 Hz –10 MHz
Power Consumption	PD		3.0	3.5	W	
Supply Current	Icc			1116.4	mA	Steady state
Transmitter (per lane)						
Signaling Rate Per Lane (Range)	TP4	-100ppm	26.5625	+100ppn	GBd	1
AC Common-Mode Output Voltage (RMS)	TP4			17.5	mV	1
Differential Peak-to-Peak Output Voltage	TP4			900	mV	1
Near-End ESMW (Eye Symmetry Mask Width)	TP4	0.265			UI	1
Near-End Eye Height, Differential	TP4	70			mV	1
Far-End ESMW (Eye Symmetry Mask Width)	TP4	0.2			UI	1
Far-End Eye Height, Differential	TP4	30			mV	1
Far-End Pre-Cursor ISI Ratio	TP4	-4.5		2.5	%	1
Differential Output Return Loss	TP4	Equation (83E-2)			dB	1, 2
Common to Differential Mode Conversion Return Loss	TP4	Equation (83E-3)			dB	1, 2
Differential Termination Mismatch	TP4			10	%	1
Transition Time (20% to 80%)	TP4	9.5			ps	1
DC Common Mode Voltage	TP4	-350		2850	mV	1
Receiver (per lane, at TP1)						
Signaling Rate Per Lane (Range)	TP1	-100ppm	26.5625	+100ppm	GBd	

Differential Pk-Pk Input Voltage Tolerance	TP1a	900			mV	
Differential Input Return Loss	TP1	Equation (83E-5)			dB	2
Differential to Common Mode Input Return Loss	TP1	Equation (83E-6)			dB	2
Differential Termination Mismatch	TP1			10	%	
ESMW (Eye Symmetry Mask Width)	TP1a	0.22			UI	
Eye Width	TP1a	0.22			UI	
Eye Height	TP1a	32			mV	
Single-Ended Input Voltage Tolerance Range	TP1a	-0.4		3.3	V	
DC Common Mode Voltage	TP1	-350		2850	mV	

Notes:

1. Electrical module output is squelched for loss of optical input signal.
2. IEEE 802.3-2018 Section 6.

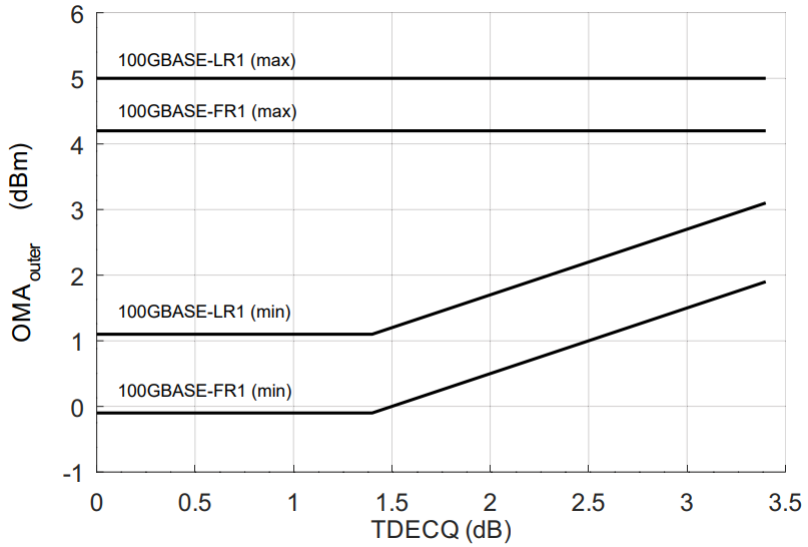
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
PAM4 Signaling Rate (Range)		53.125 ± 100 ppm			GBd	
Lane Wavelengths (Range)	λ	1304.5 – 1317.5			nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power	Aop	-1.9		4.8	dBm	1
Average Launch Power-OFF	POFF			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Outer Optical Modulation Amplitude (OMAouter)	OMA			5	dBm	
Outer Optical Modulation Amplitude (OMAouter) for TDECQ <1.4 dB		1.1			dBm	
Outer Optical Modulation Amplitude (OMAouter) for 1.4 dB ≤TDECQ ≤3.4 dB		- 0.3 + TDECQ			dBm	
Transmitter and Dispersion Penalty Eye Closure for PAM4	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ)				3.4	dB	
TDECQ – TECQ				2.5	dB	
Over/Under-Shoot				22	%	
Transmitter Power Excursion				2.8	dBm	
Optical Return Loss Tolerance	ORLT			15.6	dB	
Transmitter Reflectance				-26	dB	2
Transmitter Transition Time				17	ps	

$RIN_{15.5}$ OMA				-136	dB/Hz	
Receiver						
PAM4 Signaling Rate (Range)		53.125 ± 100 ppm			GBd	
Lane Wavelengths (Range)	λ	1304.5 – 1317.5			nm	
Damage Threshold	Pdamage	5.8			dBm	3
Average Receive Power	RxAVG	-8.2		4.8	dBm	4
Receive Power (OMAouter)	RxOMA			5	dBm	
Receiver Reflectance				-26	dB	
Receiver Sensitivity (OMAouter)	SenOMA			−6.1, TECQ-7.5	dBm	5
Stressed Receiver Sensitivity (OMAouter)	SenOMA			-4.1	dBm	6
Conditions of Stressed Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ)		3.4			dB	

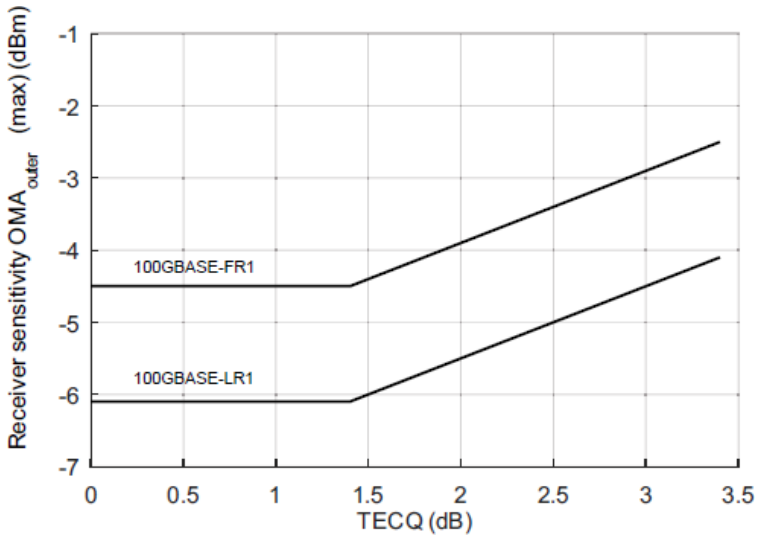
Notes:

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. OMA Outer:



6. Measured with conformance test signal at TP3 (see 100G Lambda MSA 100G-FR - “Technical Specification, Rev. 2.0 clause 3.11) for the BER specified in IEEE Std 802.3cd clause 140.1.1.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

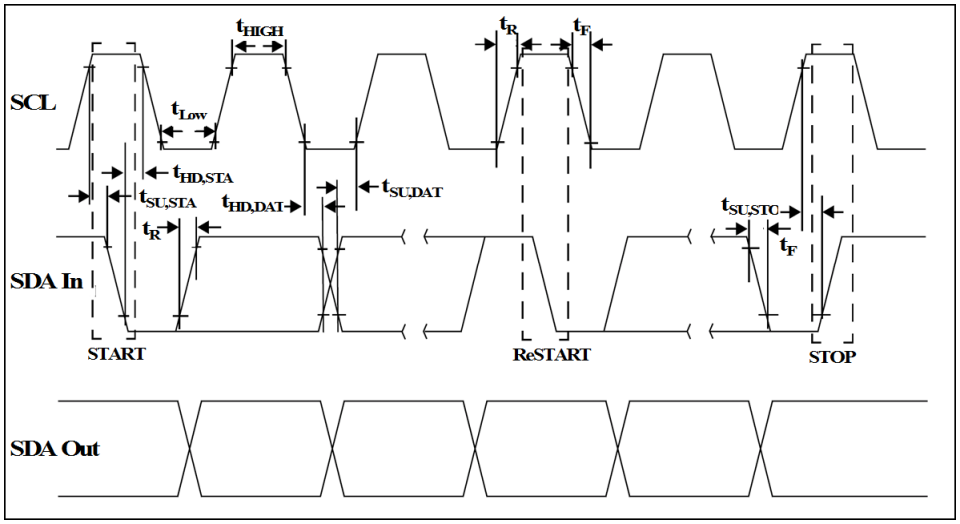
Receiver Sensitivity



RX_LOS Alarm Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Receiver Loss of Signal Indicator Assert Level	RX_LOS	-15		-8.5	dBm	Average power
Receiver Loss of Signal Indicator De-assert Level	RX_LOS			-8	dBm	Average power
Hysteresis	RX_LOS	0.5			dB	

2-Wire Interface Timing Diagram



Control and Status Timing Requirements

Parameters	Symbol	Min	Max	Units	Conditions
MgmtInit Duration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes.

Notes:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in the Electrical Specifications table.
2. Measured from the rising edge of SDA in the stop bit of the read transaction.
3. Measured from the rising edge of SDA in the stop bit of the write transaction.
4. Rx LOS condition is defined at the optical input by the relevant standard.

I/O Timing for Squelch & Disable

Parameters	Symbol	Max	Units	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached.
Tx Squelch De-assert Time	toff_Txsq	5 (Tentative)	s	Tx squelch deassert is system and implementation dependent.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence1 until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal and see notes 2 and 3.
Tx Disable De-assert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal and see note 2.
Tx Disable De-assert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see note 3.

Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal.
Rx Output Disable De-assert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable De-assert Time	toff_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Notes:

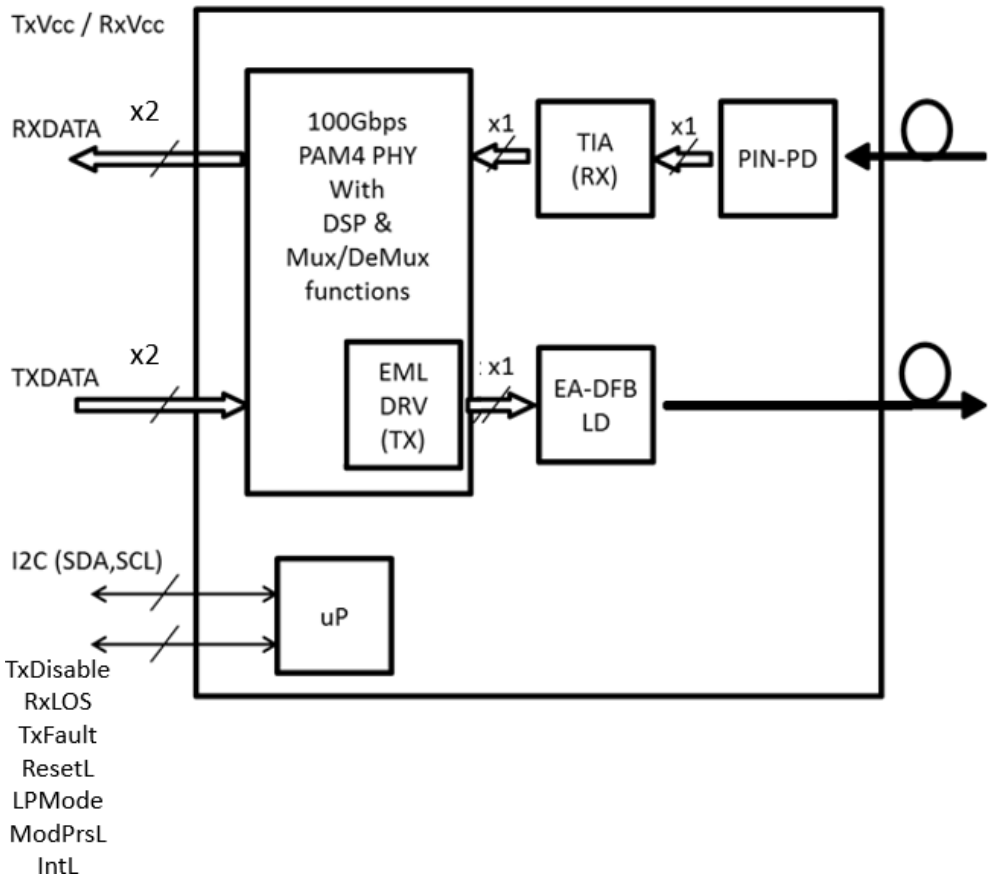
1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
2. CMIS 4.0 and beyond the listed values are superseded by the advertised. DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.
3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn _MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

Maximum Power Classes

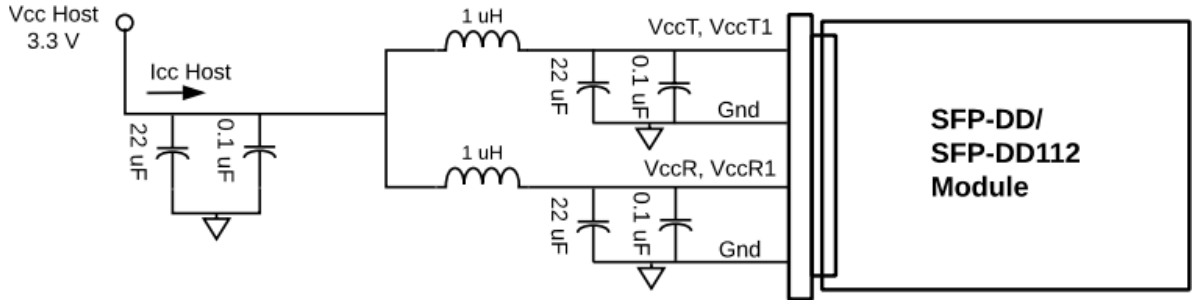
SFP56-DD modules are categorized into several power classes as listed in the table below. The power class of this module is class 4.

Power Class	Maximum power dissipation per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0

Functional Block Diagram



Recommended Host Board Power Supply Filtering Network



Pin Descriptions

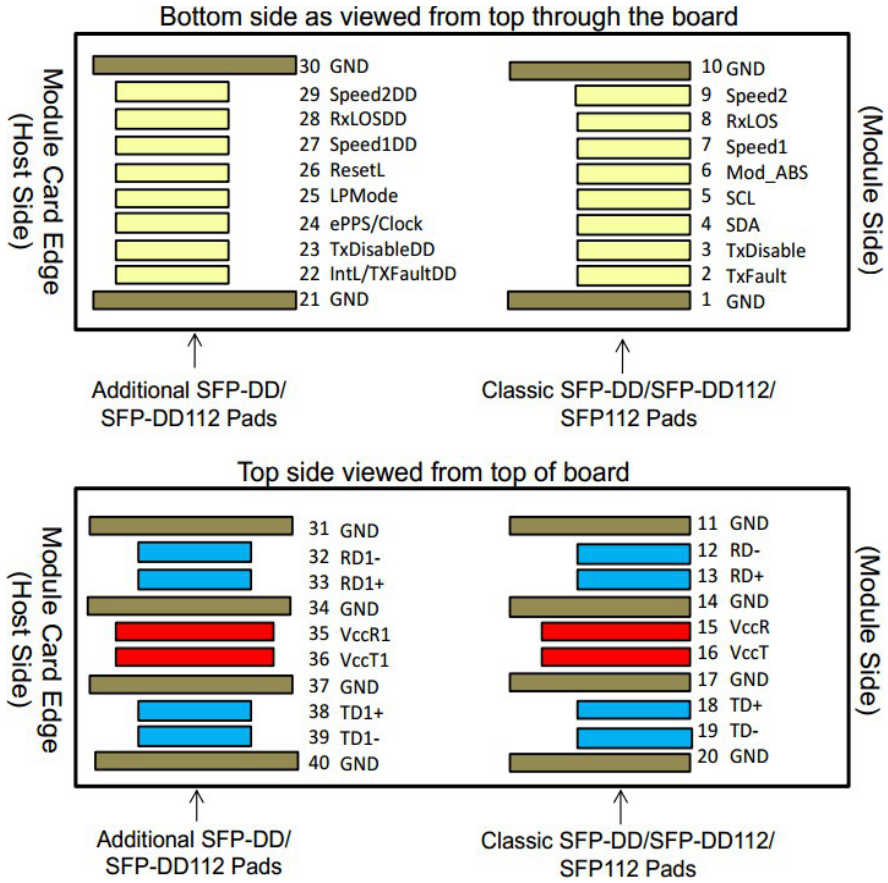
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground.	1
2	LVTTL-O	TX_Fault	Module Fault Indication: optionally configured as classic SFP Module Fault Indication via TWI as described in the SFP-DD MIS.	
3	LVTTL-I	Tx_Disable	Transmitter Disable for classic SFP channel.	
4	LVCMOS-I/O	SDA	Management I/F data line.	
5	LVCMOS-I/O	SCL	Management I/F clock.	
6	LVTTL-O	MOD_ABS	Module Absent.	
7	LVTTL-I	Speed1	Rx Rate Select for classic SFP channel.	
8	LVTTL-O	RxLOS	Rx Loss of Signal for classic SFP channel.	
9	LVTTL-I	Speed1	Tx Rate Select for classic SFP channel.	
10		GND	Ground.	1
11		GND	Ground.	1
12	CML-O	RD0-	Inverse Received Data Out for classic SFP+ channel.	
13	CML-O	RD0+	Received Data Out for classic SFP+ channel.	
14		GND	Ground.	1
15		VccR	Receive Power.	2
16		VccT	Transmitter Power.	2
17		GND	Ground.	1
18	CML-I	TD0+	Transmit Data In for classic SFP channel.	
19	CML-I	TD0-	Inverse Transmit Data In for classic SFP channel.	
20		GND	Ground.	1
21		GND	Ground.	1
22	LVTTL-O	IntL/TXFaultDD	Interrupt: optionally configured as TXFaultDD via TWI as described in the SFP-DD MIS.	
23	LVTTL-I	TxDisableDD	Transmitter Disable for DD channel.	
24	LVTTL-I	ePPS/Clock	Precision Time Protocol (PTP) reference clock input.	3
25	LVTTL-I	LPMode	Low Power Mode Control.	
26	LVTTL-I	ResetL	Module Reset.	
27	LVTTL-I	Speed1DD	Rx Rate Select for DD channel.	
28	LVTTL-O	RxLOSDD	Loss of Signal for DD channel.	
29	LVTTL-I	Speed2DD	Tx Rate Select for DD channel.	
30		GND	Ground.	1
31		GND	Ground.	1
32	CML-O	RD1-	Inverse Received Data Out for DD channel.	
33	CML-O	RD1+	Received Data Out for DD channel.	
34		GND	Ground.	1
35		VccR1	Receiver Power for DD channel.	2
36		VccT1	Transmitter Power for DD channel.	2
37		GND	Ground.	1

38	CML-I	TD1+	Transmit Data In for DD channel.	
39	CML-I	TD2-	Inverse Transmit Data In for DD channel.	
40		GND	Ground.	1

Notes:

1. SFP-DD uses common ground (GND) for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccR, VccT shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in the Maximum Power Classes table above. VccR, VccT, VccR1, VccT1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. The ePPS pins (if not used) may be terminated with 50 Ω to the ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 0, 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional SFP-DD/SFP-DD112 pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

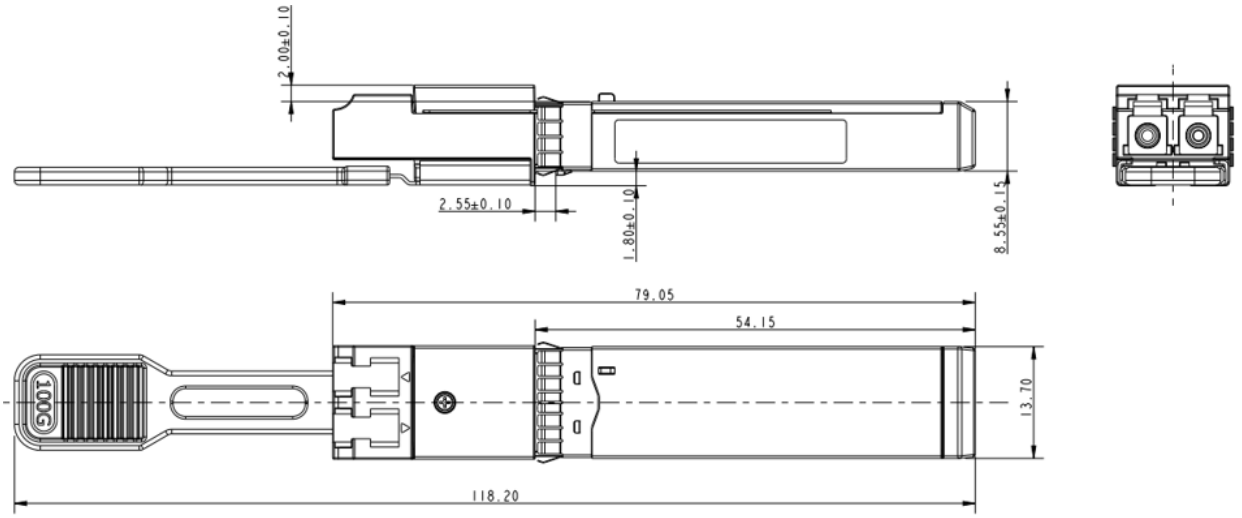
Electrical Pin-out Details

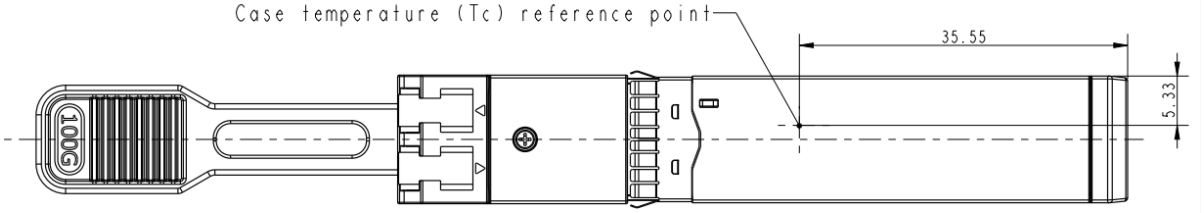


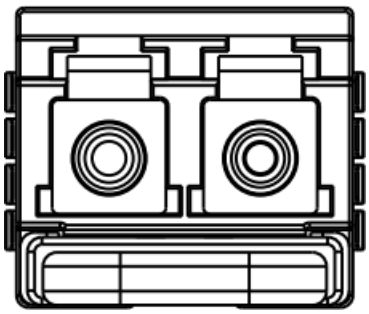
Mechanical Specifications

Unit: mm

Pull tab color: Blue







Looking into the connector, transmitter on the left.

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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