

DAC-Q56DD-2Q28-2M-AO

Dell® DAC-Q56DD-2Q28-2M Compatible TAA Compliant 200GBase-CU QSFP-DD 200G to 2xQSFP28 100G NRZ Direct Attach Cable (Passive Twinax, 2m)

Features:

- QSFP-DD MSA Compliant
- Transmission Data Rate Up to 25.78Gbps Per Channel
- SFF-8661 Compliant
- Built-In EEPROM Functions
- Operating Temperature: 0 to 70 Celsius
- Enables 200Gbps to 2x100Gbps Transmission
- RoHS Compliant and Lead-Free



Applications:

- 200GBase Ethernet

Product Description

This is a Dell® DAC-Q56DD-2Q28-2M compatible TAA compliant 200GBase-CU QSFP-DD 200G to 2xQSFP28 100G NRZ direct attach cable that operates over passive copper with a maximum reach of 2.0m (6.6ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Storage Temperature	Tstg	-40		85	°C
Operating Case Temperature	Tc	0		70	°C
Relative Humidity	RH	5		85	%
Data Rate			200		Gbps

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Length	L			2	M	
AWG			30		AWG	
Jacket Material		PVC, Black				

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Resistance	Rcon			3	Ω	
Insulation Resistance	Rins			10	MΩ	
Raw Cable Impedance	Zca	95	100	110	Ω	
Mated Connector Impedance	Zmated	85	100	115	Ω	
Insertion Loss @13.28GHz	SDD21	8		22.48	dB	
Return Loss	SDD11/22	$\text{Return_loss}(f) \geq \begin{cases} 16.5-2vf & 0.05 \leq f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{cases}$			dB	1
Differential to Common-Mode Return Loss	SCD11/22	$\text{Return_loss}(f) \geq \begin{cases} 22-(20/25.78)f & 0.01 \leq f < 12.89 \\ 15-(6/25.78)f & 12.89 \leq f \leq 19 \end{cases}$			dB	1
Differential to Common-Mode Conversion Loss	SCD21-SDD21	$\text{Conversion_loss}(f) - \text{IL}(f) \geq \begin{cases} 10 & 0.01 \leq f < 12.89 \\ 27-(29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{cases}$			dB	1
Minimum COM	COM	3			dB	

Notes:

1. For $0.05 \leq f \leq 19\text{GHz}$, where f is the frequency in GHz.

Pin Descriptions - QSFP-DD End

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input.	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input.	3B	
4		GND	Module Ground.	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input.	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input.	3B	
7		GND	Module Ground.	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Receiver Power Supply.	2B	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3B	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3B	
13		GND	Module Ground.	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output.	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output.	3B	
16		GND	Module Ground.	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output.	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output.	3B	
19		GND	Module Ground.	1B	1
20		GND	Module Ground.	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output.	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output.	3B	
23		GND	Module Ground.	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output.	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output.	3B	
26		GND	Module Ground.	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL/RxLOS	Interrupt. Optional RxLOS.	3B	
29		VccTx	+3.3V Transmitter Power Supply.	2B	2
30		Vcc1	+3.3V Power Supply.	2B	2
31	LVTTL-I	LPMode/TxDis	Low-Power Mode. Optional Tx Disable.	3B	
32		GND	Module Ground.	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input.	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input.	3B	
35		GND	Module Ground.	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input.	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input.	3B	
38		GND	Module Ground.	1B	1
39		GND	Module Ground.	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input.	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input.	3A	

42		GND	Module Ground.	1A	
43	CML-I	Tx8n	Transmitter Inverted Data Input.	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input.	3A	
45		GND	Module Ground.	1A	
46	LVC MOS/CML-I	P/VS4	Programmable. Module Vendor-Specific 4.	3A	5
47	LVC MOS/CML-I	P/VS1	Programmable. Module Vendor-Specific 1.	3A	5
48		VccRx1	+3.3V Receiver Power Supply.	2A	2
49	LVC MOS/CML-O	P/VS2	Programmable. Module Vendor-Specific 2.	3A	5
50	LVC MOS/CML-O	P/VS3	Programmable. Module Vendor-Specific 3.	3A	5
51		GND	Module Ground.	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output.	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output.	3A	
54		GND	Module Ground.	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output.	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output.	3A	
57		GND	Module Ground.	1A	1
58		GND	Module Ground.	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output.	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output.	3A	
61		GND	Module Ground.	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output.	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output.	3A	
64		GND	Module Ground.	1A	1
65		NC	Not Connected.	3A	3
66		Reserved	For Future Use.	3A	3
67		VccTx1	+3.3V Power Supply.	2A	2
68		Vcc2	+3.3V Power Supply.	2A	2
69	LVC MOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input.	3A	6
70		GND	Module Ground.	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input.	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input.	3A	
73		GND	Module Ground.	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input.	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input.	3A	
76		GND	Module Ground.	1A	1

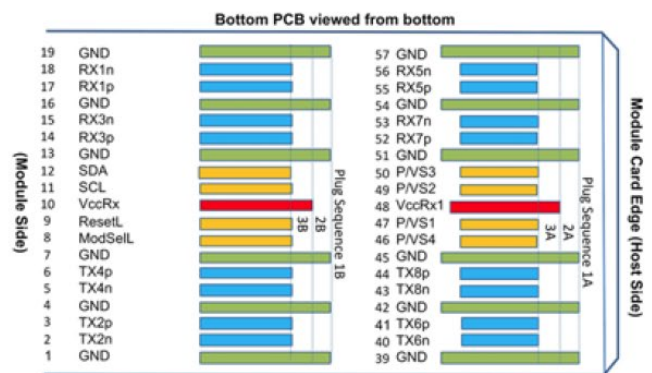
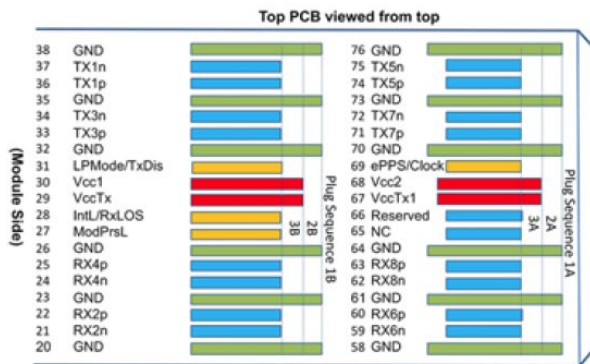
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane. Each connector GND contact is rated for maximum current of 500mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed below. For power classes 4 and above, the

module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500mA.

3. Reserved and No Connect pads recommended to be terminated with 10k Ω to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.
4. Plug sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.
5. Full definitions of P/VSx signals are currently under development. On new designs, not using P/VSx signals are recommended to be terminated on the host with 10k Ω .
6. ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.

Pin-Out Details - QSFP-DD End



Pin Descriptions - QSFP End

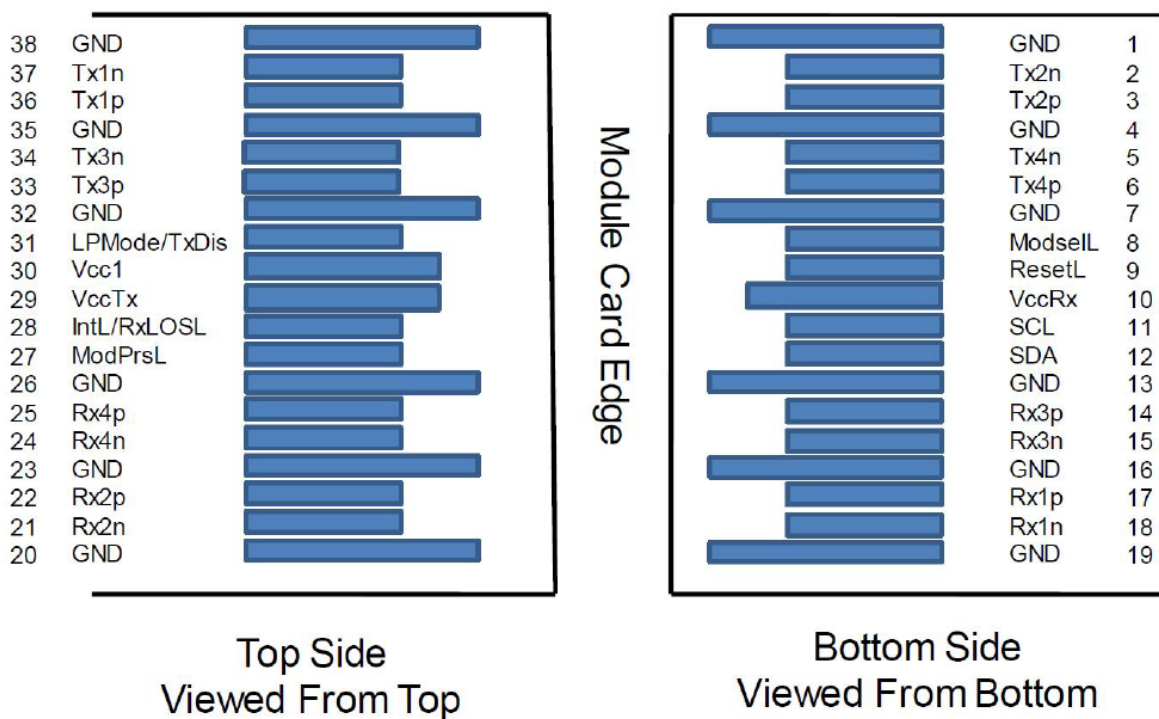
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Receiver Power Supply.	2	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3n	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1n	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output.	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output.	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1
27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL	Interrupt.	3	
29		VccTx	+3.3V Transmitter Power Supply.	2	2
30		Vcc1	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMODE	Low-Power Mode.	3	
32		GND	Module Ground.	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input.	3	

35		GND	Module Ground.	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1, and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Electrical Pin-Out Details - QSFP

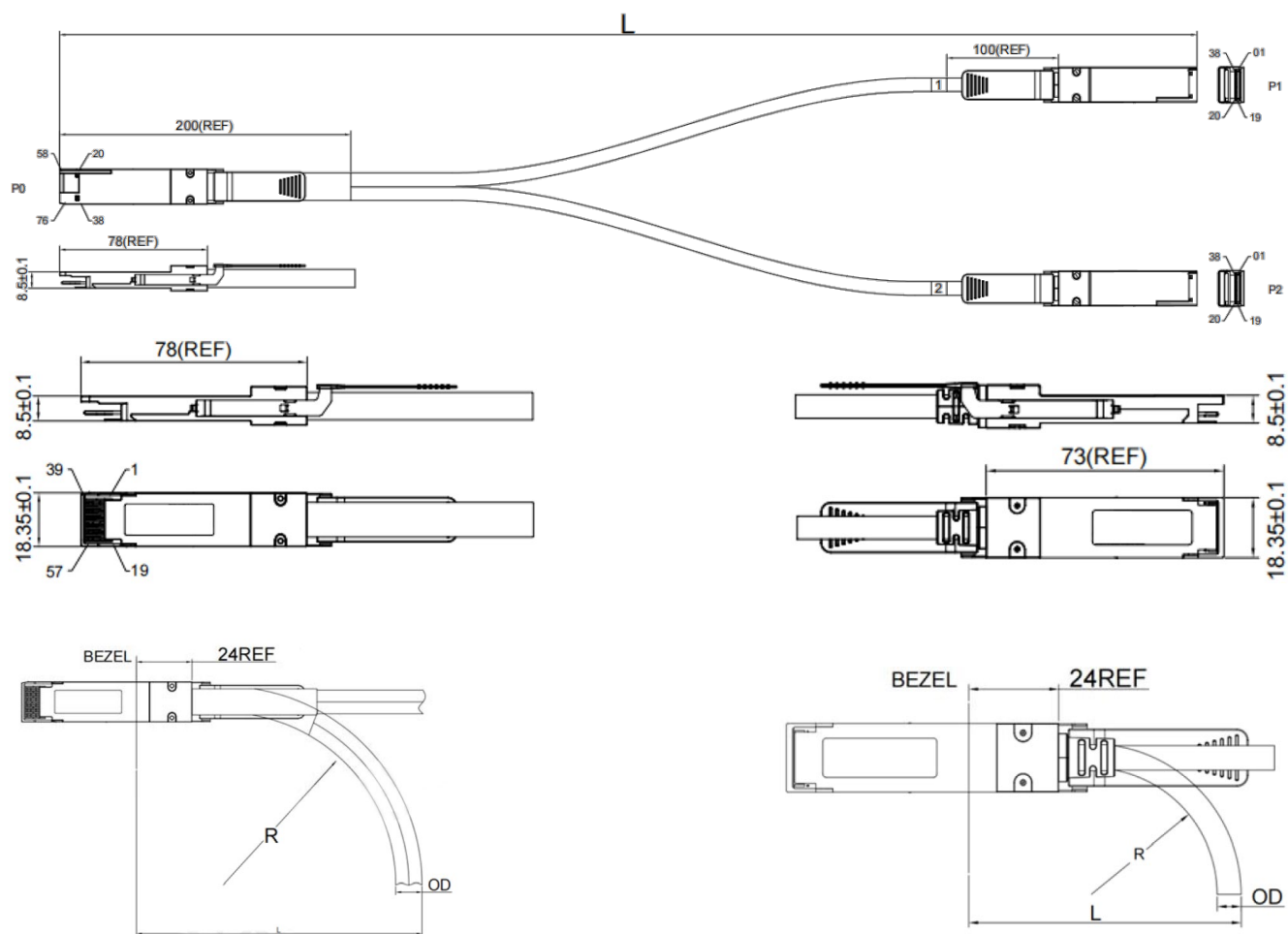


Wiring Table

WIRING DIAGRAM					
P0 END			P1&P2 END		
Pad	Signal		Pad	Signal	
1	GND	—	20	GND	
2	TX2n	→	21	RX2n	
3	TX2p	→	22	RX2p	
4	GND	—	23	GND	
5	TX4n	→	24	RX4n	
6	TX4p	→	25	RX4p	
7	GND	—	26	GND	
13	GND	—	35	GND	
14	RX3p	←	36	TX1p	
15	RX3n	←	37	TX1n	
16	GND	—	38	GND	
17	RX1p	←	36	TX1p	
18	RX1n	←	37	TX1n	
19	GND	—	38	GND	
20	GND	—	1	GND	
21	RX2n	←	2	TX2n	
22	RX2p	←	3	TX2p	
23	GND	—	1	GND	
24	RX4n	←	2	TX2n	
25	RX4p	←	3	TX2p	
26	GND	—	4	GND	
32	GND	—	16	GND	
33	TX3p	→	17	RX1p	
34	TX3n	→	18	RX1n	
35	GND	—	19	GND	
36	TX1p	→	17	RX1p	
37	TX1n	→	18	RX1n	
38	GND	—	19	GND	

WIRING DIAGRAM					
P0 END			P3&P4 END		
Pad	Signal		Pad	Signal	
39	GND	—	20	GND	
40	TX6n	→	21	RX2n	
41	TX6p	→	22	RX2p	
42	GND	—	23	GND	
43	TX8n	→	24	RX4n	
44	TX8p	→	25	RX4p	
45	GND	—	26	GND	
51	GND	—	35	GND	
52	RX7p	←	36	TX1p	
53	RX7n	←	37	TX1n	
54	GND	—	38	GND	
55	RX5p	←	36	TX1p	
56	RX5n	←	37	TX1n	
57	GND	—	38	GND	
58	GND	—	1	GND	
59	RX6n	←	2	TX2n	
60	RX6p	←	3	TX2p	
61	GND	—	1	GND	
62	RX8n	←	2	TX2n	
63	RX8p	←	3	TX2p	
64	GND	—	4	GND	
70	GND	—	16	GND	
71	TX7p	→	17	RX1p	
72	TX7n	→	18	RX1n	
73	GND	—	19	GND	
74	TX5p	→	17	RX1p	
75	TX5n	→	18	RX1n	
76	GND	—	19	GND	

Mechanical Specifications



QSFP-DD				QSFP			
Gauge	OD	Bend Radius "R"	Min. Bend Radius "L"	Gauge	OD	Bend Radius "R"	Min. Bend Radius "L"
30AWG	14MM	70MM	170MM	30AWG	7.0MM	35MM	75MM

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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