QSFP28-100GB-ZR4P-CN2-OPC

Ciena® Compatible TAA 100GBase-ZR4+ QSFP28 Transceiver (SMF, 1295nm to 1309nm, 80/95km, LC, DOM)

Features

- Supports up to 103Gbps
- Single 3.3V Power Supply
- Power Dissipation 5.5W
- Four 25Gbps EML LAN-WDM lasers on the transmitter side
- Receiver: 4x25Gbps SOA+PIN ROSA
- 4x25Gbps Electrical Interface
- Hot-pluggable QSFP28 MSA form factor
- Duplex LC Connector
- I2C interface with integrated Digital Diagnostic Monitoring
- Commercial Temperature 0 to 70 Celsius
- RoHS Compliant and Lead Free

Applications:

- 100GBase Ethernet

Product Description

This Ciena® compatible QSFP28 transceiver provides 100GBase-ZR4+ throughput up to 80/95km over single-mode fiber (SMF) using a wavelength of 1295nm to 1309nm via an LC connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Ciena®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Maximum Supply Voltage	Vcc	-0.5		3.6	V
Storage Temperature	Tstg	-40		85	℃
Operating Case Temperature	Tc	0		70	℃
Operating Relative Humidity	RH	5		85	%

Notes:

1. Exceeding any one of these values may destroy the device immediately.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	P_{DISS}			5.5	W	
Transmitter						
Differential Data Input Swing Per Lane				900	mVp-p	
Input Differential Impedance	ZIN	85	100	115	Ω	
Stressed Input Parameters						
Eye Width		0.46			UI	
Applied Pk-Pk Sinusoidal Jitter		IEEE 802.3bm Table 88-13				
Eye Height		95			mV	
DC Common-Mode Voltage		-350		2850	mV	
Receiver						
Differential Output Amplitude		200		900	mVp-p	
Output Differential Impedance	ZOUT	85	100	115	Ω	
Eye Width		0.57			UI	
Eye Height Differential		228			mV	
Vertical Eye Closure				5.5	dB	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Speed Per Lane	BRAVE		25.78		Gbps	
Data Rate Variation		-100		100	ppm	
Lane 0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm	
Lane 1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm	
Lane 2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm	
Lane 3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm	
Spectral Width (-20dB)	Δλ			1	nm	
Total Average Output Power	POUT			13	dBm	
Average Launch Power Per Lane	P_{each}	3		7	dBm	1
Optical Modulation Amplitude Per Lane	POMA	3.7		7.8	dBm	
Average Launch Power of Off Transmitter Per Lane	Poff			-30	dBm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Transmitter Dispersion Penalty Per Lane	TDP			3	dB	4
Difference in Launch Power Between Any Two Lanes				3.6	dB	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-26		
Extinction Ratio	ER	6	8		dB	
Transmitter Eye Mask Definition: X1, X2, X3, Y1, Y2, Y3	(0.25, 0.4, 0.45, 0.25, 0.28, 0.4)					
Receiver						
Signaling Speed Per Lane	BRAVE		25.78		Gbps	
Data Rate Variation		-100		100	ppm	
Damage Threshold Per Lane (Minimum)	THd			5.5	dBm	3
Lane 0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm	
Lane 1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm	
Lane 2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm	
Lane 3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm	
Average Receive Power Per Lane	Rx_pow	-31		4.5	dBm	2
Receiver Overload Per Lane	Psat	4.5			dBm	
Receive Sensitivity Average Per Lane	Rx_sens			-29	dBm	4
Stressed Sensitivity Per Lane	SRS			-25.1	GHz	4
Receiver Reflectance				-26	dBm	
LOS Assert	LOSA	-40			dBm	
LOS De-Assert	LOSD			-31.5	dBm	
LOS Hysteresis		0.5			dB	

Notes:

1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Average receive power, per lane (minimum), is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Measured with conformance test signal for BER=$5E^{-5}$ @25.78Gbps and $PRBS^{31}$-1.

Pin Descriptions

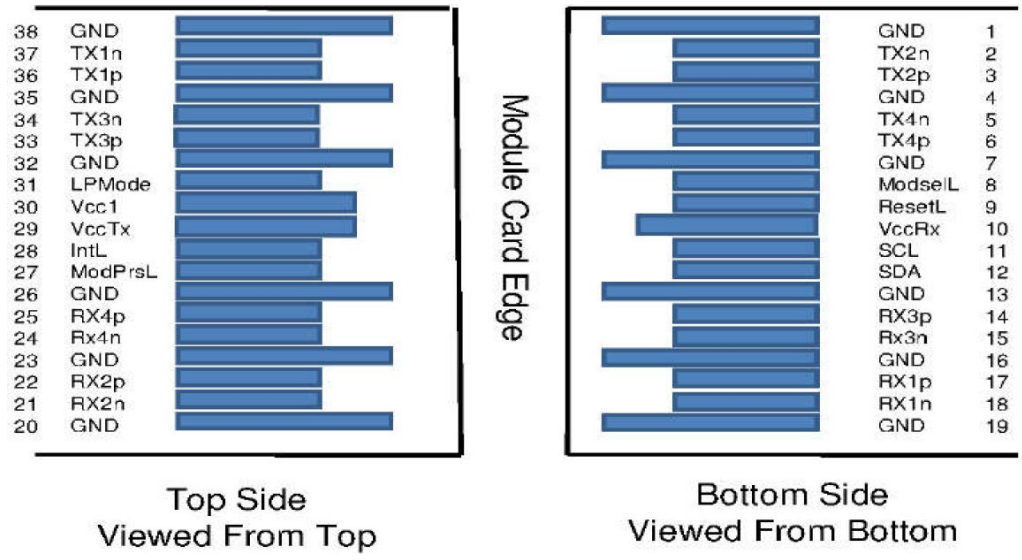
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Receiver Power Supply.	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1

27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL	Interrupt.	3	
29		VccTx	+3.3V Transmitter Power Supply.	2	2
30		Vcc1	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMode	Low-Power Mode.	3	
32		GND	Module Ground.	1	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3	
35		GND	Module Ground.	1	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

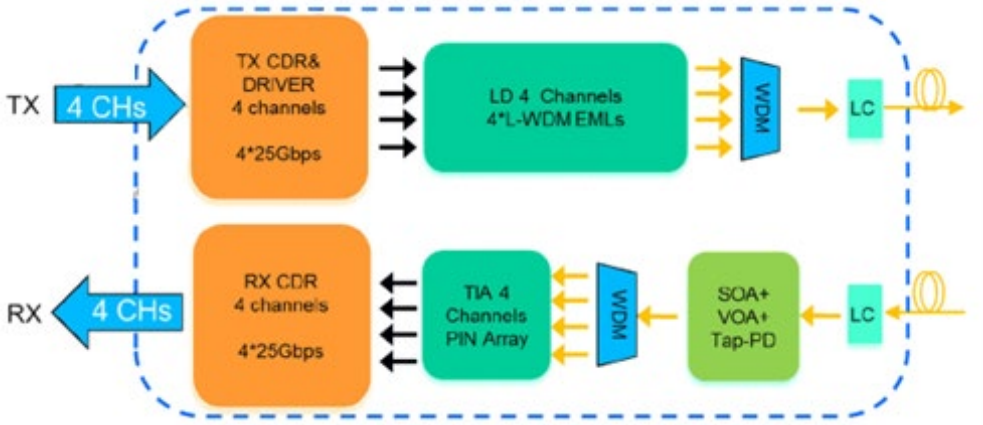
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, Vcc1, and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1, and VccTx may be internally connected within the QSFP28 module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Electrical Pin-Out Details



Function Block Diagram



Mechanical Specifications