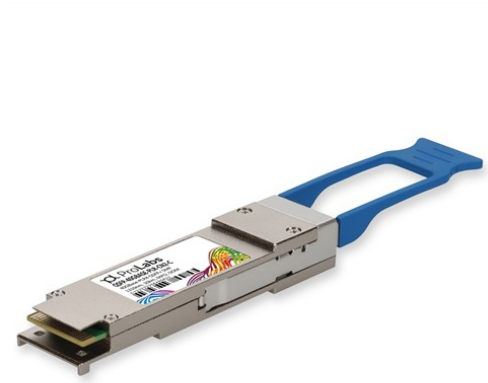
QSFP-40GBASE-PLR-CN2-C

Ciena® Compatible TAA 40GBase-PLR4 QSFP+ Transceiver (SMF, 1310nm, 10km, MPO, DOM)

Features:

- SFF-8436 Compliance
- MPO Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free



Applications:

- 40GBase Ethernet
- Access and Enterprise

Product Description

This Ciena® compatible QSFP+ transceiver provides 40GBase-PLR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is guaranteed to be 100% compatible with Ciena® transceivers. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Rev. 041426

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Supply Voltage	Vcc	-0.3		3.6	V	
Relative Humidity	RH	0		85	%	
Input Voltage	VIN	-0.3		Vcc+0.3V		
Data Rate Per Lane	DR		10.3125	11.1	Gbps	
Link Distance with G.652	D			10	km	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption	PD			3.5	W	
Differential Input Voltage Amplitude	VIN	120		1200	mVp-p	
Differential Output Voltage Amplitude	VOUT	400		800	mVp-p	
Input Logic Level - High	VIH	2.0		Vcc	V	
Input Logic Level - Low	VIL	0		0.8	V	
Output Logic Level - High	VOH	Vcc-0.5		Vcc	V	
Output Logic Level - Low	VOL	0		0.4	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λC	1260	1310	1355	nm	1
Spectral Width (-20dB)				1	nm	1
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	Pavg	-5.2		1.5	dBm	
Optical Modulation Amplitude (OMA)	TOMA	-4.5		2.0	dBm	1
Difference in Launch Power Between Any Two Lanes	Ptx, diff			5.0	dB	
Launch Power in OMA Minus Transmitter and Dispersion Penalty (TDP) Per Lane	OMA-TDP	-9.7			dBm	1
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	ORLT			12	dB	
Transmitter Reflectance	TR			-12	dB	
Average Launch Power of Off Transmitter Per Lane	Toff			-30	dBm	
Transmitter Eye Mask Definition : {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Receiver						
Center Wavelength	λC	1260	1310	1355	nm	
Damage Threshold Per Lane	THd	3			dBm	
Overload Per Lane		1			dBm	
Receiver Sensitivity in OMA Per Lane @ BER $1E^{-12}$				12.6	dBm	
Signal Loss Assert Threshold		-30			dBm	
Signal Loss De-Assert Threshold				-15	dBm	
LOS Hysteresis		0.5		6	dB	
Receiver Reflectance	RR			-12	dBm	

Notes:

1. Transmitter wavelength, spectral width, and power need to meet the OMA minus TDP specs to guarantee link performance.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	
4		GND	Module Ground.	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	
7		GND	Module Ground.	1
8	LVTTL-I	ModSelL	Module Select.	3
9	LVTTL-I	ResetL	Module Reset.	4
10		VccRx	+3.3V Receiver Power Supply.	2
11	LVCMOS	SCL	2-Wire Serial Interface Clock.	5
12	LVCMOS	SDA	2-Wire Serial Interface Data.	5
13		GND	Module Ground.	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3-	Receiver Inverted Data Output.	
16		GND	Module Ground.	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	
18	CML-O	Rx1-	Receiver Inverted Data Output.	
19		GND	Module Ground.	1
20		GND	Module Ground.	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	
23		GND	Module Ground.	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	
26		GND	Module Ground.	1
27	LVTTL-O	ModPrsL	Module Present.	6
28	LVTTL-O	IntL	Interrupt	7
29		VccTx	+3.3V Transmitter Power Supply.	2
30		Vcc1	+3.3V Power Supply.	2
31	LVTTL-I	LPMode	Low-Power Mode.	8
32		GND	Module Ground.	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	
35		GND	Module Ground.	1

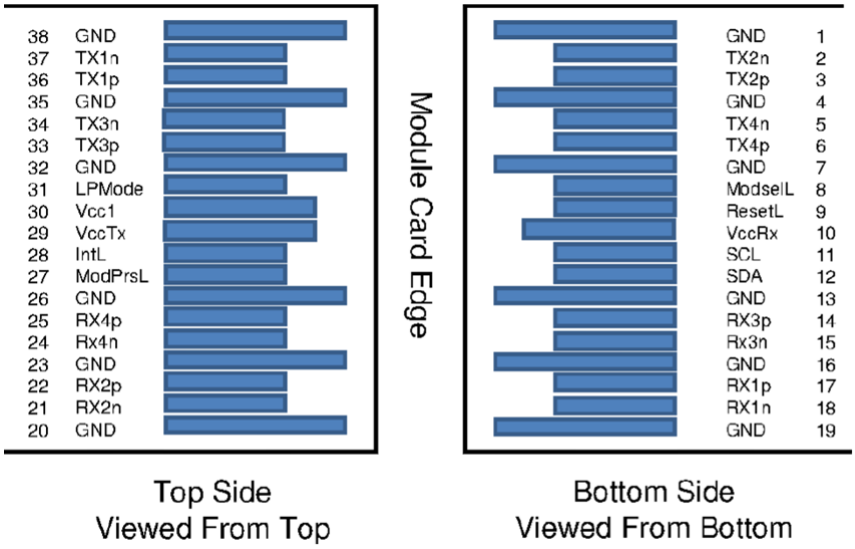
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1-	Transmitter Inverted Data Output.	
38		GND	Module Ground.	1

Notes:

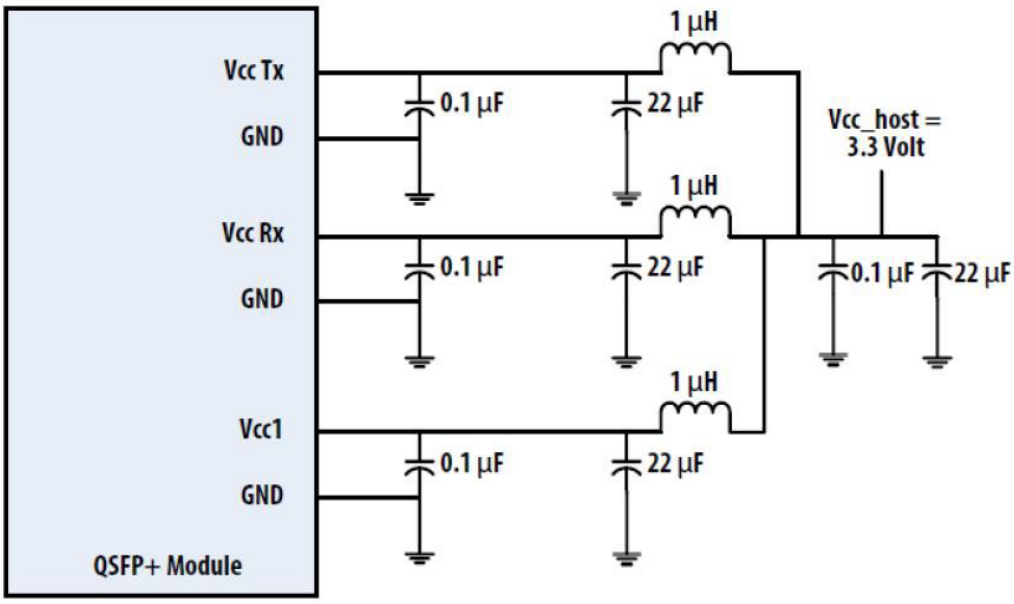
1. GND is the symbol for signal and supply (power) common for the module. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, Vcc1, and VccTx shall be applied concurrently. VccRx, Vcc1, and VccTx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA. Recommended host board power supply filtering is shown below.
3. The ModSelL is an input pin. When held “low” by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "high," the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "high" state in the module.
   In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.
4. The ResetL pin shall be pulled to the Vcc in the module. A “low” level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the “low” level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.
5. Low-speed signaling other than SCL and SDA is based on Low-Voltage TTL (LVTTL) operating at the Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Host_Vcc, or Vcc1.
   Hosts shall use a pull-up resistor connected to the Host_Vcc on each of the 2-wire interface SCL (clock), SDA (data), and all low-speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology.
6. ModPrsL is pulled up to the Host_Vcc on the host board and grounded in the module. The ModPrsL is asserted "low" when inserted and de-asserted "high" when the module is physically absent from the host connector.
7. IntL is an output pin. When IntL is “low,” it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is de-asserted “high" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of 0 and the flag field is read (see SFF-8636).

8. The LPMode pin shall be pulled up to the Vcc in the module. The pin is a hardware control used to put modules into a low-power mode when “high.” By using the LPMode pin and a combination of the Power_override, Power_set, and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0, 1, 2), the host controls how much power a module can dissipate.

Electrical Pin-Out Details

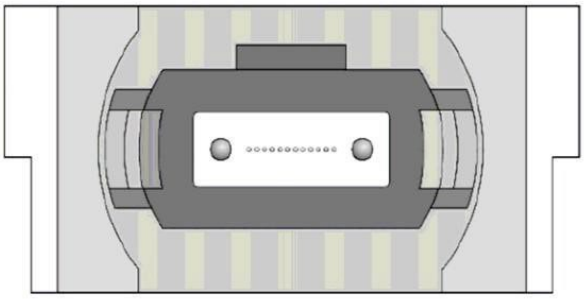


Power Supply Filter



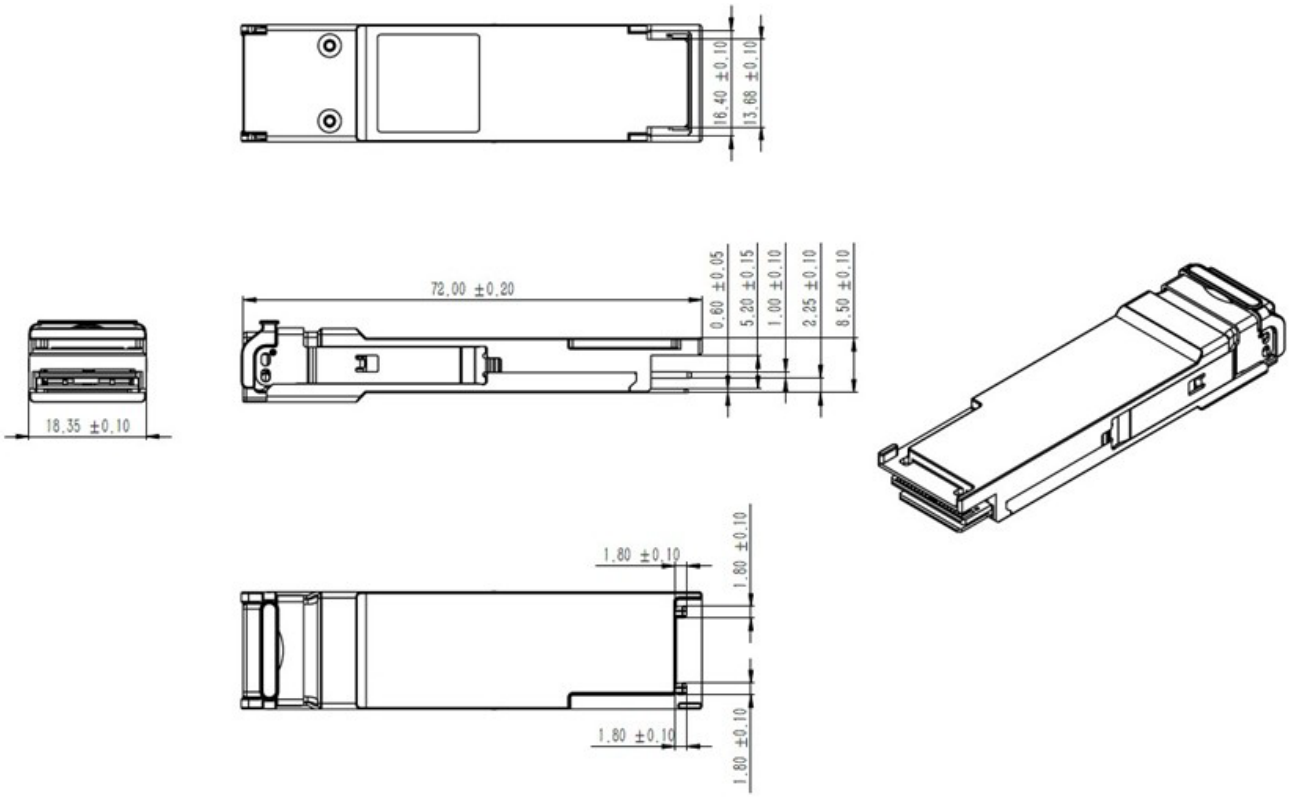
Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector. The four fiber positions on the left as shown below, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.



Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

Mechanical Specifications



About ProLabs

Our extensive experience comes as standard. For over 20 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with more than 100 optical switching and transport platforms.

A Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 1.6T while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

The Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure compatible products, and immediate answers to your questions. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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