NTTA03AA-OPC

Ciena® NTTA03AA Compatible TAA 100GBase-SR10 CFP Transceiver (MMF, 850nm, 150m, MPO, DOM)

Features

- CFP MSA 1.4 Compliance
- MPO Connector
- Multi-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free

Applications:

- 100GBase Ethernet
- Access and Enterprise

Product Description

This Ciena® NTTA03AA compatible CFP transceiver provides 100GBase-SR10 throughput up to 150m over multi-mode fiber (MMF) using a wavelength of 850nm via an MPO connector. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Ciena®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TST	-20	+85	℃
Supply Voltage	VCC	-0.3	3.6	V
Input Voltage	VIN	-0.3	VCC+0.3	V
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	TOP	0		+70	℃
Power Supply Voltage	VCC	3.13	3.3	3.47	V
Power Supply Current	ICC			300	mA
Surge Current	ISurge			+30	mA
Data Rate Per Lane	fd			11.2	Gbps

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude	ΔVin	120		820	mVp-p
Differential Output Voltage Amplitude	ΔVout	300		820	mVp-p
Input Logic Level High	VIH	2.0		VCC	V
Input Logic Level Low	VIL	0		0.8	V
Output Logic Level High	VOH	VCC-0.5		VCC	V
Output Logic Level Low	VOL	0		0.4	V

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Rate				11.2	Gbps
Transmitter					
Center Wavelength	λc	840	850	860	nm
RMS Spectral Width	λ		0.5	0.65	nm
Average Optical Power (per channel)	Pout	-8	-25	+1	dBm
Average Optical Power (per channel) Disabled	Poff			-30	dBm
Optical Return Loss Tolerance				12	dB
Extinction Ratio	ER	3			dB
Transmitter eye mask	Compliant to IEEE802.3a eye mask specification				
Receiver					
Center Wavelength	λc	840	850	860	nm
RMS Spectral Width	λ		0.5	0.65	nm
Optical Return Loss	RI	12			dB
Optical Power Sensitivity (per channel)	Pin min		-12	-9.9	dBm
Optical Power Saturation (per channel)	Pin max	+1			dBm
Stressed Receiver Sensitivity	Ps			-5.4	dBm

Pin Descriptions

Part A: Bottom Row Pin Function Definition

Pin	Symbol	Type	I/O	Description
1	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, Can be separate or tied together with Signal Ground
2	3.3V_GND	GND		
3	3.3V_GND	GND		
4	3.3V_GND	GND		
5	3.3V_GND	GND		
6	3.3V	VCC		3.3V Module Supply
7	3.3V	VCC		
8	3.3V	VCC		
9	3.3V	VCC		
10	3.3V	VCC		
11	3.3V	VCC		
12	3.3V	VCC		
13	3.3V	VCC		
14	3.3V	VCC		
15	3.3V	VCC		
16	3.3V_GND	GND		
17	3.3V_GND	GND		
18	3.3V_GND	GND		
19	3.3V_GND	GND		
20	3.3V_GND	GND		
21	NC		I/O	Do not use
22	NC		I/O	Do not use
23	GND	GND		
24	(TX_MCLKn)	CML	O	Do not use
25	(TX_MCLKp)	CML	O	Do not use
26	GND	GND		
27	NC		I/O	Do not use
28	NC		I/O	Do not use
29	NC		I/O	Do not use
30	PRG_CTL1	LVCMOS w/PU	I	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn-TX & RX IC reset. “0”=reset, “1” or NC = enabled or not used
31	PRG_CTL2	LVCMOS w/PU	I	Programmable Control 2 set via MDIO, MSA default: Hardware power Interlock LSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = >24W or not used
32	PRG_CTL3			Programmable Control 3 set via MDIO, MSA default: Hardware power Interlock MSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = >24W or not used
33	PRG_ALRM1	LVCMOS	O	Programmable Alarm 1 set via MDIO, Reflex default: HIPWR_ON, Module power on indicator. “1” = Module high power up completed, “0” = Module not high powered up
34	PRG_ALRM2	LVCMOS	O	Programmable Alarm 2 set via MDIO, Reflex default: MOD_READY, module initialization complete, “1” = complete, “0” = not complete

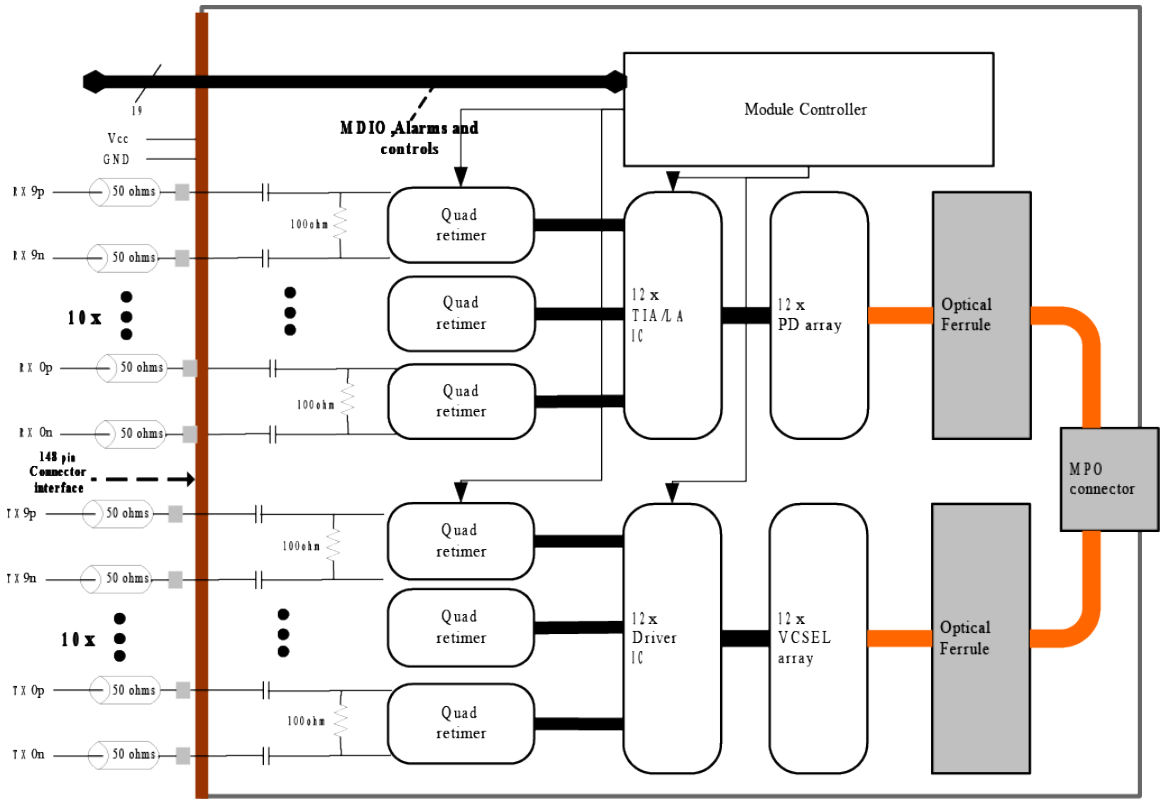
35	PRG_ALRM3	LVCMOS	O	Programmable Alarm 3 set via MDIO, Reflex default: MOD_FAULT, module fault detected, “1” = fault, “0” = no fault
36	TX_DIS	LVCMOS w/PU	I	Transmitter Disable for all channels, “1” or NC = transmitter disabled, “0” = transmitter enabled
37	MOD_LOPW	LVCMOS w/PU	I	Module low power mode. “1” or NC = module in low power (safe) mode, “0” = power-on enabled
38	MOD_ABS	GND	O	Module Absent. “1” or NC = Module absent, “0” = module present. Pull-up resistor on Host
39	MOD_RSTn	LVCMOS w/PD	I	Module Reset. “0” = reset the module, “1” or NC = module enabled, Pull Down resistor in module
40	RX_LOS	LVCMOS	O	Receiver loss of optical signal on any channel, “1” = loss of signal, “0” = normal condition
41	GLB_ALRMn	LVCMOS	O	Global Alarm. “0” = alarm condition in any MDIO alarm register, “1” = no alarm
42	PRTADR4	1.2V CMOS	I	MDIO port address bit 4
43	PRTADR3	1.2V CMOS	I	MDIO port address bit 3
44	PRTADR2	1.2V CMOS	I	MDIO port address bit 2
45	PRTADR1	1.2V CMOS	I	MDIO port address bit 1
46	PRTADR0	1.2V CMOS	I	MDIO port address bit 0
47	MDIO	1.2V CMOS	I/O	Management Data I/O bi-directional data (electrical specs as per 802.3ae)
48	MDO	1.2V CMOS	I	Management data clock (electrical specs as per 802.3ae)
49	GND	GND		
50	NC		I/O	Do not use
51	NC		I/O	Do not use
52	GND	GND		
53	NC		I/O	Do not use
54	NC		I/O	Do not use
55	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND	GND		
57	3.3V_GND	GND		
58	3.3V_GND	GND		
59	3.3V_GND	GND		
60	3.3V	VCC		3.3V Module Supply
61	3.3V	VCC		
62	3.3V	VCC		
63	3.3V	VCC		
64	3.3V	VCC		
65	3.3V	VCC		
66	3.3V	VCC		
67	3.3V	VCC		
68	3.3V	VCC		
69	3.3V	VCC		
70	3.3V_GND	GND		
71	3.3V_GND	GND		
72	3.3V_GND	GND		

73	3.3V_GND	GND		
74	3.3V_GND	GND		

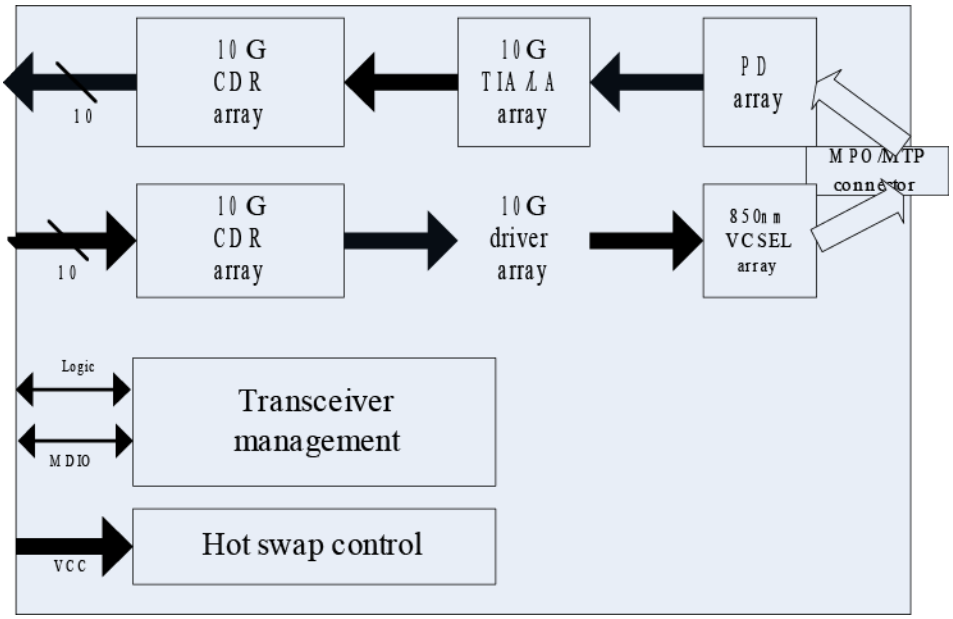
Part B: Top Row Pin Function Definition

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
148	GND	**136**	GND	**124**	GND	**112**	GND	**100**	RX7p
147	Not used	**135**	TX7n	**123**	TX3n	**111**	GND	**99**	GND
146	Not used	**134**	TX7p	**122**	TX3p	**110**	Not used	**98**	RX6n
145	GND	**133**	GND	**121**	GND	**109**	Not used	**97**	RX6p
144	Not used	**132**	TX6n	**120**	TX2n	**108**	GND	**96**	GND
143	Not used	**131**	TX6p	**119**	TX2p	**107**	RX9n	**95**	RX5n
142	GND	**130**	GND	**118**	GND	**106**	RX9p	**94**	RX5p
141	TX9n	**129**	TX5n	**117**	TX1n	**105**	GND	**93**	GND
140	TX9p	**128**	TX5p	**116**	TX1p	**104**	RX8n	**92**	RX4n
139	GND	**127**	GND	**115**	GND	**103**	RX8p	**91**	RX4p
138	TX8n	**126**	TX4n	**114**	TX0n	**102**	GND	**90**	GND
137	TX8p	**125**	TX4p	**113**	TX0p	**101**	RX7n	**89**	RX3n
88	RX3p	**85**	RX2p	**82**	RX1p	**79**	RX0p	**76**	Not used
87	GND	**84**	GND	**81**	GND	**78**	GND	**75**	GND
86	RX2n	**83**	RX1n	**80**	RX0n	**77**	Not used		

CFP Module Functional Block Diagram



Module Block Diagram



Mechanical Specifications