



### **MCA7J60-N004-OPC**

Mellanox® MCA7J60-N004 Compatible TAA 800GBase-CU OSFP112 to 2xOSFP112-RHS Direct Attach Cable (Active Twinax, 4m, Infiniband)

#### **Features**

- OSFP Module Compliant to MSA Standards
- Transmission Data Rate Up to PAM4 106.25Gbps Per Channel
- InfiniBand NDR Compatible
- Low Power Consumption
- Enable Auto-Negotiation and Link Training
- Linear PAM4 Programmable Equalizer Optimized for 56GBaud Copper Link
- Supports Device Programming by MCU with I2C
- 3.3V Power Supply
- Low Latency: 10ps
- Operating Temperature Range: 0 to 70 Celsius
- RoHS Compliant and Lead-Free



#### **Applications:**

- 800GBase Ethernet

#### **Product Description**

This is a Mellanox® compatible 800GBase-CU OSFP112 to 2xOSFP112-RHS direct attach cable that operates over active copper with a maximum reach of 4.0m (13.1ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

## General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Tstg	-40		85	°C
Operating Case Temperature	Tc	0		70	°C
Supply Voltage	Vcc	-0.3	3.3	3.6	V
Relative Operating Humidity	RH	5		85	%
Data Rate	DR		800		Gbps

## Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Length	L			4	M	
AWG			25		AWG	
Jacket Material		Plastic Braided Mesh Technology Net, Red				

## Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.1	3.3	3.5	V	
Input Amplitude		800		1200	mVp-p	
Input Low Voltage	VIL	-0.3		0.35*Vcc	V	
Input High Voltage	VIH	0.65*Vcc		Vcc+0.3	V	
Output Logic Low	VOL			0.25*Vcc	V	
I2C Master Mode Output Frequency			400		kHz	
800G End Power Consumption			1.2	1.5	W	
400G End Power Consumption			0.6	0.7	W	
Raw Cable Impedance	Zca	90	100	110	Ω	
Mated Connector Impedance	Zmated	85		115	Ω	
Maximum Insertion Loss @26.56GHz	SDD21	11		19.75	dB	
Differential to Common-Mode Return Loss	SDD11/22	$RL_{cd}(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.76) & 26.56 \leq f \leq 40 \end{cases}$			dB	1
Differential to Common-Mode Conversion Loss	SCD21-SDD21	$Conversion\_loss(f) - \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14 - 0.3108f & 12.89 \leq f \leq 40 \end{cases}$			dB	1
Common-Mode to Common-Mode Return Loss	SCC11/22	$RL_{cc}(f) \geq 1.08$			dB	1
Minimum COM	COM	3			dB	

Minimum Cable Assembly	ERL	8.25			dB	
BER				2.4x10 <sup>-4</sup>		

**Notes:**

1. For  $0.05 \leq f \leq 40\text{GHz}$ , where f is the frequency in GHz.

**Pin Descriptions**

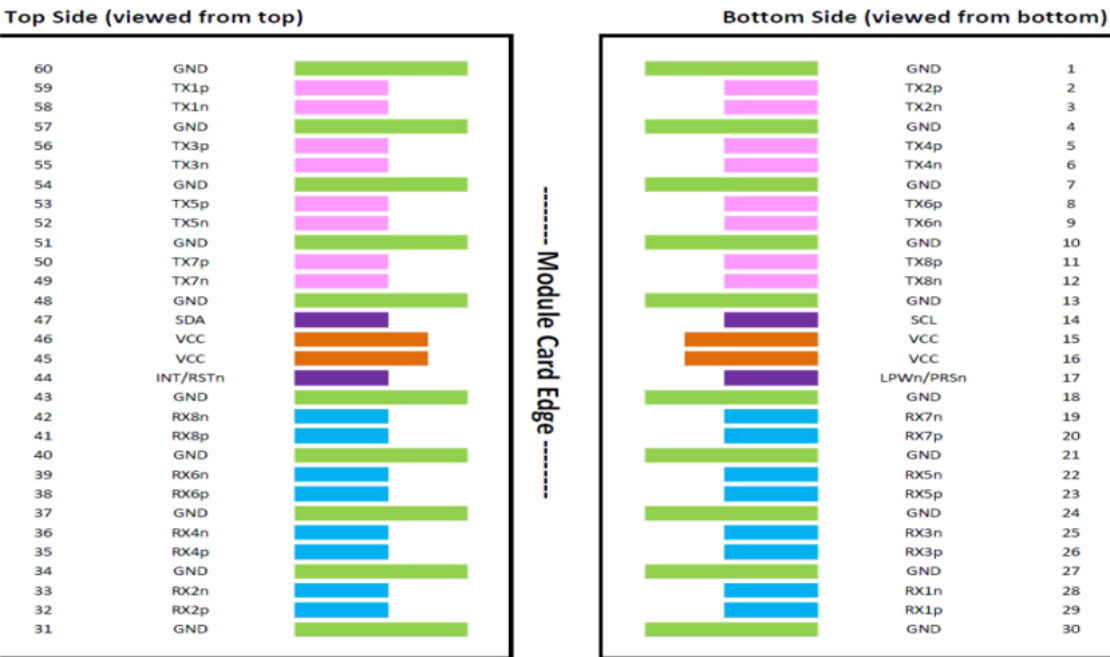
Pin	Symbol	Name/Description	Logic	Plug Sequence	Direction	Notes
1	GND	Module Ground.		1		
2	Tx2+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
3	Tx2-	Transmitter Data Inverted.	CML-I	3	Input from Host	
4	GND	Module Ground.		1		
5	Tx4+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
6	Tx4-	Transmitter Data Inverted.	CML-I	3	Input from Host	
7	GND	Module Ground.		1		
8	Tx6+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
9	Tx6-	Transmitter Data Inverted.	CML-I	3	Input from Host	
10	GND	Module Ground.		1		
11	Tx8+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
12	Tx8-	Transmitter Data Inverted.	CML-I	3	Input from Host	
13	GND	Module Ground.		1		
14	SCL	2-Wire Serial Interface Clock.	LVC MOS-I/O	3	Bi-Directional	1
15	Vcc	+3.3V Power.		2	Power from Host	
16	Vcc	+3.3V Power.		2	Power from Host	
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3	Bi-Directional	2
18	GND	Module Ground.		1		
19	Rx7-	Receiver Data Inverted.	CML-O	3	Output to Host	
20	Rx7+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
21	GND	Module Ground.		1		
22	Rx5-	Receiver Data Inverted.	CML-O	3	Output to Host	
23	Rx5+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
24	GND	Module Ground.		1		
25	Rx3-	Receiver Data Inverted.	CML-O	3	Output to Host	
26	Rx3+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
27	GND	Module Ground.		1		
28	Rx1-	Receiver Data Inverted.	CML-O	3	Output to Host	
29	Rx1+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	

30	GND	Module Ground.		1		
31	GND	Module Ground.		1		
32	Rx2+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
33	Rx2-	Receiver Data Inverted.	CML-O	3	Output to Host	
34	GND	Module Ground.		1		
35	Rx4+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
36	Rx4-	Receiver Data Inverted.	CML-O	3	Output to Host	
37	GND	Module Ground.		1		
38	Rx6+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
39	Rx6-	Receiver Data Inverted.	CML-O	3	Output to Host	
40	GND	Module Ground.		1		
41	Rx8+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
42	Rx8-	Receiver Data Inverted.	CML-O	3	Output to Host	
43	GND	Module Ground.		1		
44	INT/RSTn	Module Interrupt/Module Reset.	Multi-Level	3	Bi-Directional	2
45	Vcc	+3.3V Power.		2	Power from Host	
46	Vcc	+3.3V Power.		2	Power from Host	
47	SDA	2-Wire Serial Interface Data.	LVC MOS-I/O	3	Bi-Directional	1
48	GND	Module Ground.		1		
49	Tx7-	Transmitter Data Inverted.	CML-I	3	Input from Host	
50	Tx7+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
51	GND	Module Ground.		1		
52	Tx5-	Transmitter Data Inverted.	CML-I	3	Input from Host	
53	Tx5+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
54	GND	Module Ground.		1		
55	Tx3-	Transmitter Data Inverted.	CML-I	3	Input from Host	
56	Tx3+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
57	GND	Module Ground.		1		
58	Tx1-	Transmitter Data Inverted.	CML-I	3	Input from Host	
59	Tx1+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
60	GND	Module Ground.		1		

**Notes:**

1. Open-drain with pull-up resistor on the Host.
2. See “Pin Assignment” below for the required circuit.

Pin Assignments

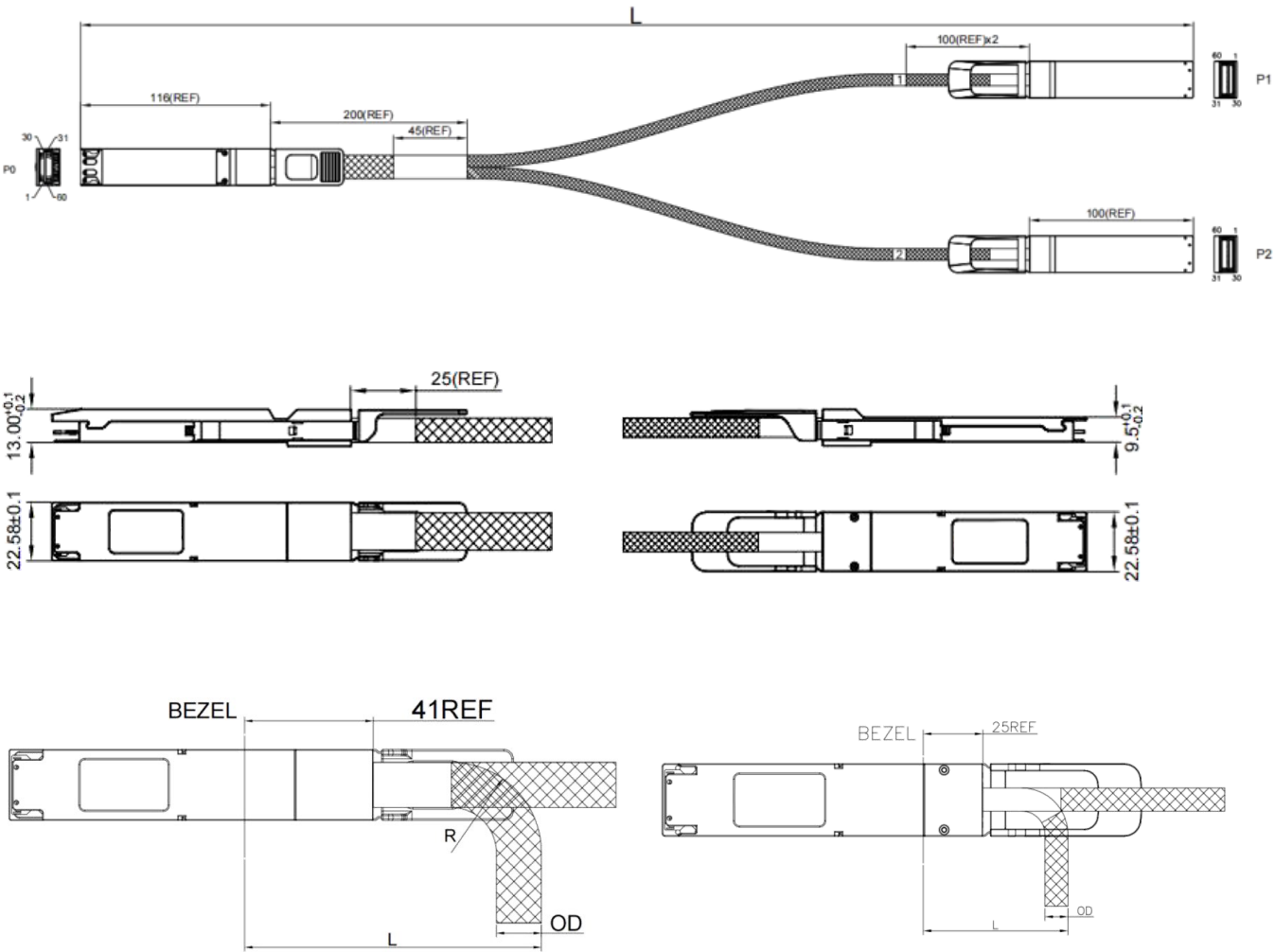


Wiring Diagram

WIRING DIAGRAM					
P0 END			P1 END		
58	TX1n	→	28	RX1n	
59	TX1p	→	29	RX1p	
28	RX1n	←	58	TX1n	
29	RX1p	←	59	TX1p	
2	TX2p	→	32	RX2p	
3	TX2n	→	33	RX2n	
32	RX2p	←	2	TX2p	
33	RX2n	←	3	TX2n	
55	TX3n	→	25	RX3n	
56	TX3p	→	26	RX3p	
25	RX3n	←	55	TX3n	
26	RX3p	←	56	TX3p	
5	TX4p	→	35	RX4p	
6	TX4n	→	36	RX4n	
35	RX4p	←	5	TX4p	
36	RX4n	←	6	TX4n	
GND GROUP 1/4/7/10/13/18/ 21/24/27/30/31/ 34/37/40/43/48/ 51/54/57/60			GND GROUP 1/4/7/10/13/18/ 21/24/27/30/31/ 34/37/40/43/48/ 51/54/57/60		
SHELL—SHIELDING—SHELL					

WIRING DIAGRAM					
P0 END			P2 END		
52	TX5n	→	28	RX1n	
53	TX5p	→	29	RX1p	
22	RX5n	←	58	TX1n	
23	RX5p	←	59	TX1p	
8	TX6p	→	32	RX2p	
9	TX6n	→	33	RX2n	
38	RX6p	←	2	TX2p	
39	RX6n	←	3	TX2n	
49	TX7n	→	25	RX3n	
50	TX7p	→	26	RX3p	
19	RX7n	←	55	TX3n	
20	RX7p	←	56	TX3p	
11	TX8p	→	35	RX4p	
12	TX8n	→	36	RX4n	
41	RX8p	←	5	TX4p	
42	RX8n	←	6	TX4n	
GND GROUP 1/4/7/10/13/18/ 21/24/27/30/31/ 34/37/40/43/48/ 51/54/57/60			GND GROUP 1/4/7/10/13/18/ 21/24/27/30/31/ 34/37/40/43/48/ 51/54/57/60		
SHELL—SHIELDING—SHELL					

Mechanical Specifications



Bending Radius

800G OSFP				OSFP RHS			
Wire Gauge	OD	Bend Radius "R"	Min. Bend Radius "L"	Wire Gauge	OD	Bend Radius "R"	Min. Bend Radius "L"
25AWG	12.1mm	25mm	86mm	25AWG	8.3mm	17mm	65mm

## **OptioConnect**

### **Innovation for the Future of High-Speed Networking**

#### **Who We Are**

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

#### **What We Do**

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

#### **Smarter Networks by Design**

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

#### **Our Team**

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

#### **Our Mission**

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

#### **Let's Connect**

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.

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