MCP7Y10-N002-OPC

Mellanox® MCP7Y10-N002 Compatible TAA 800GBase-CU OSFP to 2xQSFP112 Direct Attach Cable (Passive Twinax, 2m)

Features

- OSFP Module Compliant to MSA Standards
- QSFP112 Module Compliant to MSA Standards
- Transmission Data Rate Up to PAM4 106.25Gbps Per Channel
- Enable 800Gbps to 2x400Gbps Transmission
- Built-In EEPROM Functions with Write Protection
- Operating Temperature Range: 0 to 70 Celsius
- RoHS Compliant and Lead-Free

Applications:

- 800GBase Ethernet

Product Description

This Mellanox® compatible OSFP to 2xQSFP112 transceiver provides 800GBase-CU throughput up to over a copper connection using a wavelength of via a 2xQSFP112 connector. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Mellanox®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Tstg	-40		85	°C
Operating Case Temperature	Tc	0		70	°C
Supply Voltage	Vcc	3.13	3.3	3.47	V
Relative Operating Humidity	RH	5		85	%
Data Rate	DR		800		Gbps

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Length	L			2	M	
AWG			26		AWG	
Jacket Material		Plastic Braided Mesh Technology Net, Silver Gray				

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Resistance	Rcon			3	Ω	
Insulation Resistance	Rins			10	MΩ	
Raw Cable Impedance	Zca	95		110	Ω	
Mated Connector Impedance	Zmated	85		115	Ω	
Maximum Insertion Loss @26.56GHz	SDD21	11		19.75	dB	
Differential- to Common-Mode Return Loss	SDD11/ 22	$RLcd(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases}$			dB	1
Differential- to Common-Mode Conversion Loss	SCD21-SDD21	$\text{Conversion\_loss}(f) - \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14 - 0.3108f & 12.89 \leq f \leq 40 \end{cases}$			dB	1
Common-Mode to Common-Mode Return Loss	SCC11-22	$RLcc(f) \geq 1.08$			dB	1
Minimum COM	COM	3			dB	

Notes:

1. For $0.05 \leq f \leq 40$GHz, where f is the frequency in GHz.

Pin Descriptions for OSFP

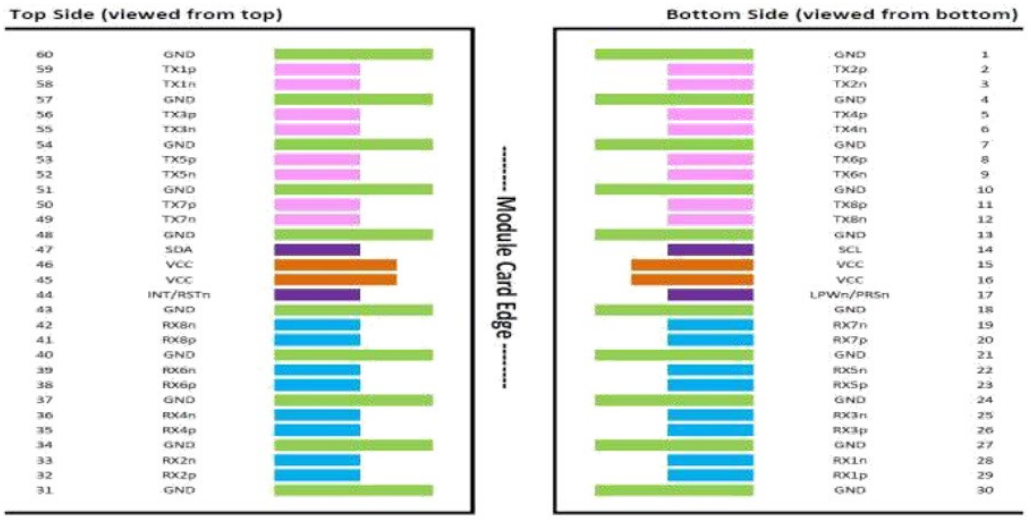
Pin	Symbol	Name/Description	Logic	Plug Sequence	Direction	Notes
1	GND	Module Ground.		1		
2	Tx2+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
3	Tx2-	Transmitter Data Inverted.	CML-I	3	Input from Host	
4	GND	Module Ground.		1		
5	Tx4+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
6	Tx4-	Transmitter Data Inverted.	CML-I	3	Input from Host	
7	GND	Module Ground.		1		
8	Tx6+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
9	Tx6-	Transmitter Data Inverted.	CML-I	3	Input from Host	
10	GND	Module Ground.		1		
11	Tx8+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
12	Tx8-	Transmitter Data Inverted.	CML-I	3	Input from Host	
13	GND	Module Ground.		1		
14	SCL	2-Wire Serial Interface Clock.	LVCMOS-I/O	3	Bi-Directional	1
15	Vcc	+3.3V Power.		2	Power from Host	
16	Vcc	+3.3V Power.		2	Power from Host	
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3	Bi-Directional	2
18	GND	Module Ground.		1		
19	Rx7-	Receiver Data Inverted.	CML-O	3	Output from Host	
20	Rx7+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
21	GND	Module Ground.		1		
22	Rx5-	Receiver Data Inverted.	CML-O	3	Output from Host	
23	Rx5+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
24	GND	Module Ground.		1		
25	Rx3-	Receiver Data Inverted.	CML-O	3	Output from Host	
26	Rx3+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
27	GND	Module Ground.		1		
28	Rx1-	Receiver Data Inverted.	CML-O	3	Output from Host	
29	Rx1+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
30	GND	Module Ground.		1		
31	GND	Module Ground.		1		
32	Rx2+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
33	Rx2-	Receiver Data Inverted.	CML-O	3	Output from Host	
34	GND	Module Ground.		1		
35	Rx4+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
36	Rx4-	Receiver Data Inverted.	CML-O	3	Output from Host	
37	GND	Module Ground.		1		
38	Rx6+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
39	Rx6-	Receiver Data Inverted.	CML-O	3	Output from Host	

40	GND	Module Ground.		1		
41	Rx8+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
42	Rx8-	Receiver Data Inverted.	CML-O	3	Output from Host	
43	GND	Module Ground.		1		
44	INT/RSTn	Module Interrupt/Module Reset.	Multi-Level	3	Bi-Directional	2
45	Vcc	+3.3V Power.		2	Power from Host	
46	Vcc	+3.3V Power.		2	Power from Host	
47	SDA	2-Wire Serial Interface Data.	LVCMOS-I/O	3	Bi-Directional	1
48	GND	Module Ground.		1		
49	Tx7-	Transmitter Data Inverted.	CML-I	3	Input from Host	
50	Tx7+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
51	GND	Module Ground.		1		
52	Tx5-	Transmitter Data Inverted.	CML-I	3	Input from Host	
53	Tx5+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
54	GND	Module Ground.		1		
55	Tx3-	Transmitter Data Inverted.	CML-I	3	Input from Host	
56	Tx3+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
57	GND	Module Ground.		1		
58	Tx1-	Transmitter Data Inverted.	CML-I	3	Input from Host	
59	Tx1+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
60	GND	Module Ground.		1		

Notes:

1. Open-drain with pull-up resistor on the host.
2. See below for required circuit.

Electrical Pin-Out Details for OSFP



Pin Descriptions for QSFP112

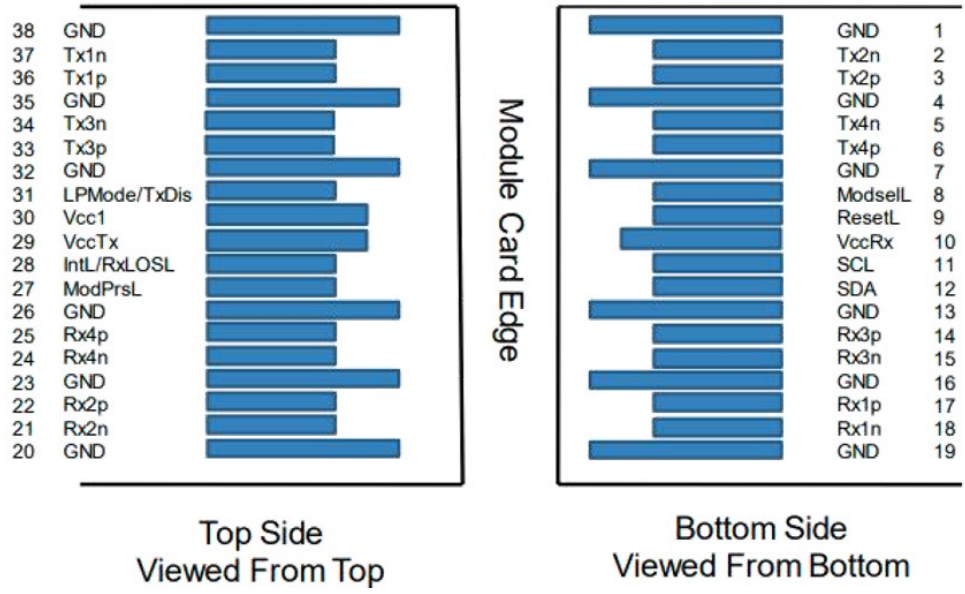
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Receiver Power Supply.	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1
27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL	Interrupt.	3	
29		Vcc	+3.3V Transmitter Power Supply.	2	2
30		Vcc	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMode	Low-Power Mode.	3	
32		GND	Module Ground.	1	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3	

35		GND	Module Ground.	1	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

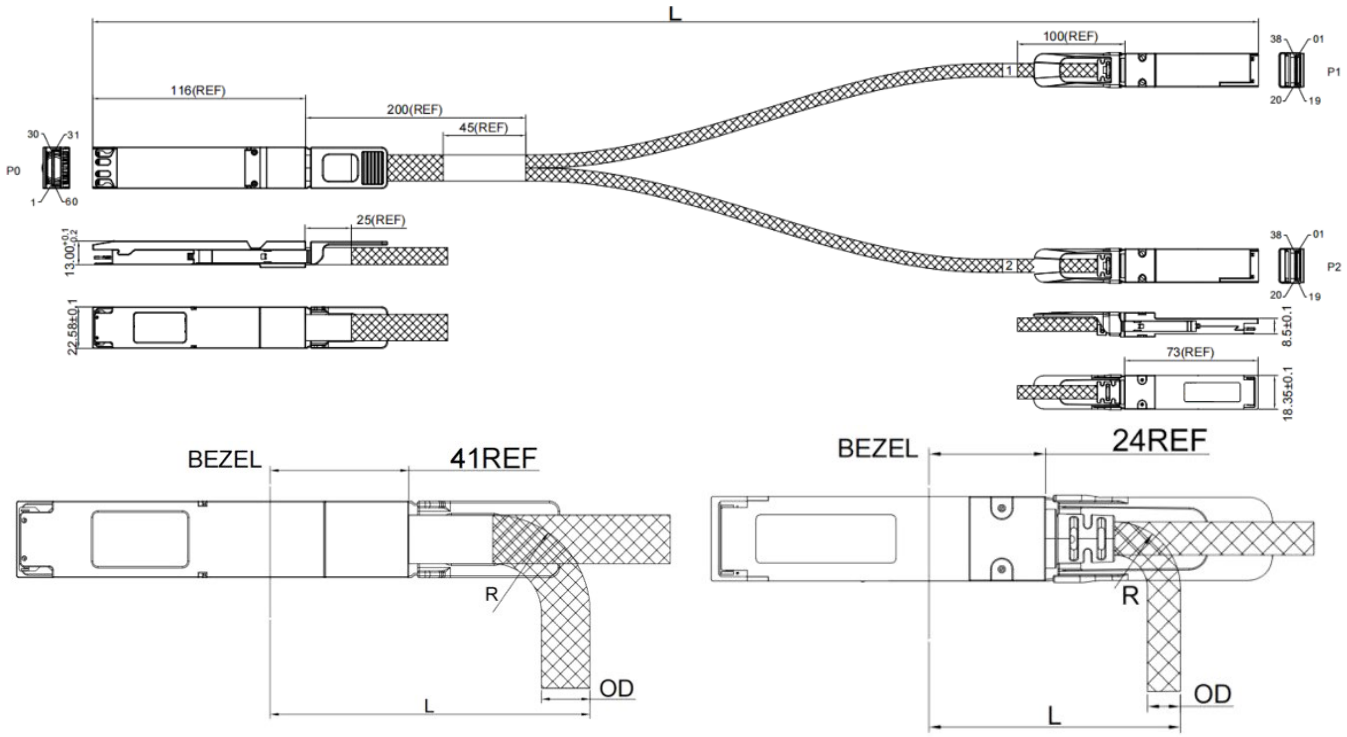
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1, and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Electrical Pin-Out Details for QSFP112



Mechanical Specifications



		800G OSFP				QSFP112	
Gauge	**OD**	**Bend Radius "R"**	**Min. Bend Radius "L"**	**Gauge**	**OD**	**Bend Radius "R"**	**Min. Bend Radius "L"**
26AWG	12.1MM	25MM	70MM	26AWG	8.3MM	17MM	55MM

OptioConnect
Innovation for the Future of High-Speed Networking

Who We Are
OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do
At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design
Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team
Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

Our Mission
To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect
Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.
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