

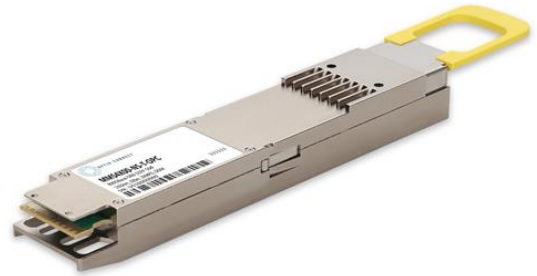


MMS4X00-NS-T-OPC

Mellanox® MMS4X00-NS Compatible TAA 800GBase-DR8 PAM4 OSFP Transceiver (SMF, 1310nm, 100m, 2xMPO, DOM, CMIS 5.0) Ethernet Only

Features

- OSFP MSA Compliant
- 8x100G PAM4/8x50G PAM4 data rates
- Supports both Ethernet and InfiniBand NDR
- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR optical interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M electrical interface
- EML transmitter and PIN PD receiver
- Cooled 1310 EML Laser
- Class 1 Laser
- Operating Temperature: 0 to 70 Celsius
- RoHS Compliant and Lead-Free
- RoHS Compliant and Lead-Free



Applications:

- 2x400GBase Ethernet

Product Description

This Mellanox® MMS4X00-NS compatible OSFP transceiver provides 800GBase-DR8 throughput up to 100m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Mellanox®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|------------------------------------|------------------|------|--------|------|------|-------|
| Power Supply Voltage | V _{CC} | -0.5 | | 3.6 | V | |
| Storage Temperature | T _{stg} | -40 | | 85 | °C | |
| Operating Case Temperature | T _c | 0 | | 70 | °C | |
| Relative Humidity (Non-Condensing) | RH | 15 | | 85 | % | |
| Data Rate | | | 106.25 | | Gbps | |
| | | | 53.125 | | Gbps | |
| Modulation Format | | | PAM4 | | | |

Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--------------------------------|--------------------------|-------|-------|-------|-------|-------|
| Power Supply Voltage | V _{CC} | 3.13 | 3.3 | 3.47 | V | |
| Module Supply Current | I _{CC} | | | 5.1 | A | |
| Power Dissipation | P _{DISS} | | | 16 | W | |
| Transmitter | | | | | | |
| Input Differential Impedance | Z _{IN} | 90 | 100 | 110 | Ω | |
| Differential Data Input Swing | V _{IN,pp} | | | 900 | mVp-p | |
| DC Common-Mode Input Voltage | | -350 | | 2850 | mV | |
| Receiver | | | | | | |
| Differential Data Output Swing | V _{OUT} | | | 900 | mV | |
| Output Differential Impedance | Z _{OUT} | 90 | 100 | 110 | Ω | 1 |
| Dual Function Signals | | | | | | |
| INT/RSTn | V _{INT/RSTn1} | 0.000 | 0.000 | 1.000 | V | 2 |
| | V _{INT/RSTn2} | 0.000 | 0.000 | 1.000 | V | 3 |
| | V _{INT/RSTn3} | 1.500 | 1.900 | 2.250 | V | 4 |
| | V _{INT/RSTn4} | 2.750 | 3.000 | 3.465 | V | 5 |
| LPWn/PRSn | V _{LPWn/PRSn_1} | 0.000 | 0.950 | 1.100 | V | 6 |
| | V _{LPWn/PRSn_2} | 1.400 | 1.700 | 2.250 | V | 7 |
| | V _{LPWn/PRSn_3} | 2.750 | 3.300 | 3.465 | V | 8 |

Notes:

1. Internally AC coupled but requires an external 100Ω differential load termination.
2. INT/RSTn voltage for no module.
3. INT/RSTn voltage for module installed, H_RSTn=Low.
4. INT/RSTn voltage for module installed, H_RSTn=High, M_INT=Low.
5. INT/RSTn voltage for module installed, H_RSTn=High, M_INT=High.

6. LPWn/PRSn for module installed, H_LPWn=Low.
7. LPWn/PRSn for module installed, H_LPWn=High.
8. LPWn/PRSn for no module.

Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--|------------|--------|------|--------|------|-------|
| Transmitter | | | | | | |
| Average Launch Per Lane | Po(100G) | -2.9 | | 4 | dBm | 1 |
| | Po(50G) | -5.1 | | 3 | dBm | 1 |
| Outer Optical Modulation Amplitude Per Lane | Poma(100G) | -0.8 | | 4.2 | dBm | 1 |
| | Poma(50G) | -3 | | 2.8 | dBm | 1 |
| Extinction Ratio | ER | 3.5 | | | dB | 2,3 |
| Lane Wavelengths | λ | 1304.5 | 1311 | 1317.5 | nm | |
| Side-Mode Suppression Ratio | SMSR | 30 | | | dB | |
| Transmitter and Dispersion Penalty Eye Closure for 100Gbps PAM4 Per Lane | TDECQ1 | | | 3.4 | dB | 2 |
| Transmitter and Dispersion Penalty Eye Closure for 50Gbps PAM4 Per Lane | TDECQ2 | | | 3.2 | dB | 3 |
| Launch Power in OMAouter Minus TDECQ for 100Gbps PAM4 Per Lane | OMA-TDECQ | -2.2 | | | dBm | 2 |
| Launch Power in OMAouter Minus TDECQ for 50Gbps PAM4 Per Lane | OMA-TDECQ | -4.4 | | | dBm | 3 |
| Average Launch Power of Off Transmitter | Poff | | | -15 | dBm | |
| Optical Return Loss Tolerance | ORLT | | | 21.4 | dB | |
| Transmitter Reflectance | | | | -26 | dB | |
| Receiver (10G) | | | | | | |
| Lane Wavelengths | | 1304.5 | 1311 | 1317.5 | nm | |
| 100G Receiver Sensitivity (OMA) | | | | -3.9 | dBm | 4 |
| 50G Receiver Sensitivity (OMA) | | | | -6.1 | dBm | 5 |
| Receiver Overload Per Lane (Pavg) | | 4 | | | dBm | |
| Damage Threshold Per Lane | | 5 | | | dBm | |
| Receive Power Per Lane (OMAouter) | | | | 4.2 | dBm | |
| Receiver Reflectance | | | | -26 | dB | |
| LOS De-Assert | | | | -10 | dBm | |
| LOS Assert | | -16 | | | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

Notes:

1. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
2. Measured with SSPRQ test pattern, @106.25Gbps PAM4.
3. Measured with SSPRQ test pattern, @53.125Gbps PAM4.

4. Measured with PRBS31Q test pattern, @53.125GBd, PAM4, and BER<2.4E⁻⁴.
5. Measured with PRBS31Q test pattern, @26.5625GBd, PAM4, and BER<2.4E⁻⁴.

Pin Descriptions

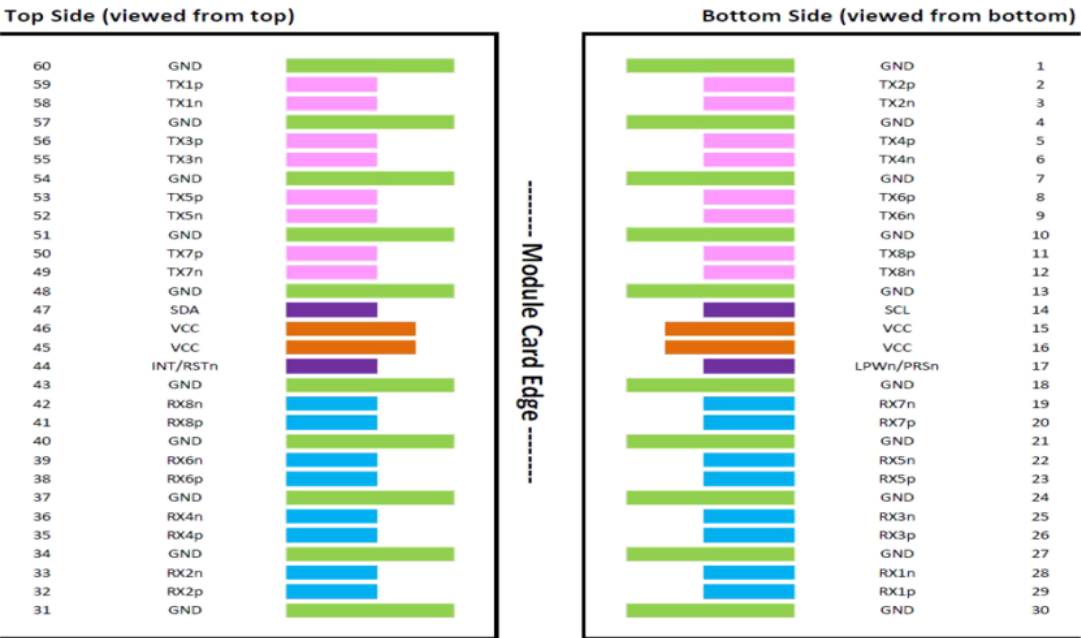
| Pin | Symbol | Name/Description | Logic | Plug Sequence | Direction | Notes |
|-----|-----------|--------------------------------|-------------|---------------|-----------------|-------|
| 1 | GND | Module Ground. | | 1 | | |
| 2 | Tx2+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 3 | Tx2- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 4 | GND | Module Ground. | | 1 | | |
| 5 | Tx4+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 6 | Tx4- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 7 | GND | Module Ground. | | 1 | | |
| 8 | Tx6+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 9 | Tx6- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 10 | GND | Module Ground. | | 1 | | |
| 11 | Tx8+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 12 | Tx8- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 13 | GND | Module Ground. | | 1 | | |
| 14 | SCL | 2-Wire Serial Interface Clock. | LVC MOS-I/O | 3 | Bi-Directional | 1 |
| 15 | Vcc | +3.3V Power. | | 2 | Power from Host | |
| 16 | Vcc | +3.3V Power. | | 2 | Power from Host | |
| 17 | LPWn/PRSn | Low-Power Mode/Module Present. | Multi-Level | 3 | Bi-Directional | 2 |
| 18 | GND | Module Ground. | | 1 | | |
| 19 | Rx7- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 20 | Rx7+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 21 | GND | Module Ground. | | 1 | | |
| 22 | Rx5- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 23 | Rx5+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 24 | GND | Module Ground. | | 1 | | |
| 25 | Rx3- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 26 | Rx3+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 27 | GND | Module Ground. | | 1 | | |
| 28 | Rx1- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 29 | Rx1+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 30 | GND | Module Ground. | | 1 | | |
| 31 | GND | Module Ground. | | 1 | | |
| 32 | Rx2+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |

| | | | | | | |
|----|----------|--------------------------------|-------------|---|-----------------|---|
| 33 | Rx2- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 34 | GND | Module Ground. | | 1 | | |
| 35 | Rx4+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 36 | Rx4- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 37 | GND | Module Ground. | | 1 | | |
| 38 | Rx6+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 39 | Rx6- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 40 | GND | Module Ground. | | 1 | | |
| 41 | Rx8+ | Receiver Data Non-Inverted. | CML-O | 3 | Output to Host | |
| 42 | Rx8- | Receiver Data Inverted. | CML-O | 3 | Output to Host | |
| 43 | GND | Module Ground. | | 1 | | |
| 44 | INT/RSTn | Module Interrupt/Module Reset. | Multi-Level | 3 | Bi-Directional | 2 |
| 45 | Vcc | +3.3V Power. | | 2 | Power from Host | |
| 46 | Vcc | +3.3V Power. | | 2 | Power from Host | |
| 47 | SDA | 2-Wire Serial Interface Data. | LVC MOS-I/O | 3 | Bi-Directional | 1 |
| 48 | GND | Module Ground. | | 1 | | |
| 49 | Tx7- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 50 | Tx7+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 51 | GND | Module Ground. | | 1 | | |
| 52 | Tx5- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 53 | Tx5+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 54 | GND | Module Ground. | | 1 | | |
| 55 | Tx3- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 56 | Tx3+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 57 | GND | Module Ground. | | 1 | | |
| 58 | Tx1- | Transmitter Data Inverted. | CML-I | 3 | Input from Host | |
| 59 | Tx1+ | Transmitter Data Non-Inverted. | CML-I | 3 | Input from Host | |
| 60 | GND | Module Ground. | | 1 | | |

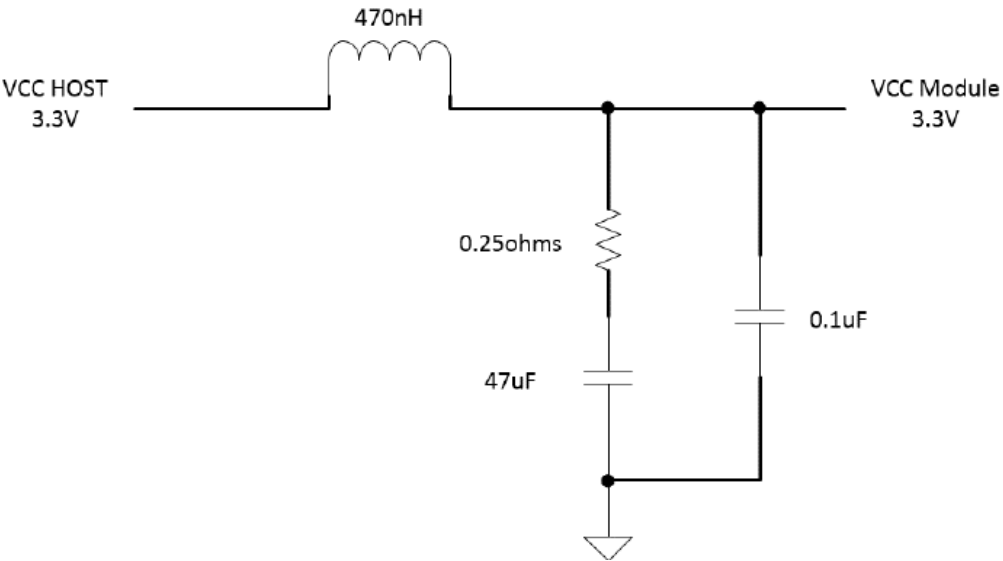
Notes:

1. Open-drain with pull-up resistor on the host.
2. See pin assignments below for the required circuit.

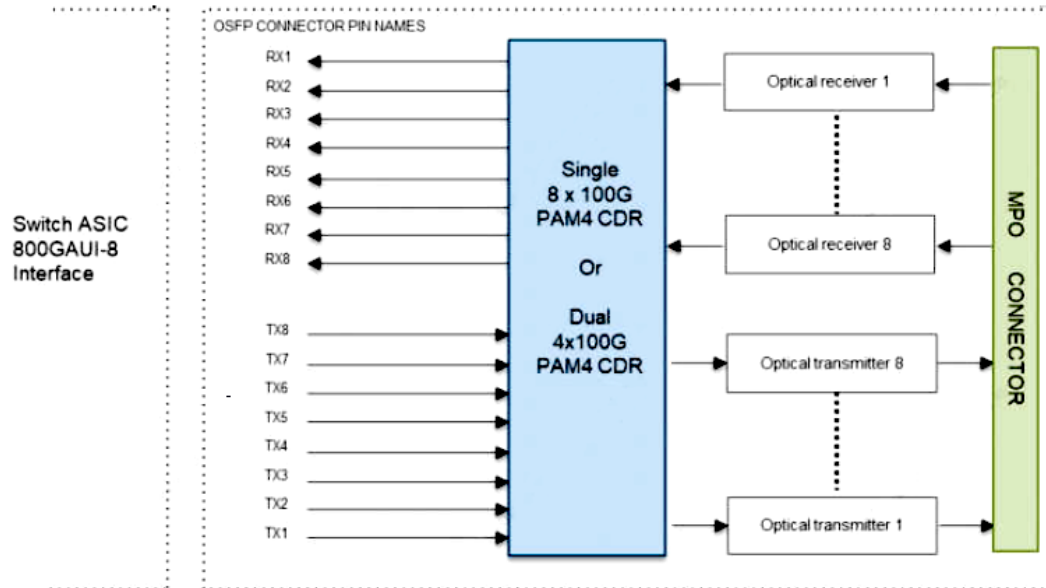
Electrical Pin-Out Details



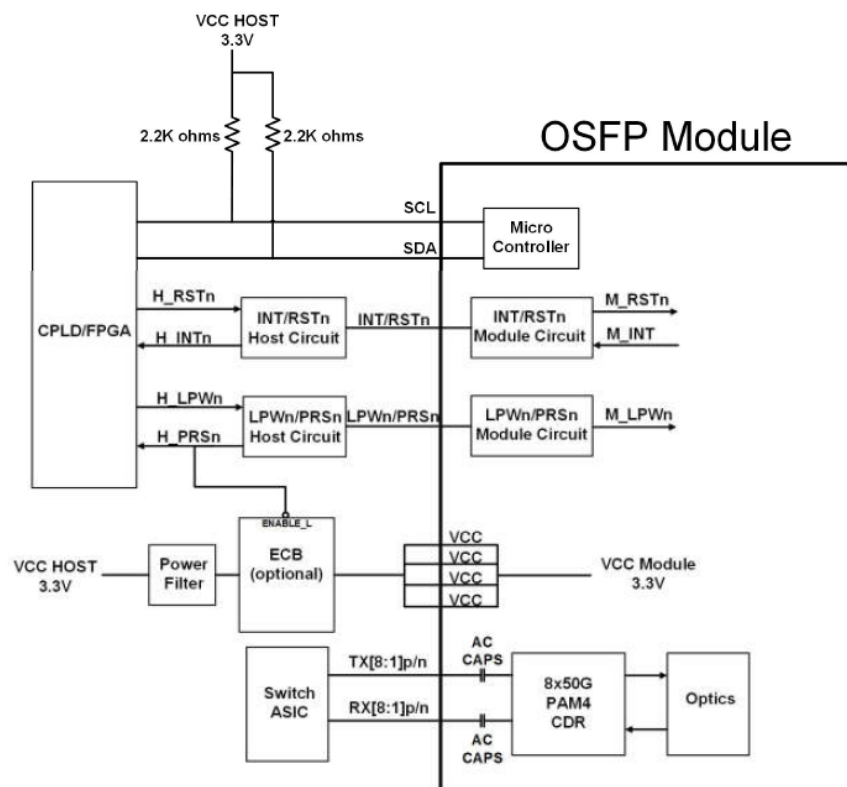
Recommended Host Board Power Supply Filter Network



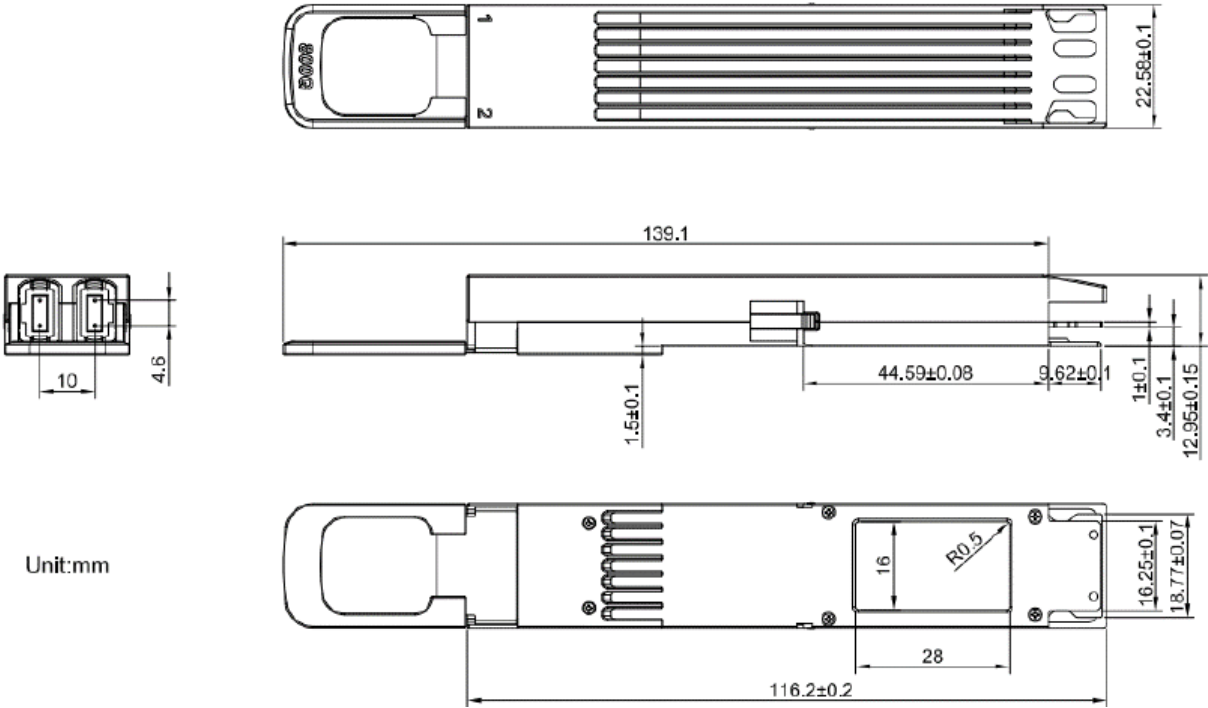
Block Diagram



Recommended Application Interface Block Diagram



Mechanical Specifications



OptioConnect

Innovation for the Future of High-Speed Networking

Who We Are

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

Our Mission

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.

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