OPTIO CONNECT

**OSFP-800GB-2XDR4-MX-OPC**

Mellanox® Compatible TAA 800GBase-2xDR4 PAM4 OSFP Transceiver (SMF, 1310nm, 100m, 2xMPO, DOM, CMIS 5.0)

**Features**

- OSFP MSA Compliant
- Supports Both Ethernet and InfiniBand NDR
- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR Optical Interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M Electrical Interface
- Supports 850Gbps
- EML Transmitter and PIN PD Receiver
- Compliant with CMIS 5.0
- Operating Temperature: 0 to 70 Celsius
- Dual MPO-12 Connector APC
- Class 1 Laser
- RoHS Compliant and Lead-Free

**Applications:**

- 800GBase Ethernet

**Product Description**

This Mellanox® compatible OSFP transceiver provides 800GBase-2xDR4 throughput up to 100m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Storage Temperature | Tstg | -40 | | 85 | °C | |
| Operating Case Temperature | Tc | 0 | | 70 | °C | |
| Power Supply Voltage | Vcc | -0.5 | | 3.6 | V | |
| Relative Humidity (Non-Condensing) | RH | 5 | | 95 | % | |
| Data Input Voltage Differential | $V_{DIP}-V_{DIN}$ | | | 1 | V | |
| Control Input Voltage | $V_I$ | -0.3 | | Vcc+0.5 | V | |
| Control Output Current | $I_O$ | -20 | | 20 | mA | |
| Signaling Speed Per Lane | DRL | | 53.125 | | GBd | |
| Operating Distance | | 2 | | 500 | m | |
| Data Rate | DR | | 850 | | Gbps | |

## Electrical Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Power Supply Voltage | | Vcc | 3.135 | 3.3 | 3.465 | V | |
| Instantaneous Peak Current at Hot Plug | | $I_{CC\_IP}$ | | | 6600 | mA | |
| Sustained Peak Current at Hot Plug | | $I_{CC\_SP}$ | | | 5494.5 | mA | |
| Maximum Power Dissipation | | PD | | | 16.5 | W | |
| Maximum Power Dissipation (Low-Power Mode) | | $PD_{LP}$ | | | 2 | W | |
| Control Input Voltage - High | | VIH | Vcc*0.7 | | Vcc+0.3 | V | |
| Control Input Voltage – Low | | VIL | -0.3 | | Vcc*0.3 | V | |
| 2-Wire Serial Interface Clock Rate | | | | | 400 | kHz | |
| Power Supply Noise (1kHz to 1MHz, Pk-Pk) | | | | | 66 | mVp-p | |
| **Transmitter (TP1)** | | | | | | | |
| Differential Pk-Pk Input Voltage Tolerance | | | 750 | | | mV | |
| Pk-Pk AC Common-Mode Voltage Tolerance | Low-Frequency ($VCM_{LF}$) | | | | 32 | mV | |
| | Full-Band ($VCM_{FB}$) | | | | 80 | mV | |
| Differential-Mode to Common-Mode Return Loss | | | | 802.3ck 120G-2 | | dB | |
| Effective Return Loss | | ERL | 8.5 | | | dB | |
| Differential Termination Mismatch | | | | | 10 | % | |
| Single-Ended Voltage Tolerance Range | | | -0.4 | | 3.3 | V | |
| DC Common-Mode Voltage Tolerance | | | -0.35 | | 2.85 | V | |
| **Receiver (TP4)** | | | | | | | |
| Pk-Pk AC Common-Mode Voltage | Low-Frequency ($VCM_{LF}$) | | | | 32 | mV | |
| | Full-Band ($VCM_{FB}$) | | | | 80 | mV | |
| Differential Pk-Pk | Short-Mode | | | | 600 | mV | |

| Output Voltage | Long-Mode | | | | 845 | mV | |
|---|---|---|---|---|---|---|---|
| Eye Height | | EH | 15 | | | mV | |
| Vertical Eye Closure | | VEC | | | 12 | dB | |
| Common-Mode to Differential-Mode Return Loss | | RLDc | 802.3ck 120G-1 | | | dB | |
| Effective Return Loss | | ERL | 8.5 | | | dB | |
| Differential Termination Mismatch | | | | | 10 | % | |
| Transition Time | | | 8.5 | | | ps | |
| DC Common-Mode Voltage Tolerance | | | -0.35 | | 2.85 | V | |

**Notes:**

1. Compliant with IEEE802.3ck C2M.

**Electrical Low-Speed Control and Sense Signal Specifications**

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Module Output SCL and SDA | VOL | 0 | 0.4 | V | |
| Module Input SCL and SDA | VIL | -0.3 | Vcc*0.3 | V | |
| | VIH | Vcc*0.7 | Vcc+0.5 | V | |
| InitMode, ResetL, and ModSelL | VIL | -0.3 | 0.8 | V | |
| | VIH | 2 | Vcc+0.3 | V | |
| IntL | VOL | 0 | 0.4 | V | |
| | VOH | Vcc-0.5 | Vcc+0.3 | V | |

## Optical Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | | |
| **Wavelength** | | λC | 1304.5 | 1311 | 1317.5 | nm | |
| **Side-Mode Suppression Ratio** | | SMSR | 30 | | | dB | |
| **Average Launch Power Per Lane** | | AOP$_L$ | -2.9 | | 4.0 | dBm | 1 |
| **Outer Optical Modulation Amplitude (OMAouter) Per Lane** | | TOMA | -0.8 | | 4.2 | dBm | |
| **Launch Power in OMAouter Minus TDECQ Per Lane** | **For ER ≥ 5dB** | TOMA - TDECQ | -2.2 | | | dBm | |
| | **For ER < 5dB** | TOMA - TDECQ | -1.9 | | | dBm | |
| **Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane** | | TDECQ | | | 3.4 | dB | |
| **TDECQ – 10log10(Ceq) Per Lane** | | Ceq | | | 3.4 | dB | |
| **Average Launch Power of Off Transmitter Per Lane** | | Toff | | | -15 | dBm | |
| **Extinction Ratio** | | ER | 3.5 | | | dB | |
| **Transmitter Transition Time** | | Tr | | | 17 | ps | |
| **RIN$_{15.5}$OMA** | | RIN | | | -136 | dB/Hz | |
| **Optical Return Loss Tolerance** | | ORLT | | | 15.5 | dB | |
| **Transmitter Reflectance** | | TR | | | -26 | dB | 2 |
| **Receiver (TP4)** | | | | | | | |
| **Wavelength** | | λC | 1304.5 | 1311 | 1317.5 | nm | |
| **Damage Threshold Per Lane** | | AOP$_D$ | 5 | | | dBm | |
| **Average Receive Power Per Lane** | | AOP$_R$ | -5.9 | | 4 | dBm | |
| **Receive Power (OMAouter) Per Lane** | | OMA$_R$ | | | 4.2 | dBm | |
| **Receiver Reflectance** | | RR | | | -26 | dB | |
| **Receiver Sensitivity (OMAouter) Per Lane** | | SOMA | | | Max. (−3.9, SECQ − 5.3) | dBm | 3 |
| **Stressed Receiver Sensitivity (OMAouter) Per Lane** | | SRS | | | -1.9 | dBm | 4 |
| **Conditions of Stressed Receiver Sensitivity Test** | | | | | | | |
| **Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test** | | SECQ | | 3.4 | | dB | |
| **SECQ – 10log10 (Ceq) Per Lane Under Test** | | Ceq | | | 3.4 | dB | |

**Notes:**
1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMAouter), per lane (maximum), is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.
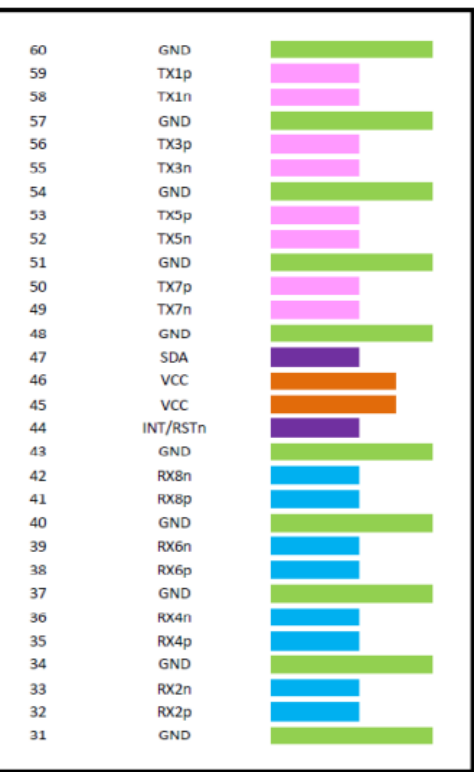4. Measured with conformance test signal at TP3 for the BER = $2.4 \times 10^{-4}$.

## Pin Descriptions

| Pin | Logic | Symbol | Name/Description | Notes |
|---|---|---|---|---|
| 1 | | GND | Module Ground. | |
| 2 | CML-I | Tx2+ | Transmitter Non-Inverted Data. | |
| 3 | CML-I | Tx2- | Transmitter Inverted Data. | |
| 4 | | GND | Module Ground. | |
| 5 | CML-I | Tx4+ | Transmitter Non-Inverted Data. | |
| 6 | CML-I | Tx4- | Transmitter Inverted Data. | |
| 7 | | GND | Module Ground. | |
| 8 | CML-I | Tx6+ | Transmitter Non-Inverted Data. | |
| 9 | CML-I | Tx6- | Transmitter Inverted Data. | |
| 10 | | GND | Module Ground. | |
| 11 | CML-I | Tx8+ | Transmitter Non-Inverted Data. | |
| 12 | CML-I | Tx8- | Transmitter Inverted Data. | |
| 13 | | GND | Module Ground. | |
| 14 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock. | |
| 15 | | Vcc | +3.3V Power Supply. | |
| 16 | | Vcc | +3.3V Power Supply. | |
| 17 | Multi-Level | LPWn/PRSn | Low-Power Mode/Module Present. | |
| 18 | | GND | Module Ground. | |
| 19 | CML-O | Rx7- | Receiver Inverted Data. | |
| 20 | CML-O | Rx7+ | Receiver Non-Inverted Data. | |
| 21 | | GND | Module Ground. | |
| 22 | CML-O | Rx5- | Receiver Inverted Data. | |
| 23 | CML-O | Rx5+ | Receiver Non-Inverted Data. | |
| 24 | | GND | Module Ground. | |
| 25 | CML-O | Rx3- | Receiver Inverted Data. | |
| 26 | CML-O | Rx3+ | Receiver Non-Inverted Data. | |
| 27 | | GND | Module Ground. | |
| 28 | CML-O | Rx1- | Receiver Inverted Data. | |
| 29 | CML-O | Rx1+ | Receiver Non-Inverted Data. | |
| 30 | | GND | Module Ground. | |
| 31 | | GND | Module Ground. | |
| 32 | CML-O | Rx2+ | Receiver Non-Inverted Data. | |
| 33 | CML-O | Rx2- | Receiver Inverted Data. | |
| 34 | | GND | Module Ground. | |
| 35 | CML-O | Rx4+ | Receiver Non-Inverted Data. | |
| 36 | CML-O | Rx4- | Receiver Inverted Data. | |

| | | | | |
|---|---|---|---|---|
| **37** | | GND | Module Ground. | |
| **38** | CML-O | Rx6+ | Receiver Non-Inverted Data. | |
| **39** | CML-O | Rx6- | Receiver Inverted Data. | |
| **40** | | GND | Module Ground. | |
| **41** | CML-O | Rx8+ | Receiver Non-Inverted Data. | |
| **42** | CML-O | Rx8- | Receiver Inverted Data. | |
| **43** | | GND | Module Ground. | |
| **44** | Multi-Level | INT/RSTn | Module Input/Module Reset. | |
| **45** | | Vcc | +3.3V Power Supply. | |
| **46** | | Vcc | +3.3V Power Supply. | |
| **47** | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data. | |
| **48** | | GND | Module Ground. | |
| **49** | CML-I | Tx7- | Transmitter Inverted Data. | |
| **50** | CML-I | Tx7+ | Transmitter Non-Inverted Data. | |
| **51** | | GND | Module Ground. | |
| **52** | CML-I | Tx5- | Transmitter Inverted Data. | |
| **53** | CML-I | Tx5+ | Transmitter Non-Inverted Data. | |
| **54** | | GND | Module Ground. | |
| **55** | CML-I | Tx3- | Transmitter Inverted Data. | |
| **56** | CML-I | Tx3+ | Transmitter Non-Inverted Data. | |
| **57** | | GND | Module Ground. | |
| **58** | CML-I | Tx1- | Transmitter Inverted Data. | |
| **59** | CML-I | Tx1+ | Transmitter Non-Inverted Data. | |
| **60** | | GND | Module Ground. | |

## Electrical Pad Layout

**Top Side (viewed from top)**

| Pin | Signal |
|-----|--------|
| 60 | GND |
| 59 | TX1p |
| 58 | TX1n |
| 57 | GND |
| 56 | TX3p |
| 55 | TX3n |
| 54 | GND |
| 53 | TX5p |
| 52 | TX5n |
| 51 | GND |
| 50 | TX7p |
| 49 | TX7n |
| 48 | GND |
| 47 | SDA |
| 46 | VCC |
| 45 | VCC |
| 44 | INT/RSTn |
| 43 | GND |
| 42 | RX8n |
| 41 | RX8p |
| 40 | GND |
| 39 | RX6n |
| 38 | RX6p |
| 37 | GND |
| 36 | RX4n |
| 35 | RX4p |
| 34 | GND |
| 33 | RX2n |
| 32 | RX2p |
| 31 | GND |

-------- Module Card Edge --------

**Bottom Side (viewed from bottom)**

| Signal | Pin |
|--------|-----|
| GND | 1 |
| TX2p | 2 |
| TX2n | 3 |
| GND | 4 |
| TX4p | 5 |
| TX4n | 6 |
| GND | 7 |
| TX6p | 8 |
| TX6n | 9 |
| GND | 10 |
| TX8p | 11 |
| TX8n | 12 |
| GND | 13 |
| SCL | 14 |
| VCC | 15 |
| VCC | 16 |
| LPWn/PRSn | 17 |
| GND | 18 |
| RX7n | 19 |
| RX7p | 20 |
| GND | 21 |
| RX5n | 22 |
| RX5p | 23 |
| GND | 24 |
| RX3n | 25 |
| RX3p | 26 |
| GND | 27 |
| RX1n | 28 |
| RX1p | 29 |
| GND | 30 |
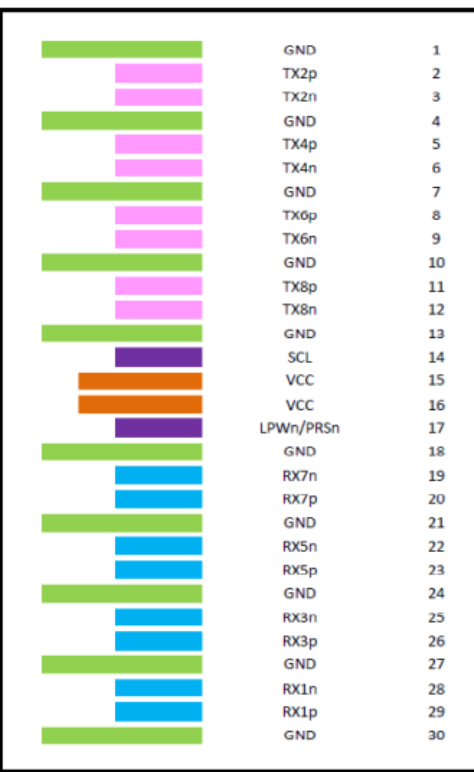
## Recommended OSFP Host Board Schematic
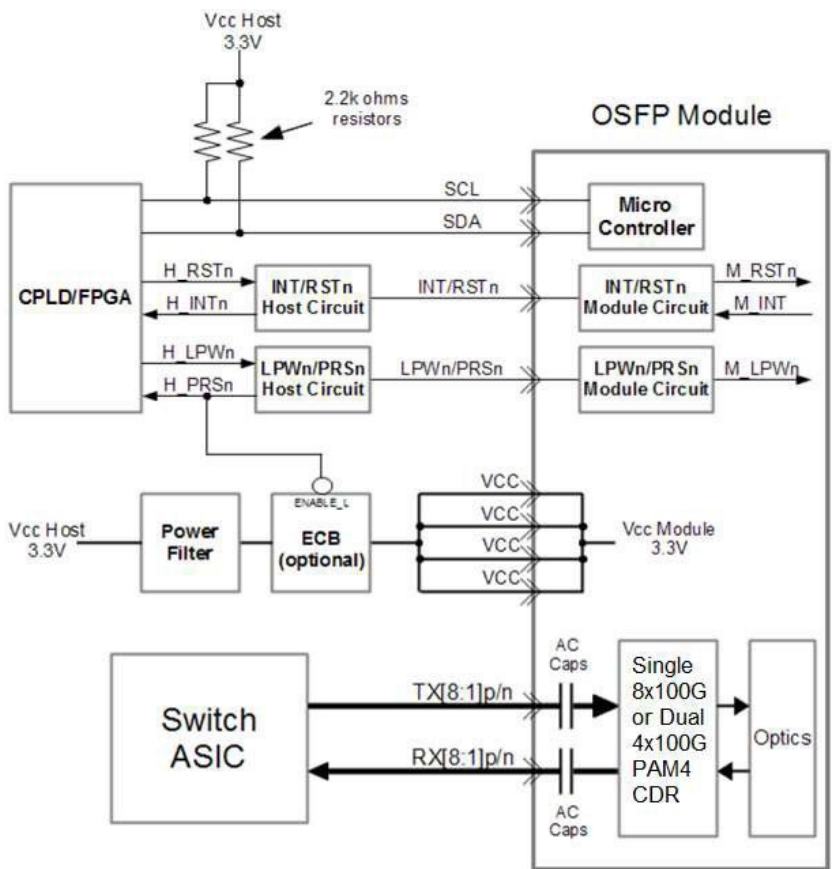
## Mechanical Specifications
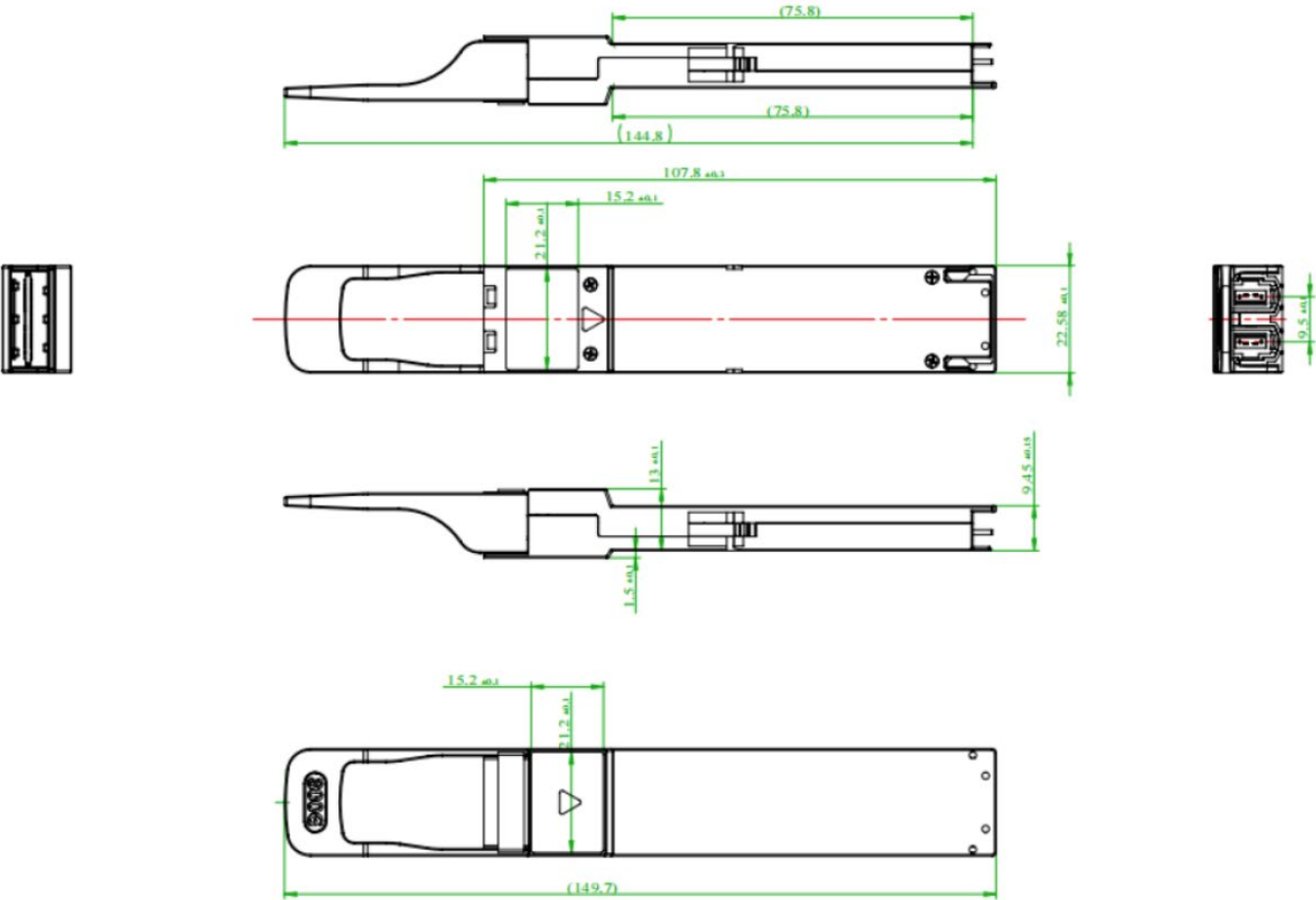
**OptioConnect**
**Innovation for the Future of High-Speed Networking**

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