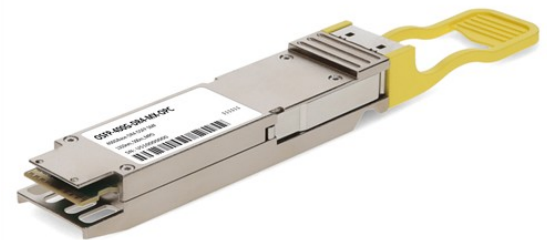


OSFP-400G-DR4-MX-OPC

Mellanox® Compatible TAA 400GBase-DR4 OSFP-IHS Transceiver (SMF, 1310nm, 500m, MPO, DOM)

Features

- MPO Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free



Applications:

- 400GBase Ethernet
- 1x Fibre Channel
- Access and Enterprise

Product Description

This Mellanox® compatible OSFP-IHS Transceiver provides 400GBase-DR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Mellanox®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	VCC	-0.5	3.6	V
Storage Temperature	Ts	-40	85	°C
Operating Case Temperature	Top	0	70	°C
Relative Humidity (non-condensing)	RH	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	TOP	0		70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		
Post-FEC Bit Error Ratio				1×10^{-12}		1
Link Distance	D	0.5		500	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Consumption				12	W	
Supply Current	I _{cc}			3.64	A	
Transmitter (each lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (V _{cm})	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Center Wavelength	λ_c	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125 $\pm$ 100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	Modulated
Average Launch Power, each Lane	PAVG	-2.9		4	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane	POMA	-0.8		4.2	dBm	2
Launch Power in OMA _{outer} minus TDECQ, each Lane		-2.2			dB	
Transmitter and Dispersion Eye Closer for PAM4, each Lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
RIN _{21.4} OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			21.4	dB	
Transmitter Reflectance	TR			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P _{off}			-15	dBm	
Receiver						
Data Rate, each Lane		53.125 $\pm$ 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH _d	5			dBm	3
Average Receive Power, each Lane		-5.9		4	dBm	4
Receive Power (OMA _{outer}), each Lane				4.2	dBm	
Receiver Sensitivity (OMA _{outer}), each Lane	SEN			-4.4	dBm	5
Stressed Receiver Sensitivity (OMA _{outer}), each Lane	SRS			-1.9	dBm	6
Receiver Reflectance	RR			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
OMA _{outer} of each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does

not ensure compliance.

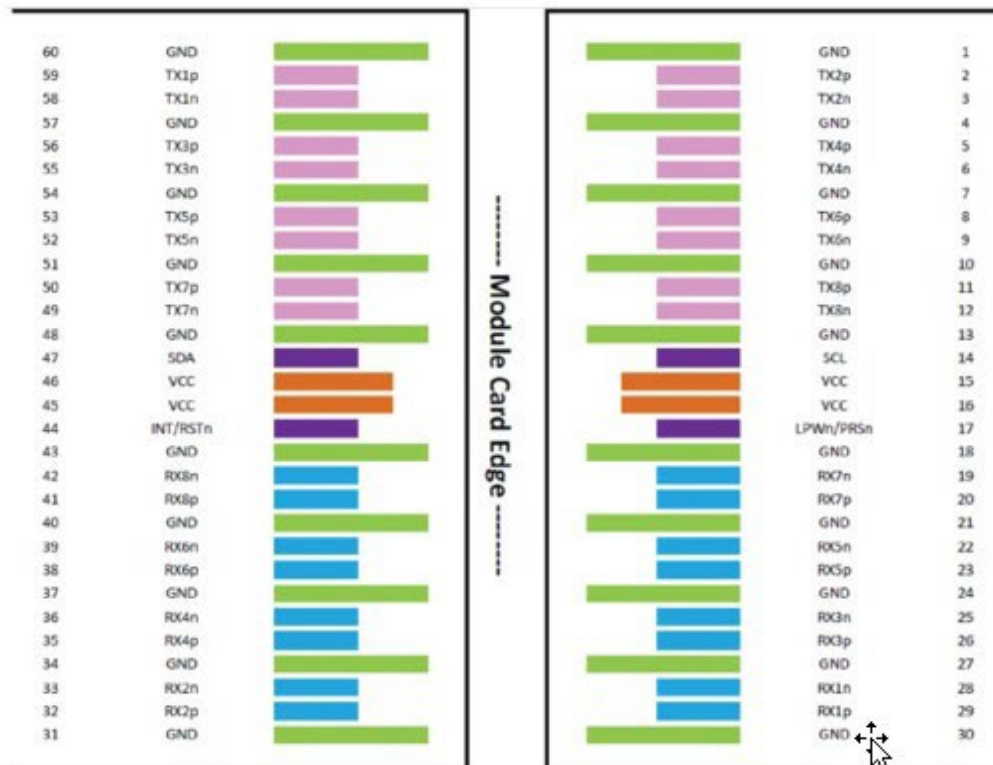
2. Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
6. Measured with conformance test signal for BER = 2.4×10^{-4} .
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Descriptions

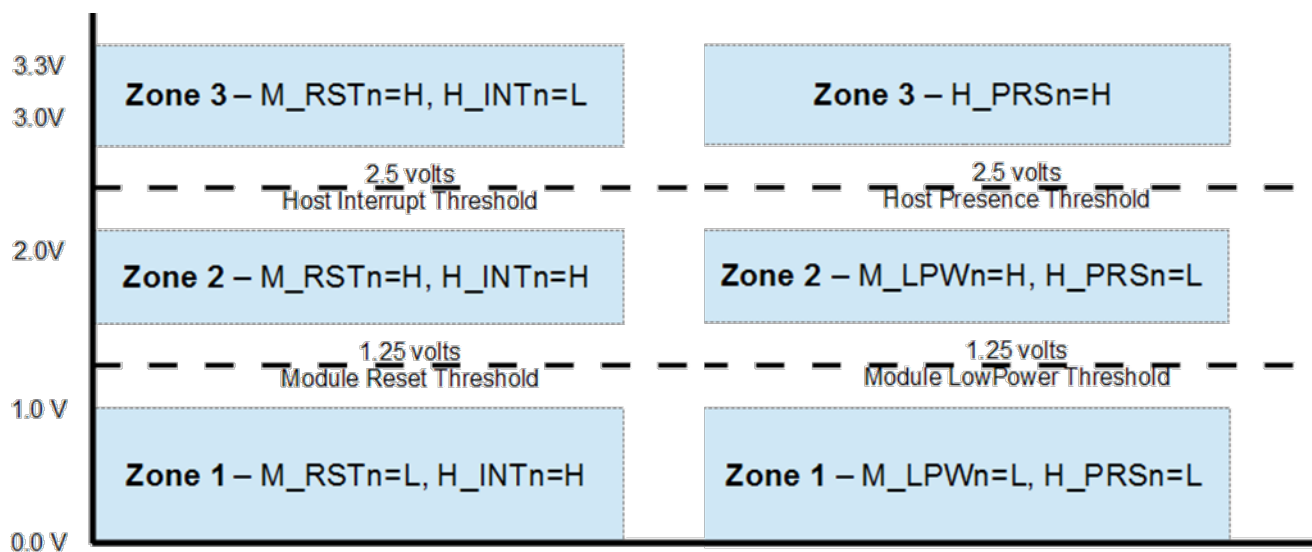
Pin	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVC MOS- I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1

41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS- I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

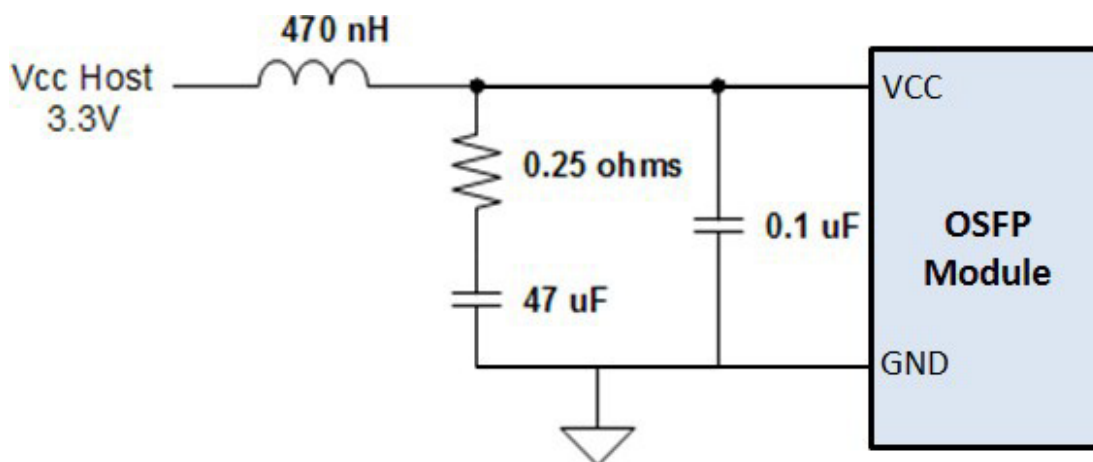
MSA Compliant Connector



Voltage Zones



Recommended Power Supply Filter



Digital Diagnostic Functions

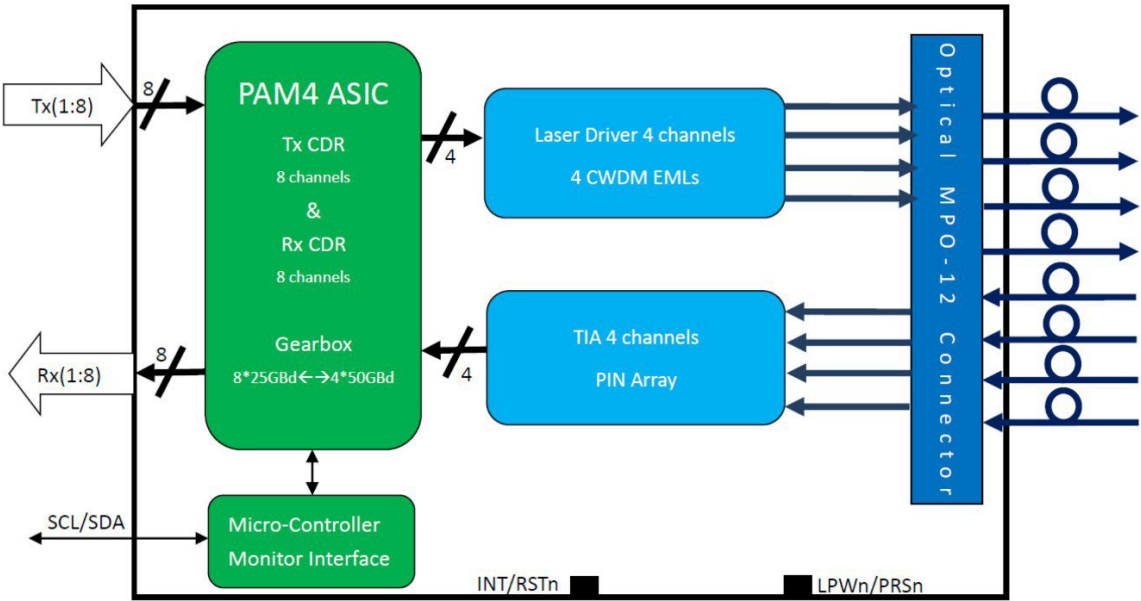
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

- 1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Transceiver Block Diagram



Mechanical Specifications

