MMS4X00-NM-T-OPC

Mellanox® MMS4X00-NM-T Compatible TAA 800GBase-DR8 PAM4 OSFP-IHS Transceiver (SMF, 1310nm, 500m, 2xMPO-12, DOM, CMIS 5.0)

Features

- OSFP MSA Compliant
- 8x53.125GBd (PAM4) Electrical Interface
- Supports 850Gbps
- Support both Ethernet and InfiniBand NDR
- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR optical interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M electrical interface
- Commercial Temperature: 0 to 70 Celsius
- EML transmitter and PIN PD receiver
- Dual MPO-12 Connector APC
- Class 1 Laser
- RoHS Compliant and Lead-Free

Applications:

- 8x100GBase Ethernet
- 2x400GBase Ethernet

Product Description

This Mellanox® MMS4X00-NM-T compatible OSFP-IHS Transceiver provides 800GBase-DR8 throughput up to 500m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO-12 connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Mellanox®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Relative Humidity (non-condensing)	RH	5		95	%	
Data Input Voltage Differential	V_{DIP}-V_{DIN}			1	V	
Control Input Voltage	V_I	-0.3		V_{CC}+0.5	V	
Control Output Current	I_O	-20		20	mA	
Signaling Speed per Lane	DRL		53.125		GBd	
Operating Distance		2		500	m	

Notes:

1. Exceeding the Absolute Maximum Ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under Absolute Maximum Ratings will affect the reliability of the device.

Electrical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage		Vcc	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug		I_{CC_IP}			6600	mA	
Sustained peak current at hot plug		I_{CC_SP}			5494.5	mA	
Maximum Power Dissipation		P_D			16.5	W	
Maximum Power Dissipation, Low Power Mode		P_{DLP}			2	W	
Control Input Voltage High		V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V	
Control Input Voltage Low		V_{IL}	-0.3		V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate					400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)					66	mVpp	
High-Speed Electrical Transmitter Characteristics (TP1)							
Differential Peak-Peak Input Voltage Tolerance			750			mV	
Peak-to-Peak AC Common-Mode Voltage Tolerance	**Low-frequency, VCM_{LF}**				32	mV	
	Full-band, VCM_{FB}				80	mV	
Differential-mode to common-mode return loss		RLcd	802.3ck 120G-2			dB	
Effective return loss		ERL	8.5			dB	
Differential termination mismatch					10	%	

Single-ended voltage tolerance range			-0.4		3.3	V	
DC common-mode voltage tolerance			-0.35		2.85	V	
High-Speed Electrical Receiver Characteristics (TP4)							
Peak-to-Peak AC Common-Mode Voltage	**Low-frequency, VCM_{LF}**				32	mV	
	Full-band, VCM_{FB}				80	mV	
Differential Peak-to-Peak Output Voltage	**Short Mode**				600	mV	
	Long Mode				845	mV	
Eye height		EH	15			mV	
Vertical eye closure		VEC			12	dB	
Common-mode to differential-mode return loss		RLDc	802.3ck 120G-1			dB	
Effective return loss		ERL	8.5			dB	
Differential termination mismatch					10	%	
Transition time			8.5			ps	
DC common-mode voltage tolerance			-0.35		2.85	V	

Notes:

1. Compliant with IEEE802.3ck C2M.

Electrical Low Speed Control and Sense Signals Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Module output SCL and SDA	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

Optical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter							
Wavelength		λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio		SMSR	30			dB	
Average Launch Power, each lane		AOPL	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane		TOMA	-0.8		4.2	dBm	
Launch power in OMAouter Minus TDECQ, each lane	**for extinction ratio >= 5dB**	TOMA-TDECQ	-2.2			dBm	
	for extinction ratio < 5dB	TOMA-TDECQ	-1.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane		TDECQ			3.4	dB	
TDECQ – 10log10(Ceq), each lane		Ceq			3.4	dB	
Average Launch Power of OFF Transmitter, each lane		TOFF			-15	dBm	
Extinction Ratio		ER	3.5			dB	
Transmitter Transition Time		Tr			17	ps	
$RIN_{15.5}OMA$		RIN			-136	dB/Hz	
Optical Return Loss Tolerance		ORL			15.5	dB	
Transmitter Reflectance		T_R			-26	dB	2
Receiver							
Wavelength		λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane		AOP_D	5			dBm	
Average Receive Power, each Lane		AOP_R	-5.9		4	dBm	
Receive Power (OMAouter), each Lane		OMA_R			4.2	dBm	
Receiver Reflectance		RR			-26	dB	
Receiver Sensitivity (OMAouter), each Lane		SOMA			Max (–3.9, SECQ – 5.3)	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane		SRS			-1.9	dBm	4
Conditions of Stressed Receiver Sensitivity Test							
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test		SECQ		3.4		dB	
SECQ – 10log10 (Ceq), Lane Under Test		Ceq			3.4	dB	

Notes:

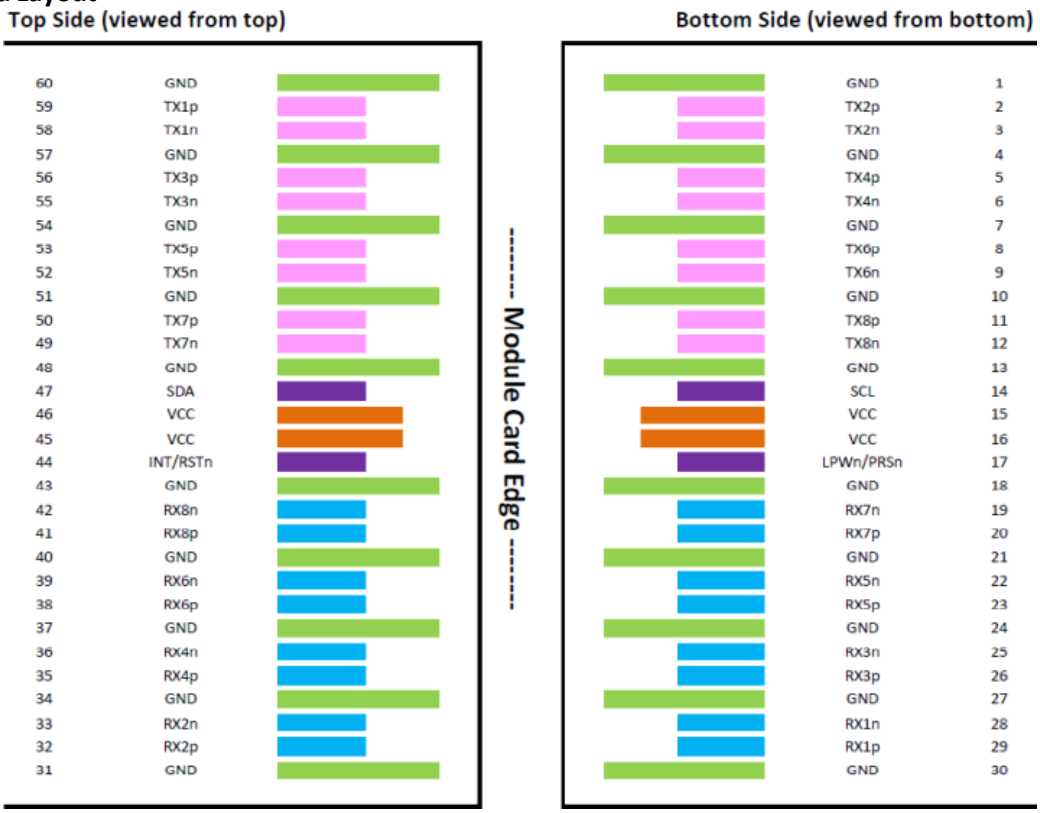
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}.

Pin Descriptions

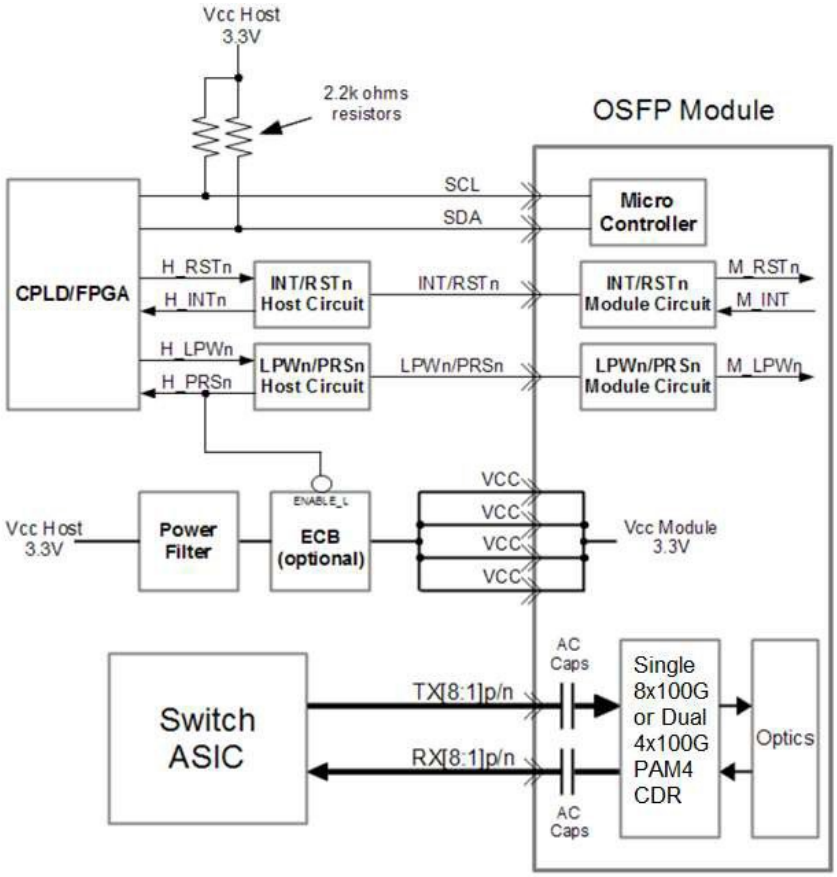
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	
2	CML-I	Tx2+	Transmitter Non-Inverted Data.	
3	CML-I	Tx2-	Transmitter Inverted Data.	
4		GND	Module Ground.	
5	CML-I	Tx4+	Transmitter Non-Inverted Data.	
6	CML-I	Tx4-	Transmitter Inverted Data.	
7		GND	Module Ground.	
8	CML-I	Tx6+	Transmitter Non-Inverted Data.	
9	CML-I	Tx6-	Transmitter Inverted Data.	
10		GND	Module Ground.	
11	CML-I	Tx8+	Transmitter Non-Inverted Data.	
12	CML-I	Tx8-	Transmitter Inverted Data.	
13		GND	Module Ground.	
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	
15		Vcc	+3.3V Power Supply.	
16		Vcc	+3.3V Power Supply.	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	
18		GND	Module Ground.	
19	CML-O	Rx7-	Receiver Inverted Data.	
20	CML-O	Rx7+	Receiver Non-Inverted Data.	
21		GND	Module Ground.	
22	CML-O	Rx5-	Receiver Inverted Data.	
23	CML-O	Rx5+	Receiver Non-Inverted Data.	
24		GND	Module Ground.	
25	CML-O	Rx3-	Receiver Inverted Data.	
26	CML-O	Rx3+	Receiver Non-Inverted Data.	
27		GND	Module Ground.	
28	CML-O	Rx1-	Receiver Inverted Data.	
29	CML-O	Rx1+	Receiver Non-Inverted Data.	
30		GND	Module Ground.	
31		GND	Module Ground.	
32	CML-O	Rx2+	Receiver Non-Inverted Data.	
33	CML-O	Rx2-	Receiver Inverted Data.	
34		GND	Module Ground.	
35	CML-O	Rx4+	Receiver Non-Inverted Data.	

36	CML-O	Rx4-	Receiver Inverted Data.	
37		GND	Module Ground.	
38	CML-O	Rx6+	Receiver Non-Inverted Data.	
39	CML-O	Rx6-	Receiver Inverted Data.	
40		GND	Module Ground.	
41	CML-O	Rx8+	Receiver Non-Inverted Data.	
42	CML-O	Rx8-	Receiver Inverted Data.	
43		GND	Module Ground.	
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	
45		Vcc	+3.3V Power Supply.	
46		Vcc	+3.3V Power Supply.	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	
48		GND	Module Ground.	
49	CML-I	Tx7-	Transmitter Inverted Data.	
50	CML-I	Tx7+	Transmitter Non-Inverted Data.	
51		GND	Module Ground.	
52	CML-I	Tx5-	Transmitter Inverted Data.	
53	CML-I	Tx5+	Transmitter Non-Inverted Data.	
54		GND	Module Ground.	
55	CML-I	Tx3-	Transmitter Inverted Data.	
56	CML-I	Tx3+	Transmitter Non-Inverted Data.	
57		GND	Module Ground.	
58	CML-I	Tx1-	Transmitter Inverted Data.	
59	CML-I	Tx1+	Transmitter Non-Inverted Data.	
60		GND	Module Ground.	

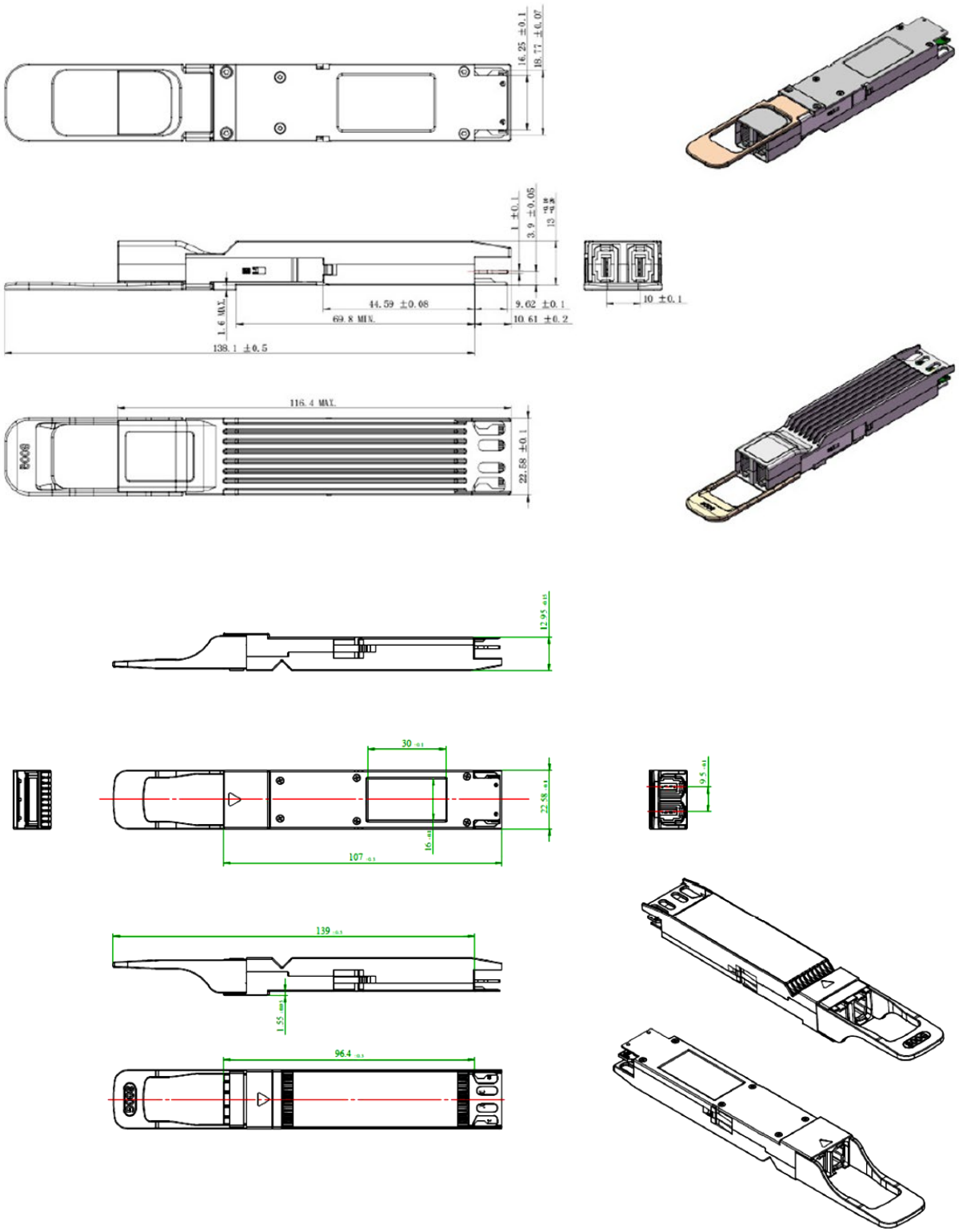
Electrical Pad Layout



Recommended OSFP Host board Schematic



Mechanical Specifications



*Note: Both Heat Sink Exposed and Heat Sink Enclosed styles are OSFP Type 2 Compliant. Images are for Illustration purposes only. Product Labels, colors, and style may vary.