F5-UPG-XFP-R-OPC

F5 Networks® F5-UPG-XFP-R Compatible TAA 10GBase-SR XFP Transceiver (MMF, 850nm, 300m, LC, DOM)

Features

- INF-8077i Compliance
- Duplex LC Connector
- VCSEL transmitter and PIN receiver
- Multi-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS Compliant and Lead Free

Applications:

- 10GBase-SR Ethernet
- 8x/10x Fibre Channel
- Access, Datacenter and Enterprise
- Mobile Fronthaul CPRI/OBSAI

Product Description

This F5 Networks® F5-UPG-XFP-R compatible XFP transceiver provides 10GBase-SR throughput up to 300m over multi-mode fiber (MMF) using a wavelength of 850nm via an LC connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with F5 Networks®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Maximum Supply Voltage	Vcc3	-0.5	3.6	V
	Vcc5	-0.5	6	V
Storage Temperature	TS	-40	85	°C
Operating Temperature	TO	-5	70	°C
Operating Humidity	RH	5	85	%
Receiver power	R_{MAX}		-1	dBm
Maximum bitrate	B_{max}		11.3	Gbps

Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc3	3.15	3.30	3.43	V	
	Vcc5	4.75	5.0	5.25	V	
Power Supply Current	Icc			455	mA	
Power Consumption	P_{DISS}			1.5	W	
Transmitter						
Differential data input swing	Vin, pp	120		850	mV	
Input differential impedance	Zin	80	100	120	Ω	
Receiver						
Differential data output swing	Vout, pp	300		850	mV	
Output differential impedance	Zin	80	100	120	Ω	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Optical Power (average)	P_{AVE}	-7.3		-1.2	dBm	1
Optical Modulation amplitude (OMA)	P_{OMA}	-1.5			dBm	2
Optical Extinction Ratio	ER	3			dB	
Optical Wavelength	Tλ	840	850	860	nm	
Insertion loss	IL		1			
Receiver						
Receiver Sensitivity (average)	R_{AVE}			-9.9	dBm	3
Receiver Sensitivity (OMA)	R_{OMA}			-11.1		2
Receiver overload	P_{max}	-1			dBm	4
Receiver wavelength	Rλ	840		860	nm	

Notes:

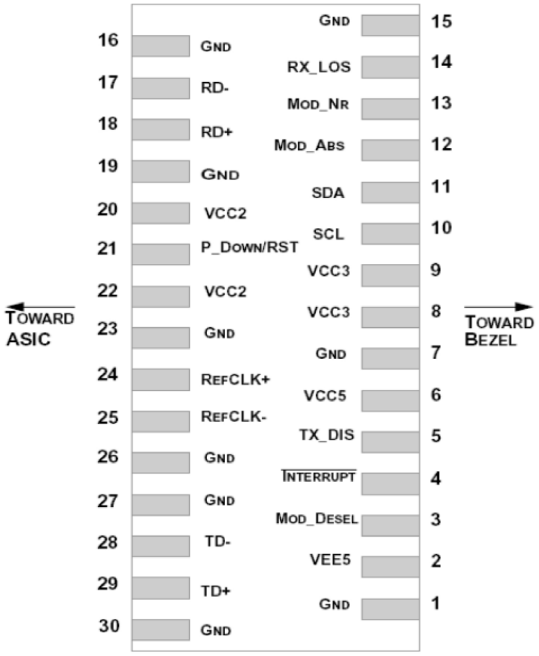
1. Coupled into a Multimode fibre
2. Per IEEE 802.3ae specification
3. Average power, back-to-back, @10.31Gbps, BER 1E-12, PRBS 231-1.
4. Exceeding the Receiver overload can physically damage the module. Please use appropriate attenuation.

Pin Descriptions

Pin	Symbol	Name/Descriptions	Ref.
1	GND	Module Ground	
2	Vee5	(not required)	
3	MOD_DESEL	Module De-select; When Held low allows the module to respond to 2-wire serial interface. LVTTL-I	
4	/INTERRUPT	Interrupt; Indicates presence of an important condition which can be read via the 2-wire serial interface. LVTTL-O	2
5	TX_DIS	Transmitter Disable. Logic1 indicates laser output disabled, LVTTL-I	
6	VCC5	+5V Power Supply (Not required)	
7	GND	Module Ground	1
8	VCC3	+3.3V Power Supply	
9	VCC3	+3.3V Power Supply	
10	SCL	2-Wire Serial Interface Clock. LVTTL-I	2
11	SDA	2-Wire Serial Interface Data Line. LVTTL-I/O	2
12	MOD_Abs	Indicates Module is not present. Grounded in the Module. LVTTL-O	2
13	MOD_NR	Module Not Ready; Indicating Module Operational Fault. Open-collector. LVTTL-O	2
14	RX_LOS	Loss of Signal indication. Logic 1 indicates loss of Signal. Open-collector. LVTTL-O	2
15	GND	Module Ground	1
16	GND	Module Ground	1
17	RD-	Receiver Inverted Data Output. CML-O	
18	RD+	Receiver Non-Inverted Data Output. CML-O	
19	GND	Module Ground	1
20	VCC2	+1.8V Power Supply (Not required).	3
21	P_DOWN/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. LVTTL-I Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle. LVTTL-I	
22	VCC2	+1.8V Power Supply (Not required)	3
23	GND	Module Ground	1
24	REFCLK+	Reference Clock (Not required)	
25	REFCLK-	Reference Clock (Not required)	
26	GND	Module Ground	1
27	GND	Module Ground	1
28	TD-	Transmitter Inverted Data Input. CML-I	
29	TD+	Transmitter Non-Inverted Data Input. CML-I	
30	GND	Module Ground	1

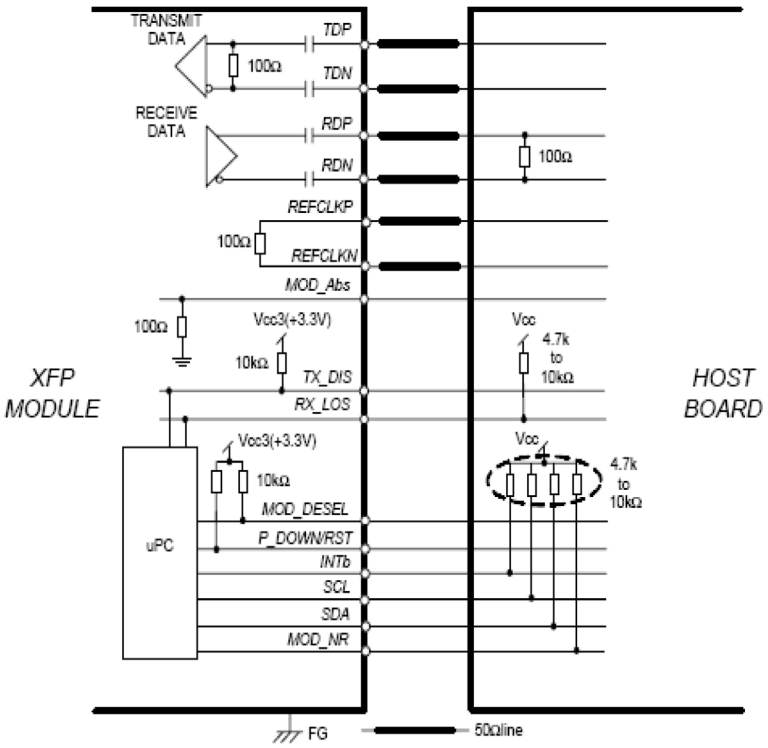
Notes:

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Open collector; should be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.6V on the host board.
3. The pins are open within module.



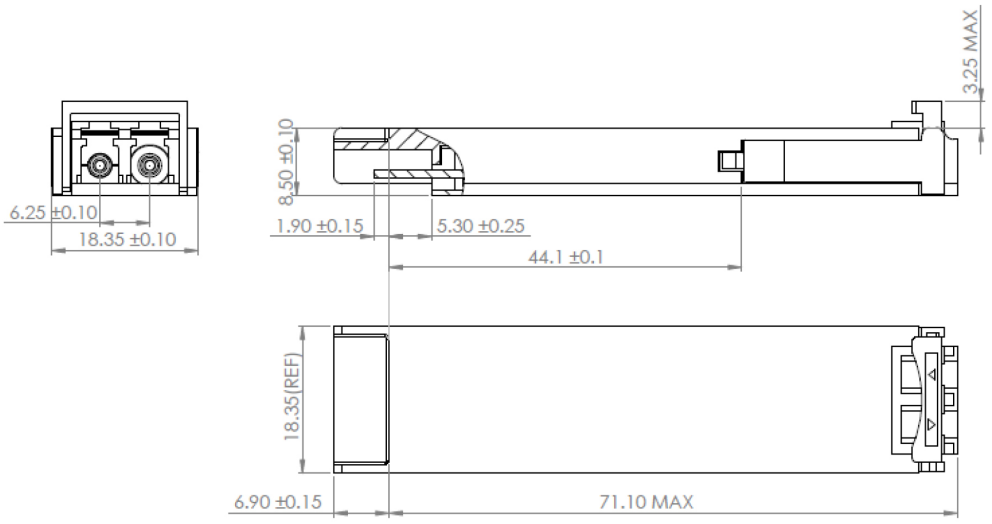
Pin-out of connector Block on Host board

Recommended Circuit Schematic



Mechanical Specifications

Small Form Factor Pluggable (XFP) transceivers are compatible with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).



EEPROM Information

Management Interface

XFP 2-wire serial interface is specified in the Chapter 4 of the XFP MSA specification. The XFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all XFP modules. The 2-wire serial interface address of the XFP module is 1010000X(A0h). In order to access to multiple modules on the same 2-wire serial bus, the XFP has a MOD_DESEL(module deselect pin). This pin (which is pull high or deselected in the module) must be held low by the host to select of interest and allow communication over 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

XFP Management Interface

XFP Management interface is specified in the Chapter 5 of the XFP MSA specification. The Figure 1 shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

EEPROM memory map specific data field description is as below: