QSFP28-100GB-SR4-LP-CX-OPC

Calix® Compatible TAA 100GBase-SR4 QSFP28 Transceiver Low Power (MMF, 850nm, 100m, MPO, DOM, 0 to 70C)

Features

- Up to 28.05 Gbps data rate per channel
- Compliant with QSFP28 MSA
- High Reliability 850nm VCSEL technology
- Digital diagnostic SFF-8636 compliant
- Compliant to IEEE 802.3bm
- Standard 12-lane with MPO connector
- Power Dissipation:
- Commercial Temperature 0 to 70 Celsius
- Hot Pluggable
- RoHS Compliant and lead-free

Applications:

- 100GBase Ethernet
- Access and Enterprise

Product Description

This Calix® compatible QSFP28 transceiver provides 100GBase-SR4 throughput up to 100m over OM4 multi-mode fiber (MMF) using a wavelength of 850nm via an MPO connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Calix®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.3		4	V	
Storage Temperature	Tstg	-40		85	°C	
Case Operating Temperature	Tc	0		70	°C	Without Air Flow
Relative Humidity	RH	5		95	%	
Signal Input Voltage		Vcc-0.3		Vcc+0.3	V	
Data Rate	BR		25.78125	28.05	Gbps	Each Channel
Transmission Distance	TD			100	m	1

Notes:

1. OM4, or 70m on OM3.
2. 100GBase-SR4 and ITU-T OTU4 have different register settings not auto-negotiation.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.14	3.3	3.46	V	
Power Supply Current	Icc			600	mA	
Transmitter						
Input Differential Impedance	RIN		100		Ω	1
Differential Data Input Swing	VIN,pp	180		1000	mV	
Single-Ended Input Voltage Tolerance	VIN	-0.3		4.0	V	
Receiver						
Differential Data Output Swing	VOUT,pp	300		850	mV	2
Single-Ended Output Voltage		-0.3		4.0	V	

Notes:

1. Connected directly to Tx data input pins. AC coupled thereafter.
2. Into 100Ω differential termination.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λC	840		860	nm	
Average Launch Power Per Lane		-8.4		2.4	dBm	
Spectral Width (RMS)	σ			0.6	nm	
Optical Extinction Ratio	ER	2			dB	
Optical Return Loss Tolerance	ORLT			12	dB	
Output Eye Mask	Compliant with IEEE 802.3bm					1
Receiver						
Receiver Wavelength	λ	840		860	nm	
Rx Sensitivity Per Lane	RSENS			-10.3	dBm	2
LOS De-Assert	LOSD	-30			dBm	
LOS Assert	LOSA			-12	dBm	
Input Saturation Power (Overload)	Psat	2.4			dBm	
Receiver Reflectance				-12	dB	

Notes:

1. Hit ratio $1.5*10^{-5}$ hits per sample.
2. Measured with a PRBS 2^{31}-1 test pattern, @25.78Gbps, and BER<$5.0*10^{-5}$.

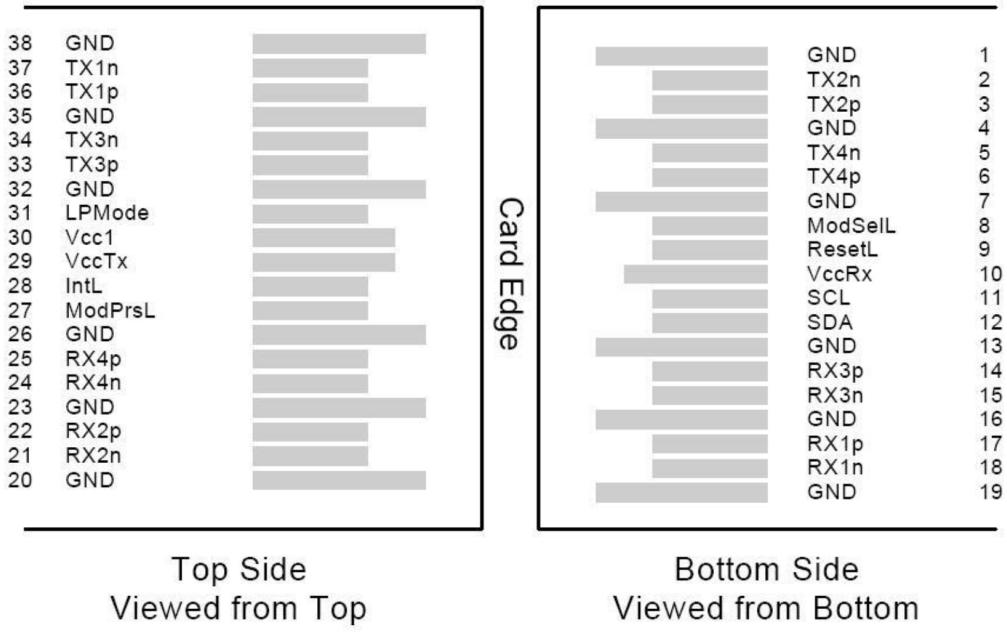
Pin Descriptions

Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground.	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	
4		GND	Module Ground.	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	
7		GND	Module Ground.	1
8	LVTTL-I	MODSEIL	Module Select.	2
9	LVTTL-I	ResetL	Module Reset.	2
10		VccRx	+3.3V Receiver Power Supply.	
11	LVCMOS-I	SCL	2-Wire Serial Interface Clock.	2
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	2
13		GND	Module Ground.	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3-	Receiver Inverted Data Output.	
16		GND	Module Ground.	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output	
18	CML-O	Rx1-	Receiver Inverted Data Output.	
19		GND	Module Ground.	1
20		GND	Module Ground.	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	
23		GND	Module Ground.	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	
26		GND	Module Ground.	1
27	LVTTL-O	ModPrsL	Module Present. Internally pulled down to GND.	
28	LVTTL-O	IntL	Interrupt output should be pulled up on the host board.	2
29		VccTx	+3.3V Transmitter Power Supply.	
30		Vcc1	+3.3V Power Supply.	
31	LVTTL-I	LPMode	Low-Power Mode.	2
32		GND	Module Ground.	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	
35		GND	Module Ground.	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	
38		GND	Module Ground.	1

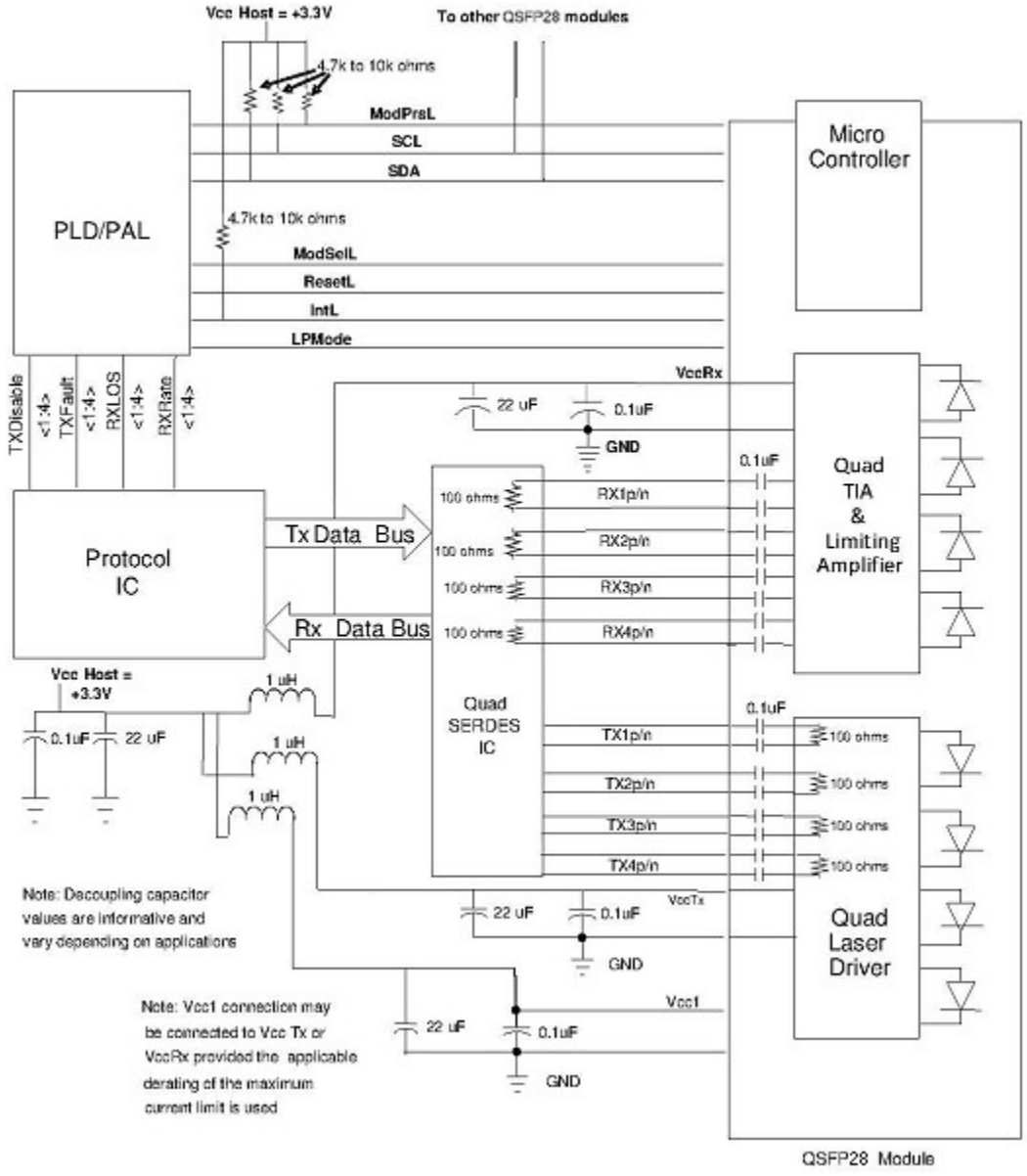
Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector. Should be pulled up with 4.7kΩ-10kΩ on the host board to a voltage between 3.15V and 3.6V.

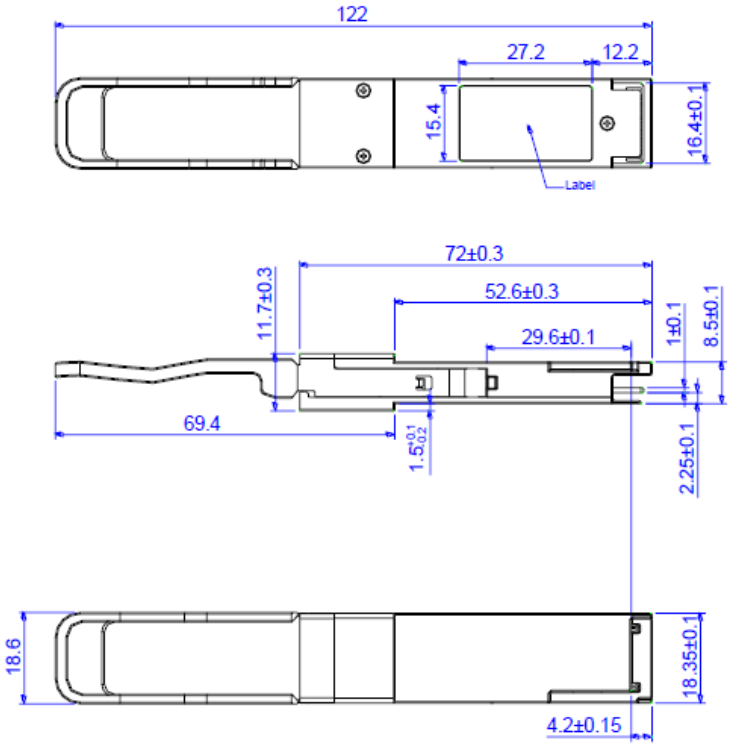
Electrical Pin-Out Details

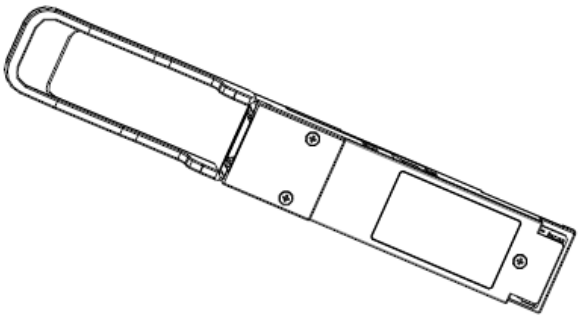


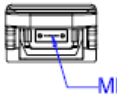
Transceiver Interface Block Diagram



Mechanical Specifications







Units in mm