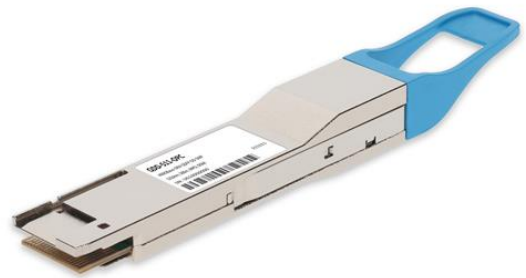


QDD-511-OPC

Gigamon Systems® QDD-511 Compatible TAA 400GBase-DR4 QSFP-DD Transceiver (SMF, 1310nm, 500m, MPO, DOM, CMIS 4.0)

Features

- Compliant with IEEE802.3bs Standard: 400GAUI-8 Electrical Interface
- Compliant with IEEE 802.3bs Standard: 400GBASE-DR4 Optical Interface
- QSFP-DD MSA Compliant
- MPO-12 Connector
- CMIS 4.0
- Class 1 Laser
- Operating Temperature: 0 to 70 Celsius
- RoHS Compliant and Lead-Free
- RoHS compliant and Lead Free
- Excellent ESD Protection
- RoHS Compliant and Lead Free



Applications:

- 400GBase Ethernet
- Access and Enterprise

Product Description

This Gigamon Systems® QDD-511 compatible QSFP-DD transceiver provides 400GBase-DR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Gigamon Systems®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0	25	70	°C	
Supply Voltage	Vcc	-0.5		3.6	V	
Relative Humidity	RH	5		95	%	
Operating Distance		2		500	m	
Signaling Speed Per Lane	DRL		53.125		GBd	PAM4
Maximum Power Dissipation	PD			9	W	
Maximum Power Dissipation (Low-Power Mode)	PDLP			2	W	
Rx Differential Data Output Load			100		Ω	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Control Input Voltage	V _I	-0.3		V _{CC} +0.5	V	
Instantaneous Peak Current at Hot Plug	I _{CC_IP}			3600	mA	
Sustained Peak Current at Hot Plug	I _{CC_SP}			2970	mA	
2-Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise (10Hz-10MHz)				66	mVp-p	
Transmitter - Module Input						
Differential Pk-Pk Input Voltage Tolerance		900			mV	
Differential Termination Mismatch				10	%	
Single-Ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common-Mode Voltage		-350		2850	mV	
Receiver - Module Output						
AC Common-Mode Output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Differential Near-End Eye Height		70			mV	
Differential Far-End Eye Height		30			mV	
Far-End Pre-Cursor Ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (Minimum, 20-80%)		9.5			ps	
DC Common-Mode Voltage		-350		2850	mV	
Low-Speed Control and Sense Signals						
Module Output SCL and SDA	V _{OL}	0		0.4	V	
Module Input SCL and SDA	V _{IL}	-0.3		V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7		V _{CC} +0.5	V	
InitMode, ResetL, and ModSelL	V _{IL}	-0.3		0.8	V	
	V _{IH}	2		V _{CC} +0.3	V	
IntL	V _{OL}	0		0.4	V	
	V _{OH}	V _{CC} -0.5		V _{CC} +0.3	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	P	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}) Per Lane	TOMA	-0.8		4.2	dBm	2
Launch Power in OMA _{outer} Minus TDECQ Per Lane	TOMA	-2.2			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane	TDECQ			3.4	dB	
TDECQ-TECQ 10log10 (Ceq)				3.4	dB	
Average Launch Power of Off Transmitter Per Lane	T _{off}			-15	dBm	
Extinction Ratio Per Lane	ER	3.5			dB	
Transmitter Transition Time				17	ps	
RIN _{21.4OMA}	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORLT			21.4	dB	
Transmitter Reflectance	TR			-26	dB	3
Receiver						
Center Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold Per Lane		5			dBm	
Average Receiver Power Per Lane	P _{avg}	-5.9		4.0	dBm	1
Receive Power Per Lane (OMA _{outer})				4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity Per Lane (OMA _{outer})	SOMA			-4.4	dBm	2
Stressed Receiver Sensitivity Per Lane (OMA _{outer})	SRS			-1.9	dBm	3
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test			3.4		dB	
SECQ -10log10 (Ceq) Per Lane Under Test				3.4	dB	
OMA _{outer} of Each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength.
2. Even if TDECQ < 1.4dB, OMA_{outer} (minimum) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Average receive power, per lane (minimum), is informative and not the principal indicator of signal strength.
5. Receiver sensitivity (OMA_{outer}), per lane (maximum), is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.

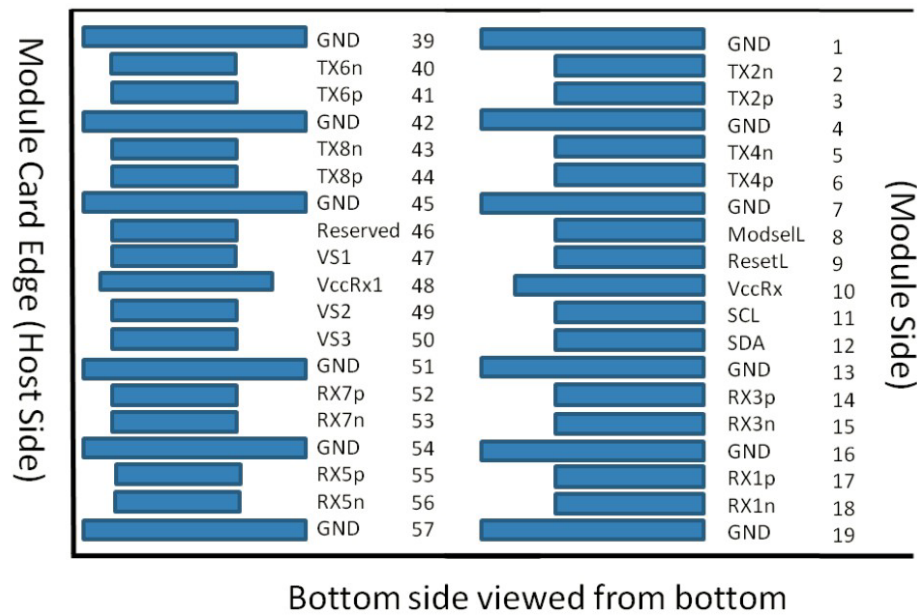
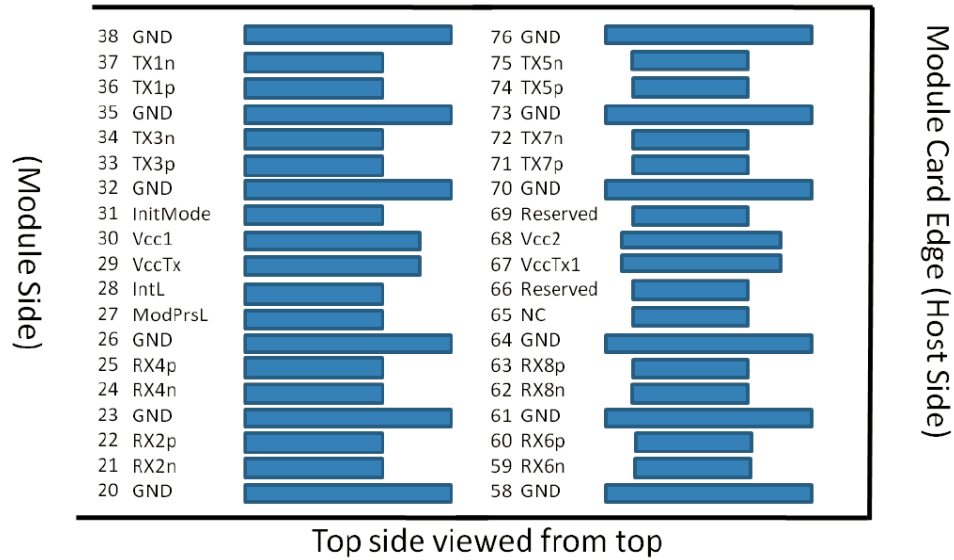
6. Measured with conformance test signals at TP3 for the $BER=2.4 \times 10^{-4}$.

Pin Descriptions

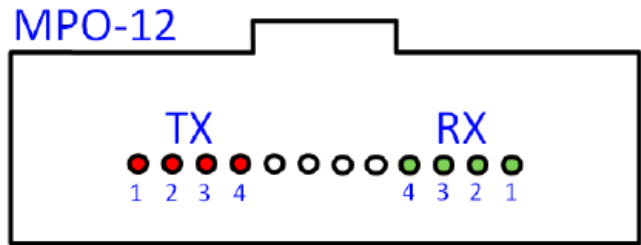
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	
2	CML-I	Tx2-	Transmitter Inverted Data Input.	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	
4		GND	Module Ground.	
5	CML-I	Tx4-	Transmitter Inverted Data Input.	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	
7		GND	Module Ground.	
8	LVTTTL-I	ModSelL	Module Select.	
9	LVTTTL-I	ResetL	Module Reset.	
10		VccRx	+3.3V Receiver Power Supply.	
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	
13		GND	Module Ground.	
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3-	Receiver Inverted Data Output.	
16		GND	Module Ground.	
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	
18	CML-O	Rx1-	Receiver Inverted Data Output.	
19		GND	Module Ground.	
20		GND	Module Ground.	
21	CML-O	Rx2-	Receiver Inverted Data Output.	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	
23		GND	Module Ground.	
24	CML-O	Rx4-	Receiver Inverted Data Output.	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	
26		GND	Module Ground.	
27	LVTTTL-O	ModPrsL	Module Present.	
28	LVTTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Transmitter Power Supply.	
30		Vcc1	+3.3V Power Supply.	
31	LVTTTL-I	InitMode	Initialization Mode.	
32		GND	Module Ground.	
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	
35		GND	Module Ground.	
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1-	Transmitter Inverted Data Output.	
38		GND	Module Ground.	

39		GND	Module Ground.	
40	CML-I	Tx6-	Transmitter Inverted Data Input.	
41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	
42		GND	Module Ground.	
43	CML-I	Tx8-	Transmitter Inverted Data Input.	
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	
45		GND	Module Ground.	
46		Reserved		
47		VS1	Module Vendor-Specific 1.	
48		VccRx1	+3.3V Receiver Power Supply.	
49		VS2	Module Vendor-Specific 2.	
50		VS3	Module Vendor-Specific 3.	
51		GND	Module Ground.	
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	
53	CML-O	Rx7-	Receiver Inverted Data Output.	
54		GND	Module Ground.	
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	
56	CML-O	Rx5-	Receiver Inverted Data Output.	
57		GND	Module Ground.	
58		GND	Module Ground.	
59	CML-O	Rx6-	Receiver Inverted Data Output.	
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	
61		GND	Module Ground.	
62	CML-O	Rx8-	Receiver Inverted Data Output.	
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	
64		GND	Module Ground.	
65		NC	Not Connected.	
66		Reserved		
67		VccTx1	+3.3V Transmitter Power Supply.	
68		Vcc2	+3.3V Power Supply.	
69		Reserved		
70		GND	Module Ground.	
71	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	
72	CML-I	Tx7-	Transmitter Inverted Data Input.	
73		GND	Module Ground.	
74	CML-I	Tx5+	Transmitter Non-Inverted Data Input.	
75	CML-I	Tx5-	Transmitter Inverted Data Input.	
76		GND	Module Ground.	

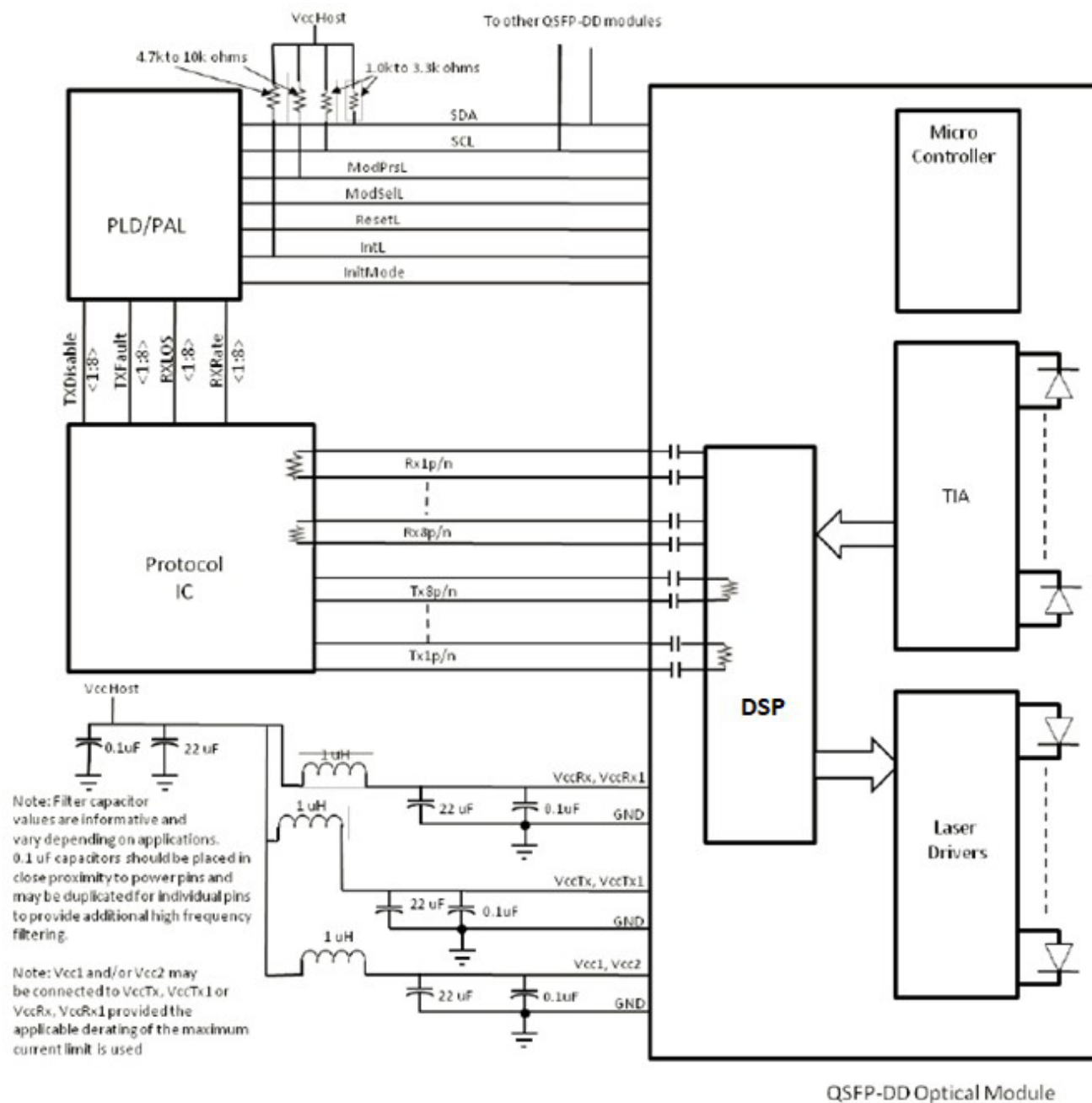
Electrical Pin-Out Details



Active Fiber Ports in MPO-12 Connector on Module Side



Host Board Schematic



Mechanical Specifications

