JL856A-OPC

HP® JL856A Compatible TAA Compliant 100GBase-AOC QSFP28 to QSFP28 Active Optical Cable (850nm, MMF, 2m)

Features

- QSFP28 MSA compliant
- Four independent full-duplex channels
- Supports 103.1Gbps aggregate bit rate
- Operating case temperature: 0 to 70 Celsius
- 4x25G electrical interface (OIF CEI-28G-VSR)
- Single 3.3V power supply
- Maximum power consumption 2.5W each terminal
- RoHS Compliant and Lead Free

Applications:

- 100GBase Ethernet
- InfiniBand EDR

Product Description

This is a HP® JL856A compatible 100GBase-AOC QSFP28 to QSFP28 active optical cable that operates over multi-mode fiber with a maximum reach of 2.0m (6.6ft). At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Tstg	-40		85	˚C
Operating Case Temperature	Tc	0		70	
Power Supply Voltage	Vcc	-0.5		3.6	V
Relative Humidity (Non-Condensing)	RH	0		85	%

Electrical Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes
Power Consumption				2.5	W	1
Supply Current	Icc			757	mA	1
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Data Rate Per Lane			25.78125		Gbps	
Data Rate Accuracy		-100		100	ppm	
Control Input Voltage - High		2		Vcc	V	
Control Input Voltage - Low		0		0.8	V	
Transmitter (Per Lane)						
Overload Differential Voltage	TP1a	900			mV	
Common-Mode Voltage (Vcm)	TP1	-350		2825	mV	2
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz
Differential Return Loss (SDD11)	TP1			See CEI-28G0VSR Equation 13-19	dB	
Common-Mode to Differential Conversion and Differential to Common-Mode Conversion	TP1			See CEI-28G-VSR Equation 13-20	dB	
Stressed Input Test	TP1a	See CEI-28G-VSR Section 13.3.11.2.1				
Receiver (Per Lane)						
Differential Voltage (Pk-Pk)	TP4			900	mV	
Common-Mode Voltage (Vcm)	TP4	-350		2850	mV	2
Common-Mode Noise (RMS)	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHz

Differential Return Loss (SDD22)	TP4			See CEI-28G-VSR Equation 13-19	dB	
Common-Mode to Differential Conversion and Differential to Common-Mode Conversion (SCC22)	TP4			-2	dB	3
Transition Time (20-80%)	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10^{-15} Probability (EW15)	TP4	0.57			UI	
Eye Height at 10^{-15} Probability (EH15)	TP4	0.57			UI	

Notes:

1. Per terminal.
2. Vcm is generated by the host. Specification includes the effects of ground offset voltage.
3. From 250MHz to 30GHz.

Pin Descriptions

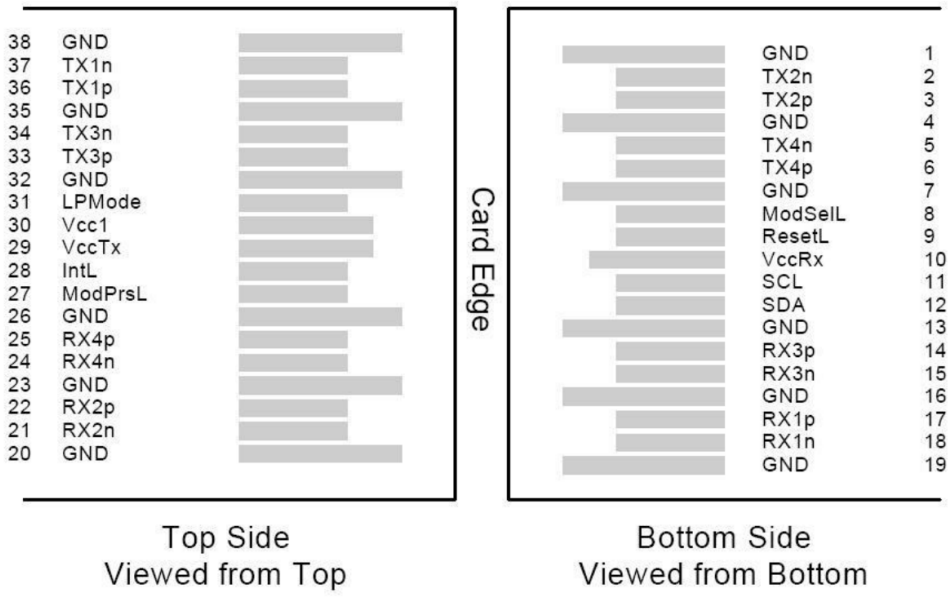
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	
4		GND	Module Ground.	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	
7		GND	Module Ground.	1
8	LVTTL-I	ModSelL	Module Select.	2
9	LVTTL-I	ResetL	Module Reset.	2
10		VccRx	+3.3V Receiver Power Supply.	
11	LVCMOS-I	SCL	2-Wire Serial Interface Clock.	2
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	2
13		GND	Module Ground.	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3-	Receiver Inverted Data Output.	
16		GND	Module Ground.	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	
18	CML-O	Rx1-	Receiver Inverted Data Output.	
19		GND	Module Ground.	1
20		GND	Module Ground.	1

21	CML-O	Rx2-	Receiver Inverted Data Output.	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	
23		GND	Module Ground.	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	
26		GND	Module Ground.	1
27	LVTTL-O	ModPrsL	Module Present. Internally pulled down to the GND.	
28	LVTTL-O	IntL	Interrupt output should be pulled up on the host board.	2
29		VccTx	+3.3V Transmitter Power Supply.	
30		Vcc1	+3.3V Power Supply.	
31	LVTTL-I	LPMode	Low-Power Mode.	2
32		GND	Module Ground.	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	
35		GND	Module Ground.	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	
38		GND	Module Ground.	1

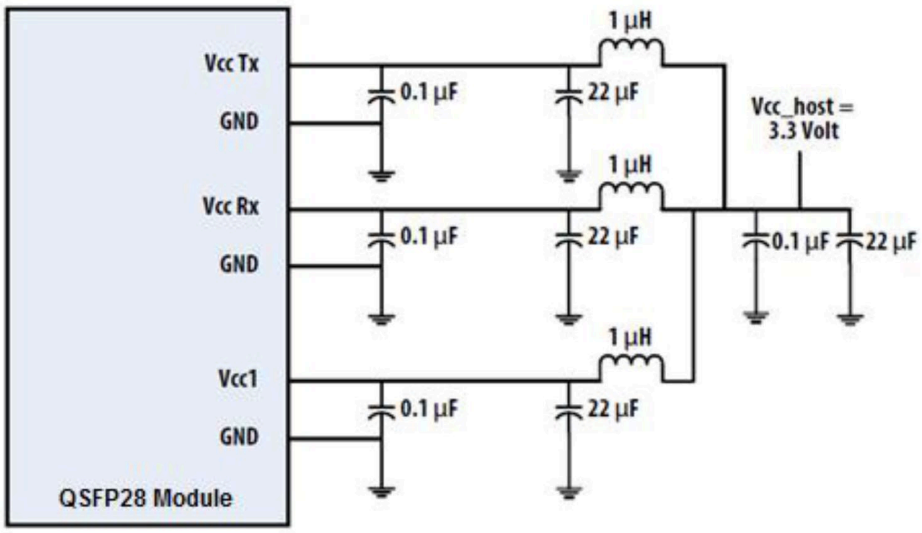
Notes:

1. The module circuit ground is isolated from the module chassis ground within the module.
2. Open collector. Should be pulled up with 4.7kΩ to 10kΩ on the host board to a voltage between 3.15V and 3.6V.

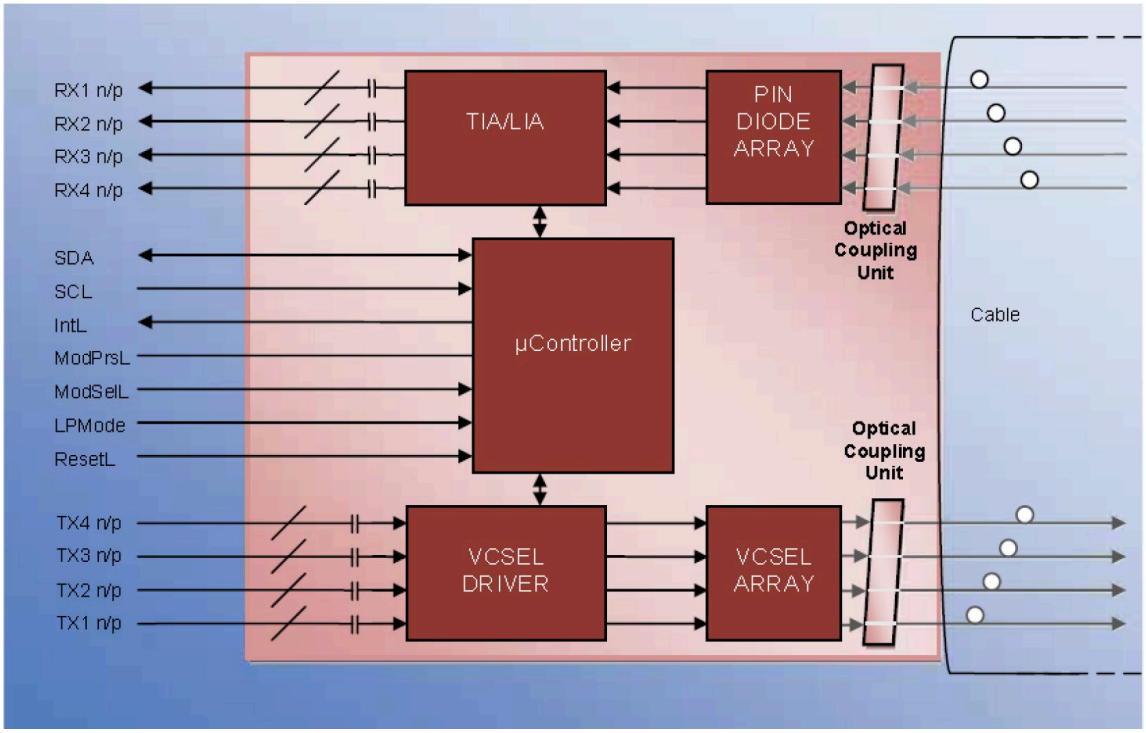
Electrical Pin-Out Details



Recommended Power Supply Filter



Block Diagram



Mechanical Specifications