OSFP-2X400G-LR4-P-AO

Juniper Networks® Compatible TAA 800GBase-2xLR4 PAM4 OSFP-IHS Transceiver (SMF, 1310nm, 10km, 2xLC, DOM, CMIS 5.0)

Features:

- Compliant with MSA: 2x400G-LR4-10 Optical Interface
- Compliant with OSFP MSA HW Rev 4.1
- Compliant with IEEE 802.3ck-2022: 2x400GAUI-4 C2M Electrical Interface
- CMIS 5.0 Compliant
- Class 1 Laser
- Type 2 Housing with Dual LC Connector
- Operating Temperature: 0 to 70 Celsius
- 2-Wire Serial Interface with Digital Diagnostic Monitoring
- RoHS Compliant and Lead-Free

Applications:

- 2x400GBase Ethernet

Product Description

This Juniper Networks® compatible OSFP-IHS Transceiver provides 800GBase-2xLR4 throughput up to 10km over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xLC connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

Rev. 100526

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Tstg	-40	85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (Non-Condensing)	RH	5	95	%
Data Input Voltage Differential	IVdip-VdinI		1	V
Control Input Voltage	Vi	-0.3	Vcc+0.5	V
Control Output Current	Io	-20	20	mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Instantaneous Peak Current at Hot Plug	Icc_IP			6800	mA
Sustained Peak Current at Hot Plug	Icc_SP			5661	mA
Maximum Power Dissipation	PDISS			17	W
Maximum Power Dissipation (Low-Power Mode)	P_{DLP}			2	W
Signaling Speed Per Lane	DRL		53.125		GBd
Control Input Voltage – High	V_{IH}	Vcc*0.7		Vcc+0.3	V
Control Input Voltage – Low	V_{IL}	-0.3		Vcc*0.3	V
2-Wire Serial Interface Clock Rate				400	kHz
Power Supply Noise (1kHz to 1MHz Pk-Pk)				66	mVp-p
Operating Distance		2		10000	m

Electrical Characteristics High-Speed Signal (Compliant with IEEE 802.3ck C2M)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter (Module Input, TP1)							
Differential Pk-Pk Input Voltage Tolerance (TP1a)			750			mV	
Pk-Pk AC Common-Mode Voltage Tolerance	**Low-Frequency (VCMLF)**				32	mV	
	Full-Band (VCMFB)				80		
Differential-Mode to Common-Mode Return Loss		RLcd	802.3ck 120G-2			dB	
Effective Return Loss		ERL	8.5			dB	
Differential Termination Mismatch					10	%	
Single-Ended Voltage Tolerance Range			-0.4		3.3	V	

DC Common-Mode Voltage Tolerance			-0.35		2.85	V	
Receiver (Module Output, TP4)							
Pk-Pk AC Common-Mode Voltage	**Low-Frequency (VCMLF)**				32	mV	
	Full-Band (VCMFB)				80		
Differential Pk-Pk Output Voltage	**Short-Mode**				600	mV	
	Long-Mode				845		
Eye Height		EH	15			mV	
Vertical Eye Closure		VEC			12	dB	
Common-Mode to Differential-Mode Return Loss		RLDc	802.3ck 120G-1			dB	
Effective Return Loss		ERL	8.5			dB	
Differential Termination Mismatch					10	%	
Transition Time			8.5			ps	
DC Common-Mode Voltage Tolerance			-0.35		2.85	V	

Electrical Characteristics Low-Speed Control and Sense Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Output SCL and SDA	V_{OL}	0		0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3		Vcc*0.3	V	
	V_{IH}	Vcc*0.7		Vcc+0.5	V	
InitMode, ResetL, and ModSelL	V_{IL}	-0.3		0.8	V	
	V_{IH}	2		Vcc+0.3	V	
IntL	V_{OL}	0		0.4	V	
	V_{OH}	Vcc-0.5		Vcc+0.3	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Wavelength L0, L4	λC0, λC4	1264.5	1271	1277.5	nm	
Wavelength L1, L5	λC1, λC5	1284.5	1291	1297.5	nm	
Wavelength L2, L6	λC2, λC6	1304.5	1311	1317.5	nm	
Wavelength L3, L7	λC3, λC7	1324.5	1331	1337.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOP_T			11.1	dBm	
Average Launch Power Per Lane	AOP_L	-2.7		5.1	dBm	1

Outer Optical Modulation Amplitude (OMAouter) Per Lane	**TDECQ<1.4dB**	TOMA	-0.3		4.4	dBm	
	1.4dB≤TDECQ≤3.4dB		-1.1+TDECQ				
Difference in Launch Power Between Any Two Lanes (OMAouter)		AOPd			4	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane		TDECQ			3.9	dB	
Transmitter Eye Closure for PAM4 (TECQ) Per Lane		TECQ			3.9	dB	
| TDECQ – TECQ |					2.5	dB	
Transmitter Overshoot/Undershoot					25	%	
Transmitter Power Excursion					5.2	dBm	
Average Launch Power of Off Transmitter Per Lane		Toff			-16	dBm	
Extinction Ratio		ER	3.5			dB	
Transmitter Transition Time (Maximum)		Tr			17	ps	
$RIN_{15.6}$OMA (Maximum)		RIN			-136	dB/Hz	
Optical Return Loss Tolerance		ORL			15.6	dB	
Transmitter Reflectance		T_R			-26	dB	2
Receiver							
Wavelength L0, L4		λC0, λC4	1264.5	1271	1277.5	nm	
Wavelength L1, L5		λC1, λC5	1284.5	1291	1297.5	nm	
Wavelength L2, L6		λC2, λC6	1304.5	1311	1317.5	nm	
Wavelength L3, L7		λC3, λC7	1324.5	1331	1337.5	nm	
Damage Threshold Per Lane		AOP_D	6.1			dBm	
Average Receive Power Per Lane		AOP_R	-9		5.1	dBm	
Receive Power (OMAouter) Per Lane		OMA_R			4.4	dBm	
Difference in Receive Power Between Any Two Lanes (OMAouter) Maximum		AOP_g			4.3	dB	
Receiver Reflectance		RR			-26	dB	
Receiver Sensitivity (OMAouter) Per Lane	**TECQ<1.4dB**	SOMA			-6.8	dBm	
	1.4dB≤TECQ≤3.4dB				-8.2+TECQ		
Stressed Receiver Sensitivity (OMAouter) Per Lane		SRS			-4.3	dBm	3
Conditions of Stressed Receiver Sensitivity Test							
Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test				3.9		dB	
OMAouter of Each Aggressor Lane				1.4		dBm	

Notes:

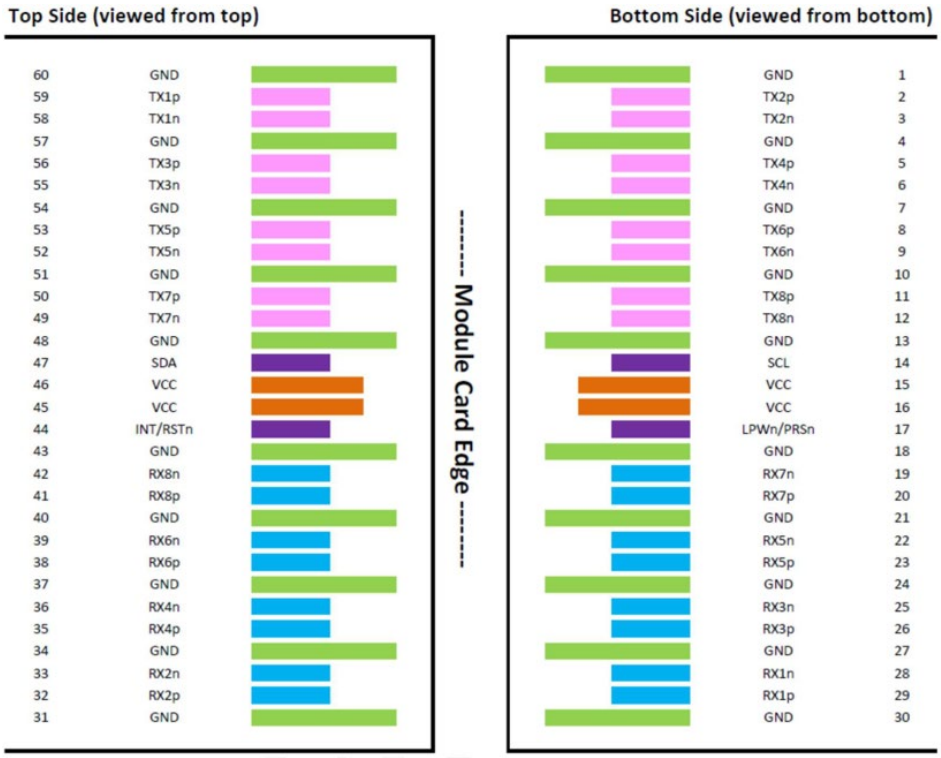
1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Measured with conformance test signal at TP3 for the BER=2.4×10^{-4}.

Pin Descriptions

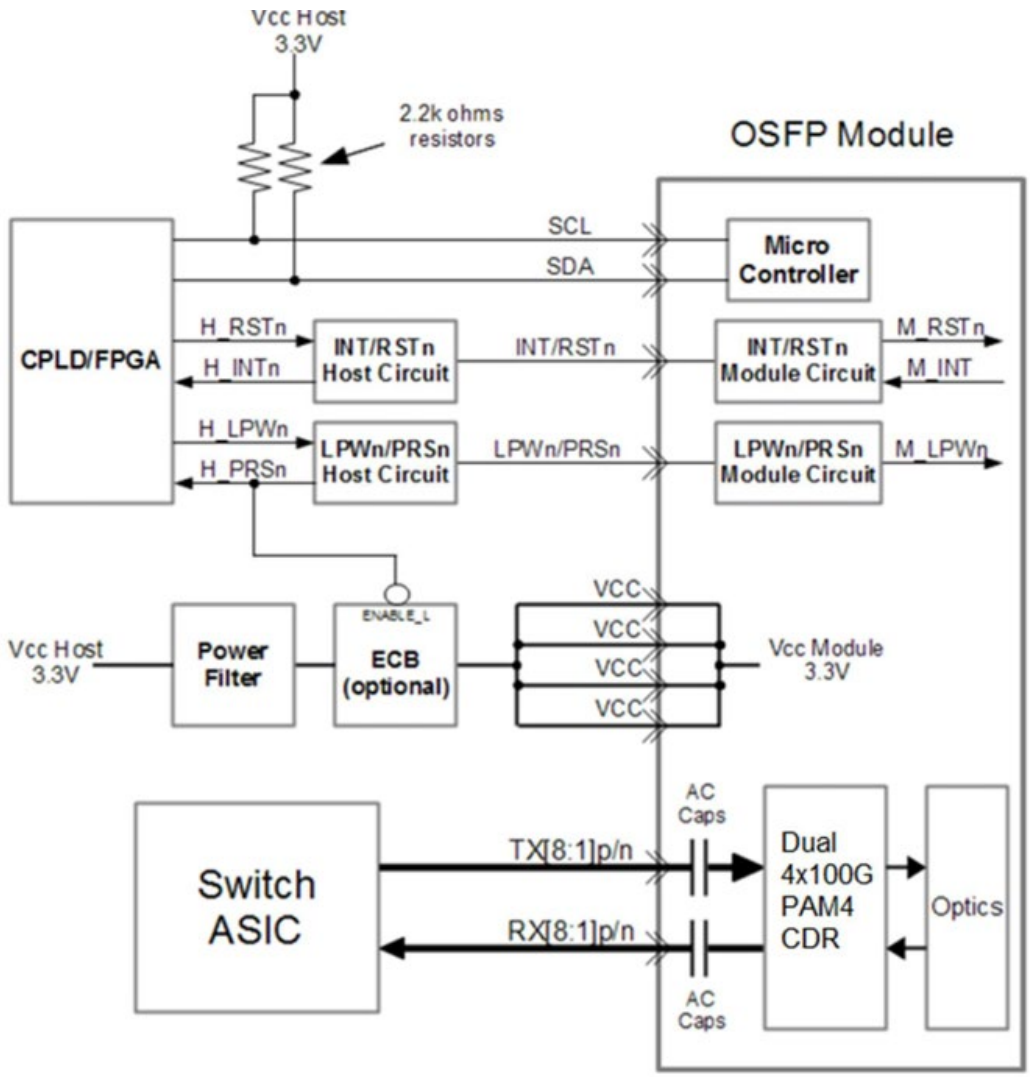
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	
2	CML-I	Tx2p	Transmitter Data Non-Inverted.	
3	CML-I	Tx2n	Transmitter Data Inverted.	
4		GND	Module Ground.	
5	CML-I	Tx4p	Transmitter Data Non-Inverted.	
6	CML-I	Tx4n	Transmitter Data Inverted.	
7		GND	Module Ground.	
8	CML-I	Tx6p	Transmitter Data Non-Inverted.	
9	CML-I	Tx6n	Transmitter Data Inverted.	
10		GND	Module Ground.	
11	CML-I	Tx8p	Transmitter Data Non-Inverted.	
12	CML-I	Tx8n	Transmitter Data Inverted.	
13		GND	Module Ground.	
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	
15		Vcc	+3.3V Power.	
16		Vcc	+3.3V Power.	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	
18		GND	Module Ground.	
19	CML-O	Rx7n	Receiver Data Inverted.	
20	CML-O	Rx7p	Receiver Data Non-Inverted.	
21		GND	Module Ground.	
22	CML-O	Rx5n	Receiver Data Inverted.	
23	CML-O	Rx5p	Receiver Data Non-Inverted.	
24		GND	Module Ground.	
25	CML-O	Rx3n	Receiver Data Inverted.	
26	CML-O	Rx3p	Receiver Data Non-Inverted.	
27		GND	Module Ground.	
28	CML-O	Rx1n	Receiver Data Inverted.	
29	CML-O	Rx1p	Receiver Data Non-Inverted.	
30		GND	Module Ground.	
31		GND	Module Ground.	
32	CML-O	Rx2p	Receiver Data Non-Inverted.	
33	CML-O	Rx2n	Receiver Data Inverted.	
34		GND	Module Ground.	
35	CML-O	Rx4p	Receiver Data Non-Inverted.	
36	CML-O	Rx4n	Receiver Data Inverted.	
37		GND	Module Ground.	
38	CML-O	Rx6p	Receiver Data Non-Inverted.	
39	CML-O	Rx6n	Receiver Data Inverted.	

40		GND	Module Ground.	
41	CML-O	Rx8p	Receiver Data Non-Inverted.	
42	CML-O	Rx8n	Receiver Data Inverted.	
43		GND	Module Ground.	
44	Multi-Level	INT/RSTn	Module Interrupt/Module Reset.	
45		Vcc	+3.3V Power.	
46		Vcc	+3.3V Power.	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	
48		GND	Module Ground.	
49	CML-I	Tx7n	Transmitter Data Inverted.	
50	CML-I	Tx7p	Transmitter Data Non-Inverted.	
51		GND	Module Ground.	
52	CML-I	Tx5n	Transmitter Data Inverted.	
53	CML-I	Tx5p	Transmitter Data Non-Inverted.	
54		GND	Module Ground.	
55	CML-I	Tx3n	Transmitter Data Inverted.	
56	CML-I	Tx3p	Transmitter Data Non-Inverted.	
57		GND	Module Ground.	
58	CML-I	Tx1n	Transmitter Data Inverted.	
59	CML-I	Tx1p	Transmitter Data Non-Inverted.	
60		GND	Module Ground.	

Electrical Pad Layout



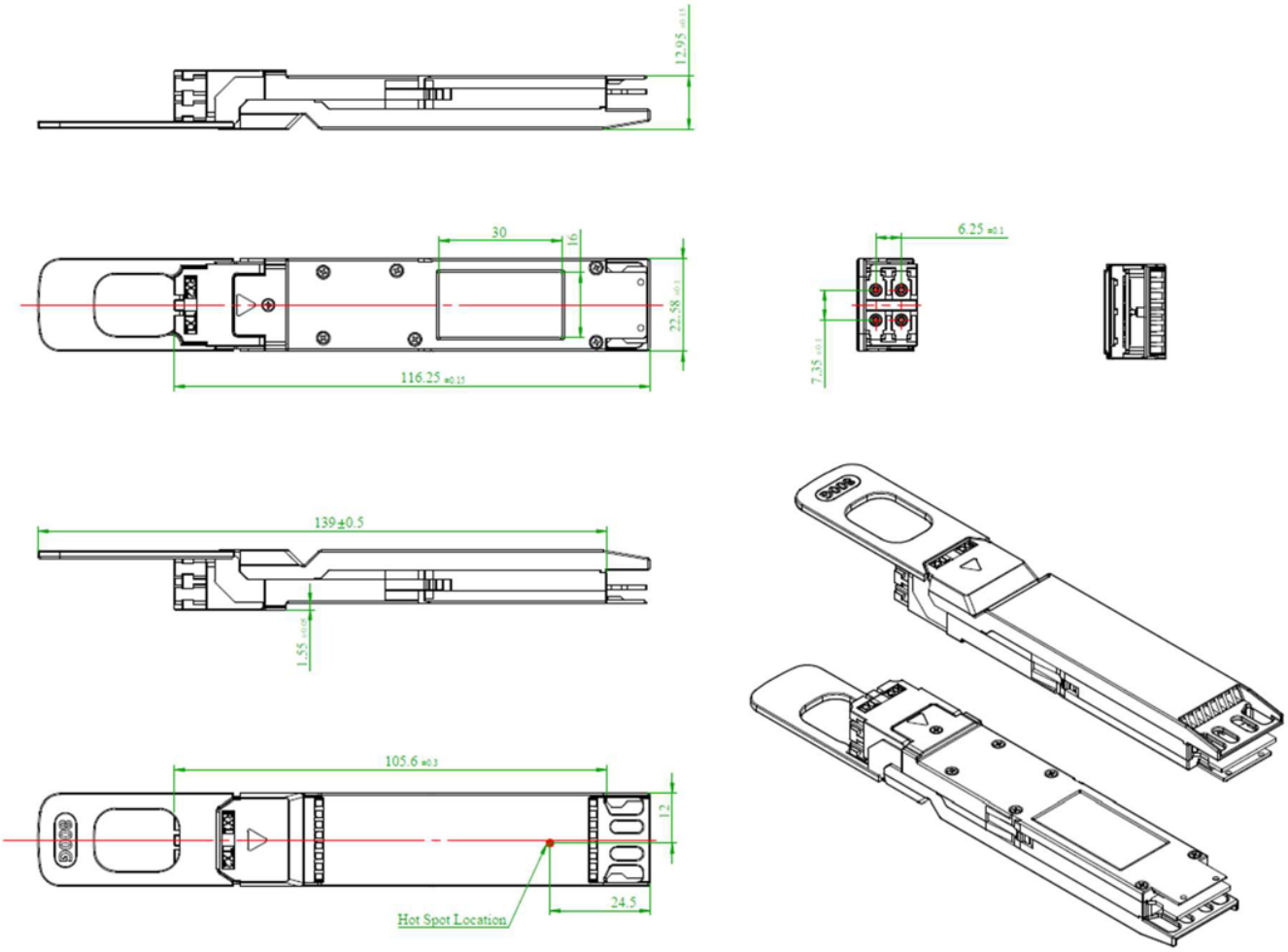
Recommended Host Board Schematic



Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 10	±3	°C	Internal
Voltage	0 to Vcc	0.1	V	Internal
Tx Bias Current Per Lane	0 to 100	10%	mA	Internal
Tx Output Power Per Lane	-2.7 to +5.1	±3	dB	Internal
Rx Receive Power Per Lane	-9 to +5.1	±3	dB	Internal

Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.

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