QDD-400G-PLR4-AO

Juniper Networks® Compatible TAA 400GBase-PLR4 QSFP-DD Transceiver (SMF, 1310nm, 10km, MPO, DOM, CMIS 4.0)

Features

- INF-8628 Compliance
- MPO Connector
- Commercial Temperature 0 to 70 Celsius
- Single-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free

Applications

- 400GBase Ethernet

Product Description

This Juniper Networks® QSFP-DD transceiver provides 400GBase-PLR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is guaranteed to be 100% compatible with the equivalent Juniper Networks® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

TAA COMPLIANT

Rev. 051123

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Power Supply Voltage	VCC	0		3.6	V	3.3V
Storage Temperature	Ts	-40		85	°C	
Case Operating Temperature	TC	0	25	70	°C	
Optical Receiver Input				5.8	dBm	Average

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Module Power Supply Noise Tolerance	$PSNR_{mod}$			66	mV	10 Hz – 10 MHz
Power Consumption				12	W	
Instantaneous peal current	Icc_ip_6			4800	mA	
Sustained peak current	Icc_sp_6			3960	mA	
Supply Current	Icc_6			3827.8	mA	Steady state
Transmitter Output (Each Lane, at TP4) Note 1						
Signaling rate per lane (range)		-100ppm	26.5625	+100ppn	GBd	
AC Common-mode output voltage	RMS			17.5	mV	
Differential peak-to-peak output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Near-end Eye height, differential		70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		Equation (83E-2)			dB	2
Common to differential mode conversion return loss		Equation (83E-3)			dB	2
Differential termination mismatch				10	%	
Transition time (20% to 80%)		9.5			ps	
DC common mode voltage		-350		2850	mV	
Receiver Input (Each Lane)						
Signaling rate per lane (range)		-100ppm	26.5625	+100ppm	GBd	
Differential pk-pk input voltage tolerance		900			mV	at TP1a
Differential Input Return Loss		Equation (83E-5)			dB	at TP1, Note 2
Differential to common mode input return loss		Equation (83E-6)			dB	at TP1,Note 2
Differential termination mismatch				10	%	at TP1

ESMW (Eye symmetry mask width)		0.22			UI	at TP1a
Eye width		0.22			UI	at TP1a
Applied pk-pk sinusoidal jitter		Table 120E–6			MHz, UI	at TP1a
Eye height		32			mV	at TP1a
Single-ended input voltage tolerance range		-0.4		3.3	V	at TP1a
DC common mode voltage		-350		2850	mV	at TP1

Notes:

1. Electrical module output is squelched for loss of optical input signal.
2. IEEE 802.3-2018 Section 6

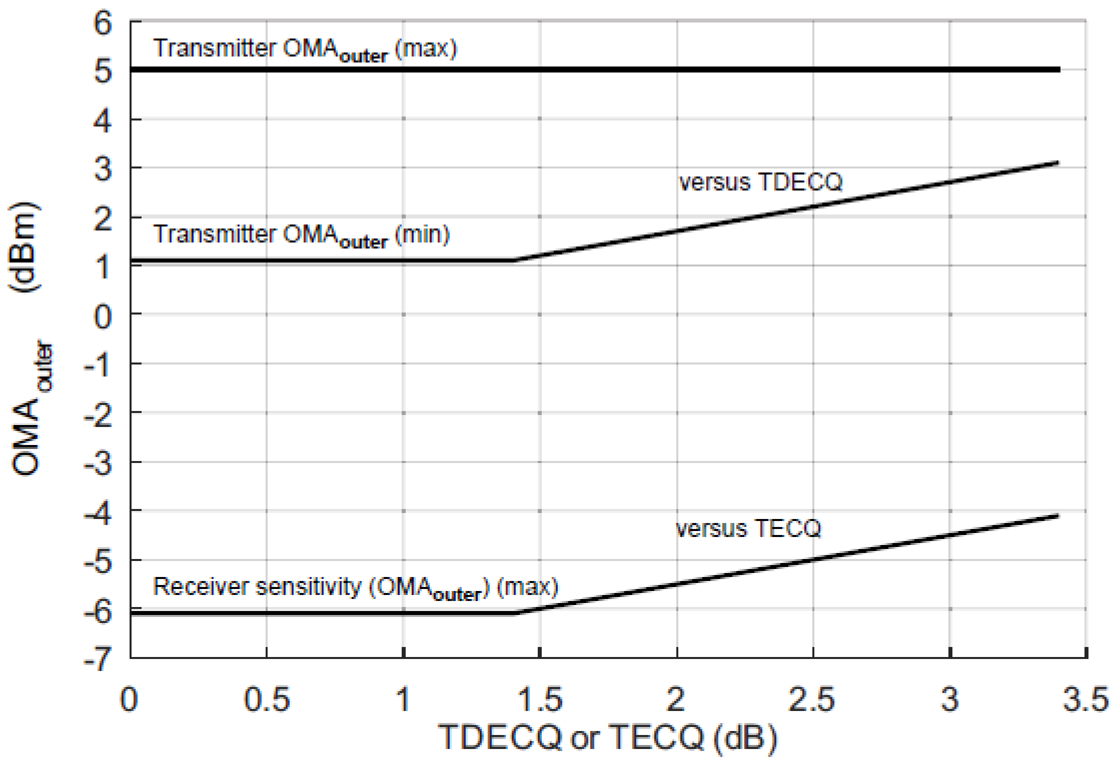
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Channel data rate	fDC	106.25			Gbit/s	
Signaling rate	fSG	53.125			GBd	
Signal speed variation from nominal	Δf_{SG}	-100		+100	ppm	
Lane wavelength (range)	λ_C	1304.5		1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power		-1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMAouter) [Figure below]		1.1		5.0	dBm	for TDECQ <1.4 dB
		-0.3 + TDECQ				for 1.4 dB ≤ TDECQ ≤ 3.4 dB
Transmitter and dispersion eye closure for PAM4	TDECQ			3.4	dB	
Transmitter eye closure for PAM4	TECQ			3.4	dB	
TDECQ - TECQ				2.5	dB	
Average Optical Output Power of Off Transmitter	Poff			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter transition time				17	ps	
Transmitter over/under-shoot				22	%	
Transmitter peak-to-peak power				5.5	dBm	
$RIN_{15.6}OMA$				-136	dB/Hz	
Optical return loss tolerance				15.6	dB	
Transmitter reflectance				-26	dB	2
Receiver						
Average receive power		–8.2		4.8	dBm	3
Receive power (OMAouter)				5.0	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter) [Figure below]		Max -6.1				for TECQ <1.4 dB, Note 4
		Max (-7.5 + TECQ)				for 1.4 dB ≤ TECQ ≤ 3.4 dB, Note 4
Stressed receiver sensitivity (OMAouter)				-4.1	dBm	4, 5
Conditions of stressed receiver sensitivity test [Note 6]						
Stressed eye closure for PAM4	SECQ	3.4			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.

3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. For when Pre-FEC BER is 2.4×10^{-4}.
5. Measured with conformance test signal at TP3 (see 140.7.10) for the BER specified in 140.1.1.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



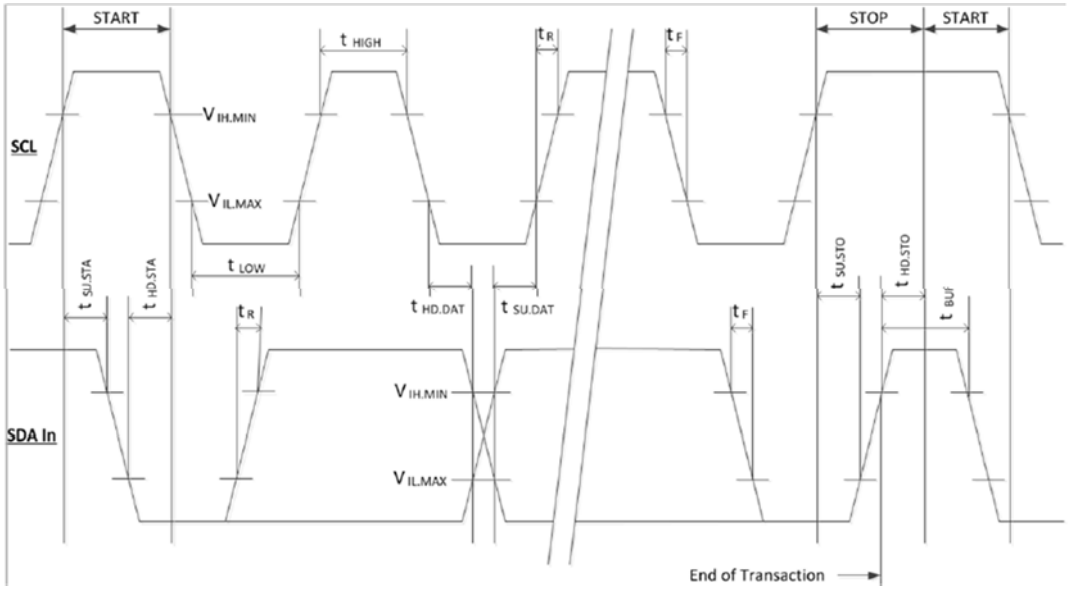
Transmitter OMAouter versus TDECQ and Receiver sensitivity (OMAouter) versus TECQ for 100GBASE-LR1

Management Interface Timing Parameters

Parameter	Symbol	Fast Mode Plus (1 MHz)		Unit	Conditions
		Min	Max		
Clock Frequency	fSCL	0	1000	kHz	
Clock Pulse Width Low	tLOW	0.50		µs	
Clock Pulse Width High	tHIGH	0.26		µs	
Time bus free before new transmission can start	tBUF	1		µs	Between STOP and START andbetween ACK and ReStart
START Hold Time	tHD.STA	0.26		µs	The delay required between SDA becoming low and SCL starting to golow in a START
START Setup Time	tSU.STA	0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		µs	
Data In Setup Time	tSU.DAT	0.1		µs	
Input Rise Time	tR		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.26		µs	
STOP Hold Time	tHD.STO	0.26		us	
Aborted sequence. bus release	Deselect _Abort		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCLand SDA
ModSelL Setup Time[1]	tSU.ModSelL	2		ms	ModSelL Setup Time is the setup timeon the select lines before the start of a host initiated serial bus sequence.
ModSelL Hold Time[1]	tHD.ModSelL	2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status.
Serial Interface ClockHoldoff "Clock Stretching"	T_clock_hold		500	us	Maximum time the QSFP-DD modulemay hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write to non-volatile registers	tWR		80	ms	Complete Write of up to 8 Bytes
Accept a single or sequential write tovolatile memory.	tNACK		80	ms	Time required for the module to accept a single or sequential write to volatile memory.
Endurance (Write Cycles)		50k		cycles	Module Case Temperature= 70°C

Notes:

1. When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.



2-Wire Interface Timing Diagram

Pin Descriptions

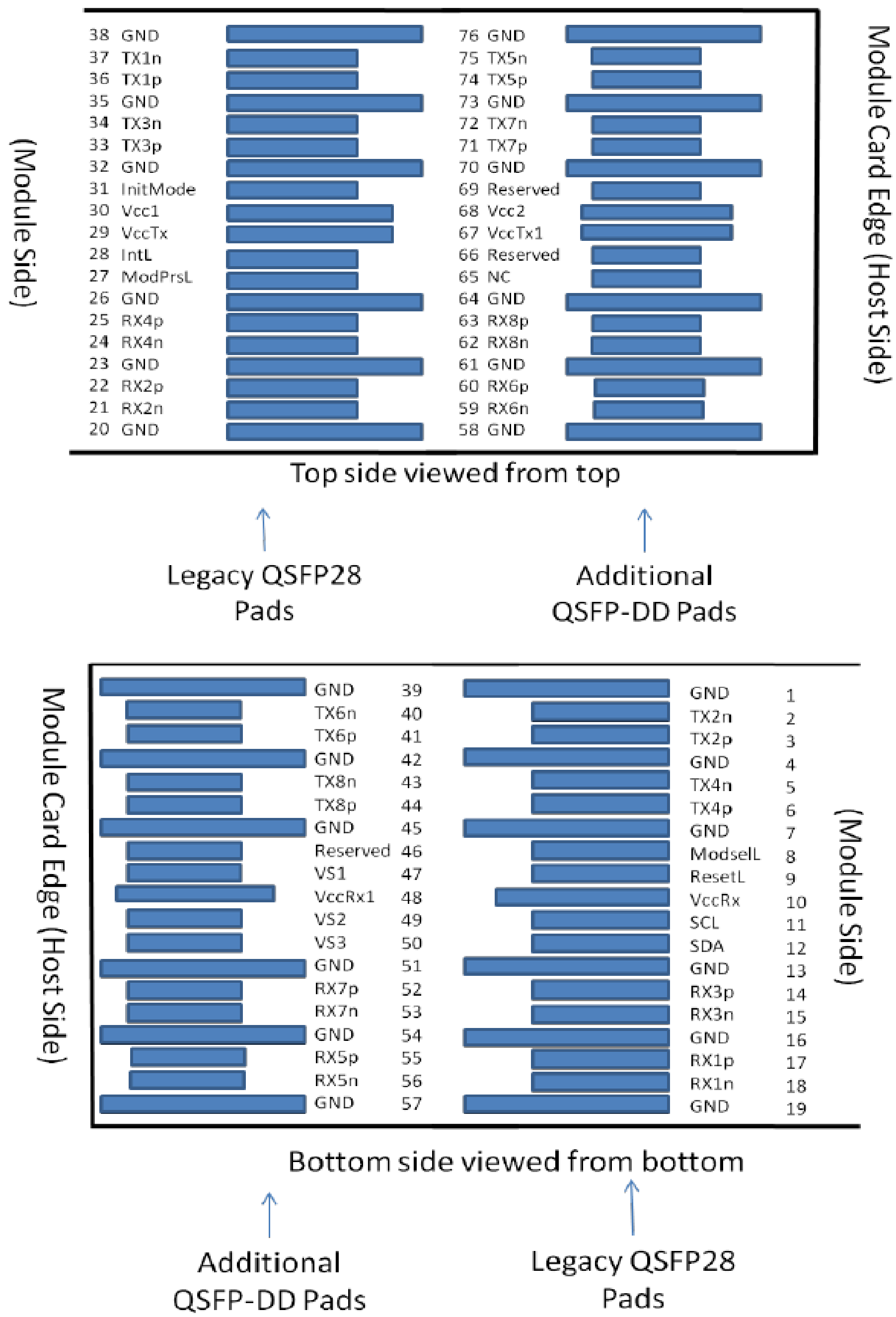
Pin	Logic	Symbol	Name/Descriptions	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16	GND	Ground	1B		1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	Reserved	~~Precision Time Protocol (PTP) reference clock input~~	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

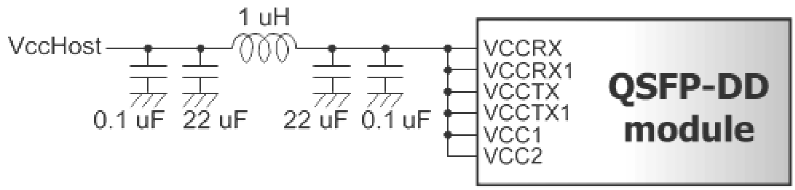
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are refenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1

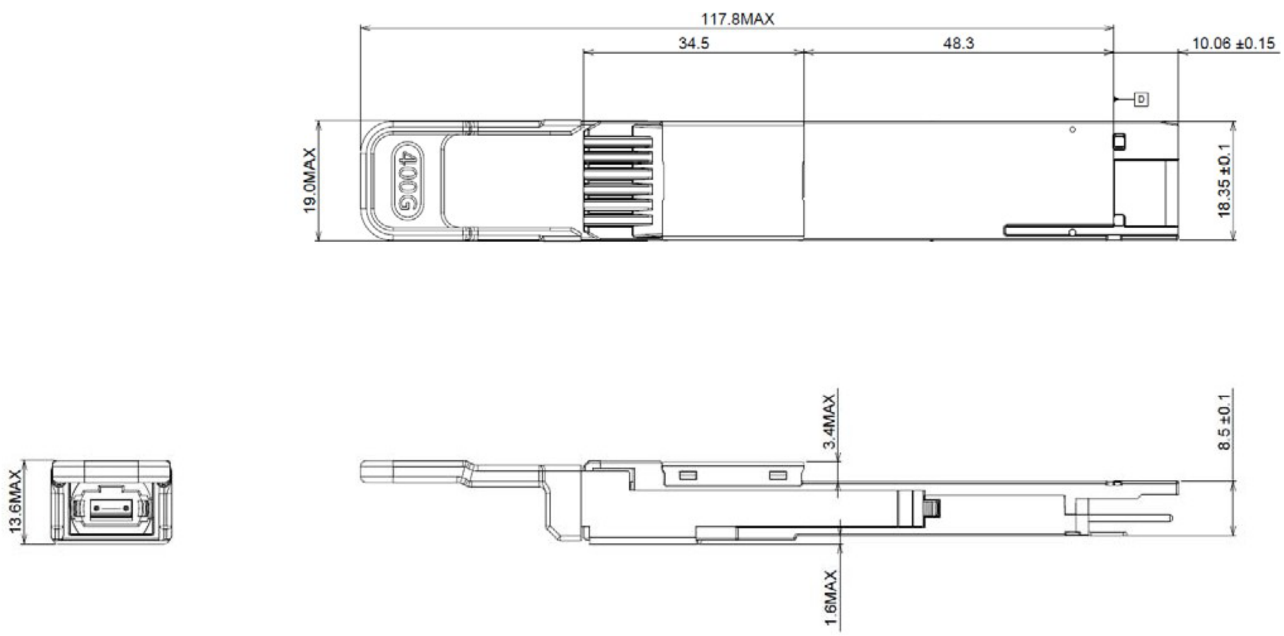
QSFPDD Connector Pin Definition



Recommended Power Supply Filter



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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