SFP-10GBASE-LR-20-I-AT-OPC

ADTRAN® 1700486F1 Compatible TAA 10GBase-LR SFP+ Transceiver (SMF, 1310nm, 20km, LC, DOM, -40 to 85C)

Features

- Compliant with IEEE802.3ae 10GBASE-LR/LW
- Compliant with MSA SFP+ Specification SFF-8431
- 1310nm DFB-LD Transmitter
- Distance up to 20km
- Single 3.3V Power Supply and TTL Logic Interface
- Duplex LC Connector
- Industrial Temperature -40 to 85 Celsius
- Hot-Pluggable
- Metal with Lower EMI
- Excellent ESD Protection
- RoHS compliant and Lead Free

Applications:

- 10GBase-LR Ethernet
- 8x/10x Fibre Channel
- Access, Datacenter and Enterprise
- Mobile Fronthaul CPRI/OBSAI

Product Description

This ADTRAN® 1700486F1 compatible SFP+ transceiver provides 10GBase-LR throughput up to 20km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It is capable of withstanding rugged environments and can operate at temperatures between -40 and 85C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with ADTRAN®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	Vcc	-0.5		4	V	1
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	-40		85	°C	
Relative Humidity	RH	0		85	%	
Data Rate	DR	9.83	10.3125	11.3	Gb/s	2
Bit Error Rate	BER			10^{-12}		

Notes:

1. For electrical interface
2. IEEE 802.3ae

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Supply Voltage	Vcc	3.14	3.3	3.46	V	
Module Supply Current	Icc		200	350	mA	
Power Dissipation	PD		0.65	1.2	W	
Transmitter						
Input Differential Impedance	R_{IN}		100		Ω	
Differential Data Input Swing	$V_{IN\ PP}$	180		700	mV	
Transmit Disable Voltage	V_D	2		V_{CC}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	
Receiver						
Differential Data Output Swing	$V_{OUT\ PP}$	300		850	mV	
Data Output Rise/Fall Time (20%-80%)	t_r/t_f	28			ps	
LOS Assert	$V_{LOS\ A}$	2		$V_{CC\ HOST}$	V	
LOS De-Assert	$V_{LOS\ D}$	V_{EE}		V_{EE}+0.5	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Output Optical Power	P_{TX}	-8.2		0.5	dBm	1
Optical Center Wavelength	λ_C	1260		1355	nm	
Optical Modulation Amplitude	OMA	-5.2			dBm	2
Extinction Ratio	ER	3.5	5.5		dB	
Spectral Width(-20dB)	$\Delta\lambda$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Transmitter Dispersion Penalty	TDP			3.2	dB	
Launch Power of OFF Transmitter	P_{OUT_OFF}			-30	dBm	1
Transmitter Jitter						2
Receiver						
Optical Center Wavelength	λ_C	1260		1600	nm	
Average Receive Power	P_{RX}	-14.4		0.5	dBm	
Receiver Sensitivity @10.3Gb/s	R_{X_SEN}			-14.4	dBm	3
Receiver Reflectance	TR_{RX}			-12	dB	
LOS Assert	LOS_A	-30			dBm	
LOS De-Assert	LOS_D			-17	dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Notes:

1. Average
2. According to IEEE 802.3ae requirement.
3. Test the resulting value using the minimum ER value within the defined range; BER<10^{-12}; 2^{31}-1 PRBS.

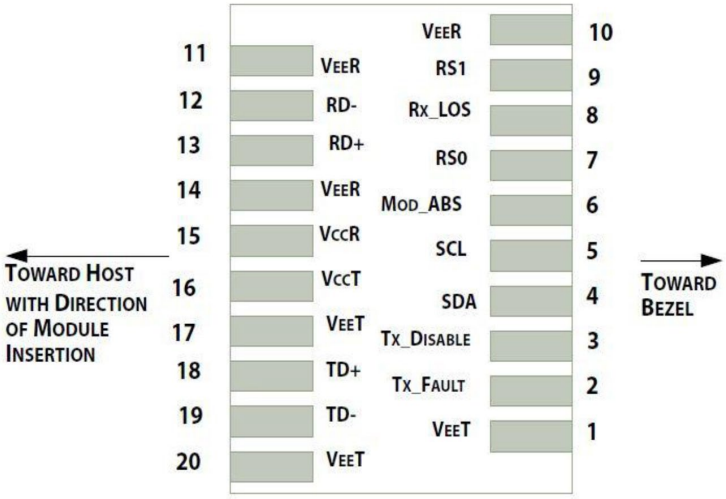
Pin Descriptions

Pin	Symbol	Name/Descriptions	Ref.
1	VeeT	Transmitter Ground.	1
2	Tx_Fault	Transmitter Fault. LVTTL-O. “High” indicates a fault condition.	2
3	Tx_Disable	Transmitter Disable. LVTTL-I. “High” or “open” disables the transmitter.	3
4	SDA	2-Wire Serial Interface Data. LVCMOS-I/O. MOD-DEF2.	4
5	SCL	2-Wire Serial Interface Clock. LVCMOS-I/O. MOD-DEF1.	4
6	MOD_ABS	Module Absent (Output). Connected to VeeT or VeeR in the module.	5
7	RS0	N/A.	6
8	Rx_LOS	Receiver Loss of Signal. LVTTL-O.	2
9	RS1	N/A.	6
10	VeeR	Receiver Ground.	1
11	VeeR	Receiver Ground.	1
12	RD-	Inverse Received Data Out. CML-O.	
13	RD+	Received Data Out. CML-O.	
14	VeeR	Receiver Ground.	
15	VccR	+3.3V Receiver Power.	
16	VccT	+3.3V Transmitter Power.	
17	VeeT	Transmitter Ground.	1
18	TD+	Transmitter Data In. CML-I.	
19	TD-	Inverse Transmitter Data In. CML-I.	
20	VeeT	Transmitter Ground.	1

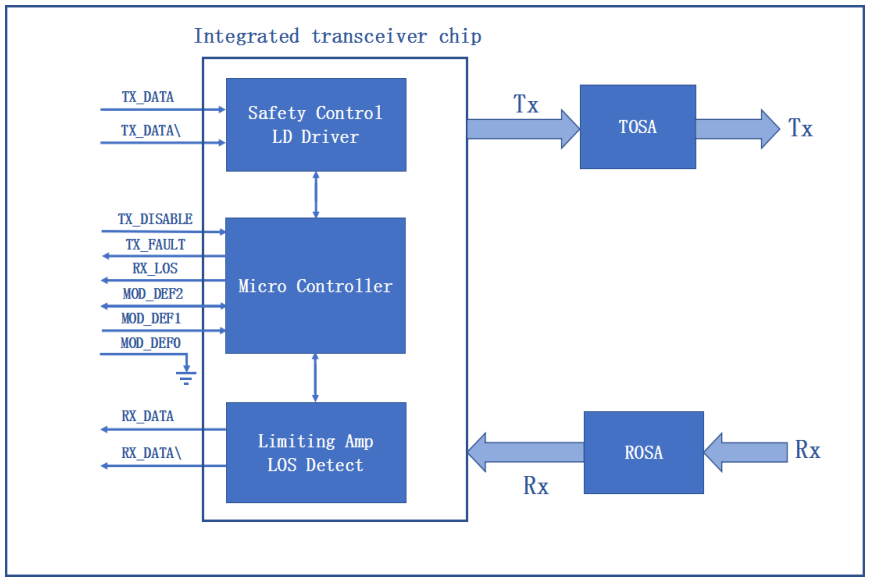
Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to Host_Vcc.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. 2-Wire Serial Interface Clock and Data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that, on the host board, requires a 4.7KΩ to 10KΩ pull-up resistor to the Host_Vcc.
6. Rate select can also be set through the 2-wire bus in accordance with SFF-8472 v. 12.1. Rx Rate Select is set at Bit 3, Byte 110, and Address A2h, and Tx Rate Select is set at Bit 3, Byte 118, and Address A2h. **Note:** Writing a “1” selects maximum bandwidth operation. Rate select is the logic OR of the input state of Rate Select Pin and 2-wire bus.

Electrical Pin-out Details



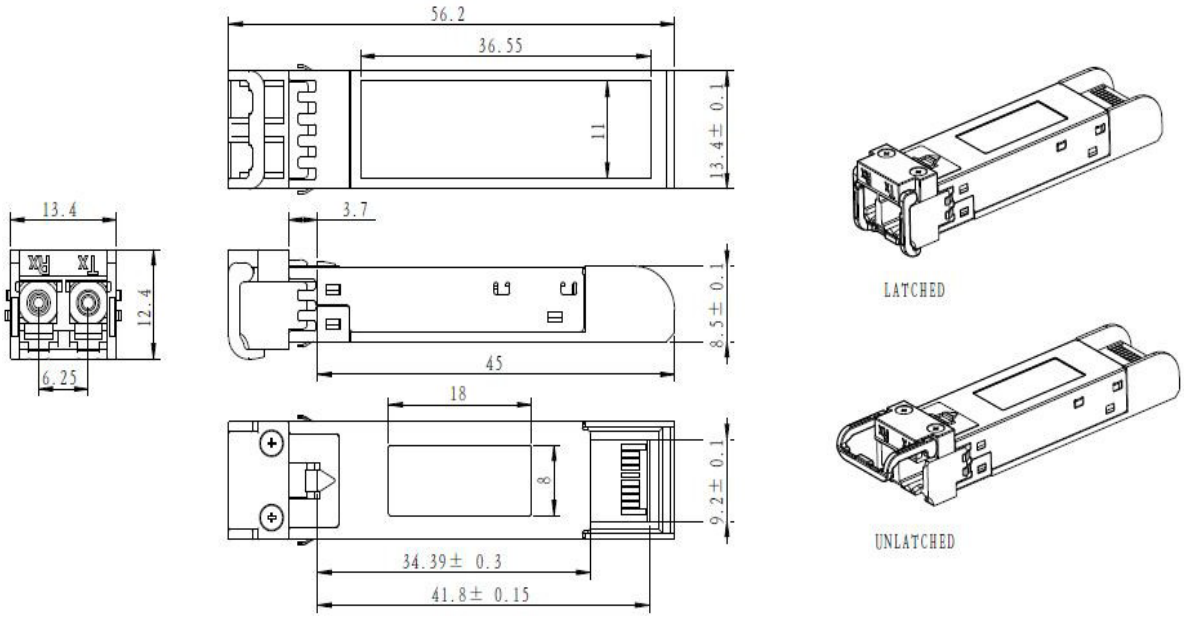
Block Diagram



Mechanical Specifications

ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED

UNIT: mm



EEPROM Information

EEPROM memory map-specific data field description is as below: