MMA1U00-WS-AO

NVIDIA® MMA1U00-WS Compatible TAA 400GBase-SR8 QSFP-DD Transceiver (MMF, 850nm, MPO-16, 100m)

Features:

- Hot-Pluggable QSFP-DD Form Factor
- 8x50G PAM4 Retimed 400GUAI-8 Electrical Interface Aligned with IEEE 802.3bs
- 8x50G PAM4 VCSEL Transmitter
- Power Dissipation: 9W
- Maximum Link Length of 100M on OM4 Fiber with KP4 FEC
- I2C Management Interface
- Single 3.3V Power Supply
- MPO-16 APC Connector
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius



Applications:

- 400GBase Ethernet

Product Description

This NVIDIA® MMA1U00-WS compatible QSFP-DD transceiver provides 400GBase-SR8 throughput up to 100m over multi-mode fiber (MMF) using a wavelength of 850nm via an MPO-16 connector. It is guaranteed to be 100% compatible with the equivalent NVIDIA® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.5	4.0	V	
Storage Temperature	Tstg	-40	85	°C	
Operating Temperature	Tc	0	70	°C	
Relative Humidity	RH	15	85	%	1
Receiver Damage Threshold Per Lane	THd	5		dBm	
Bit Error Ratio	BER		$2.4E^{-4}$		2
Bit Rate (All Wavelengths Combined)	BR		425	Gbps	3

Notes:

1. Non-condensing.
2. As defined by IEEE P802.3cm.
3. Supports 400GBase-SR8 per IEEE P802.3cm.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2.87	A	
Module Total Power	P			9	W	1
Transmitter (Per Lane)						
Signaling Rate Per Lane	TP1	26.5625 ± 100ppm			GBd	
Differential Data Input Voltage Per Lane	VIN,pp	900			mV	2
Differential Input Return Loss		Per Equation (83E-5) IEEE802.3bm				
Differential- to Common-Mode Input Return Loss		Per Equation (83E-6) IEEE802.3bm				
Differential Termination Mismatch				10		
Module Stressed Input Test		Per 120E.3.4.1 IEEE802.3bs				3
Single-Ended Voltage Tolerance Range		-0.4		3.3		
DC Common-Mode Voltage		-350		2850	mV	4
Receiver (Per Lane)						
Signaling Rate Per Lane		26.5625 ± 100ppm			Gbd	
AC Common-Mode Output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-End ESMW (Eye Symmetry Mask Width)		0.265			UI	
Differential Near-End Eye Height (Minimum)		30			mV	
Far-End Pre-Cursor ISI Ratio		-4.5		2.5	%	
Differential Output Return Loss		Per Equation (83E-2) IEEE802.3bm				

Common- to Differential-Mode Conversion Return Loss		Per Equation (83E-3) IEEE802.3bm				
Differential Termination Mismatch				10	%	
Transition Time (20-80%)		9.5			ps	
DC Common-Mode Voltage Minimum		-350		2850	mV	

Notes:

1. The maximum total power value is specified across the full temperature and voltage range.
2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets specified BER.
4. DC common-mode voltage is generated by the host. Specification includes the effects of ground offset voltage.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λC	840	850	860	nm	
Data Rate Per Lane		26.5625 ± 100ppm			GBd	
Modulation Format		PAM4				
RMS Spectral Width				0.6	nm	1
Average Launch Power Per Lane		-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMAouter) Per Lane		-4.5			dBm	2
Launch Power in OMAouter Minus TDECQ Per Lane		-5.9			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane				4.5	dB	
TDECQ -10Log$_{10}$(Ceq) Per Lane				4.5	dB	3
Average Launch Power of Off Transmitter Per Lane				-30	dBm	
Extinction Ratio		3			dB	
Transmitter Transition Time Per Lane				34	ps	
RIN$_{12}$OMA				-128	dB/Hz	
Optical Return Loss Tolerance				12	dB	
Encircle Flux		≥86% at 19µm ≤30% at 4.5µm				4
Receiver						
Center Wavelength	λC	840	850	860	nm	
Data Rate Per Lane		26.5625 ± 100ppm			GBd	
Modulation Format		PAM4				
Damage Threshold Per Lane		5			dBm	1
Average Receive Power Per Lane		-8.4		4	dBm	2
Receive Power (OMA$_{outer}$) Per Lane				3	dBm	

Receiver Reflectance				-12	dBm	
Receiver Sensitivity (OMA_{outer}) Per Lane				-3	dBm	3
Stressed Receiver Sensitivity (OMAouter) Per Lane				-12	dB	4
Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test			4.5			5
SECQ-$10Log_{10}$(Ceq)f Per Lane (Maximum)			4.5			5
OMAouter of Each Aggressor Lane			3			
LOS De-Assert				-9	dBm	
LOS Assert		-30		-10	dBm	
LOS Hysteresis		0.5			dB	
Conditions of Stressed Receiver Sensitivity Test						6

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
2. Average receive power, each lane (minimum), is informative and not the principal indicator of signal strength.
3. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5dB.
4. Measured with conformance test signal at TP3 (see 138.8.10) for the BER specified in 138.1.1.
5. Ceq is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1B	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3B	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3B	
4		GND	Module Ground.	1B	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3B	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3B	
7		GND	Module Ground.	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Receiver Power Supply.	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3B	
13		GND	Module Ground.	1B	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3B	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3B	
16		GND	Module Ground.	1B	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3B	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3B	
19		GND	Module Ground.	1B	1
20		GND	Module Ground.	1B	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3B	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3B	
23		GND	Module Ground.	1B	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3B	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3B	
26		GND	Module Ground.	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Transmitter Power Supply.	2B	2
30		Vcc1	+3.3V Power Supply.	2B	2
31	LVTTL-I	InitMode	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMode.	3B	
32		GND	Module Ground.	1B	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3B	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3B	
35		GND	Module Ground.	1B	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3B	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3B	
38		GND	Module Ground.	1B	1
39		GND	Module Ground.	1A	1

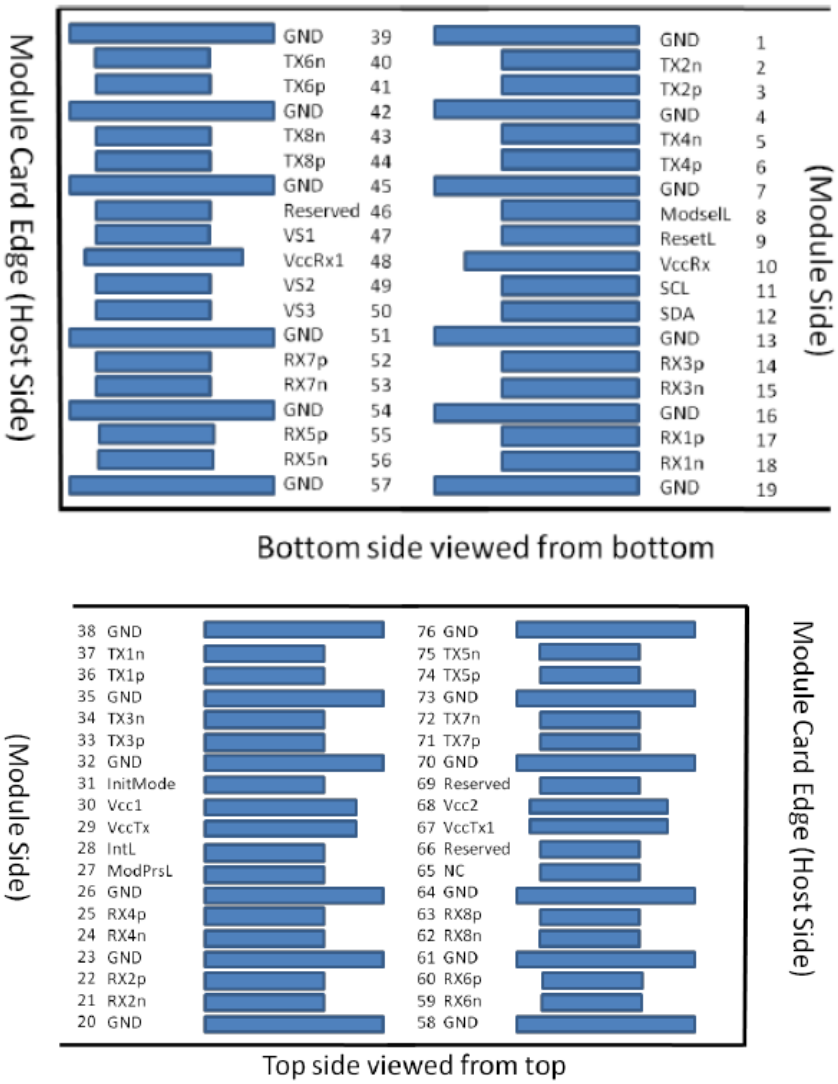
40	CML-I	Tx6-	Transmitter Inverted Data Input.	3A	
41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	3A	
42		GND	Module Ground.	1A	1
43	CML-I	Tx8-	Transmitter Inverted Data Input.	3A	
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	3A	
45		GND	Module Ground.	1A	1
46		Reserved	For Future Use.	3A	3
47		VS1	Module Vendor-Specific 1.	3A	3
48		VccRx1	+3.3V Receiver Power Supply.	2A	2
49		VS2	Module Vendor-Specific 2.	3A	3
50		VS3	Module Vendor-Specific 3.	3A	3
51		GND	Module Ground.	1A	1
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	3A	
53	CML-O	Rx7-	Receiver Inverted Data Output.	3A	
54		GND	Module Ground.	1A	1
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	3A	
56	CML-O	Rx5-	Receiver Inverted Data Output.	3A	
57		GND	Module Ground.	1A	1
58		GND	Module Ground.	1A	1
59	CML-O	Rx6-	Receiver Inverted Data Output.	3A	
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	3A	
61		GND	Module Ground.	1A	1
62	CML-O	Rx8-	Receiver Inverted Data Output.	3A	
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	3A	
64		GND	Module Ground.	1A	1
65		NC	Not Connected.	3A	3
66		Reserved	For Future Use.	3A	3
67		VccTx1	+3.3V Transmitter Power Supply.	2A	2
68		Vcc2	+3.3V Power Supply.	2A	2
69		Reserved	For Future Use.	3A	3
70		GND	Module Ground.	1A	1
71	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	3A	
72	CML-I	Tx7-	Transmitter Inverted Data Input.	3A	
73		GND	Module Ground.	1A	1
74	CML-I	Tx5+	Transmitter Non-Inverted Data Input.	3A	
75	CML-I	Tx5-	Transmitter Inverted Data Input.	3A	
76		GND	Module Ground.	1A	1

Notes:

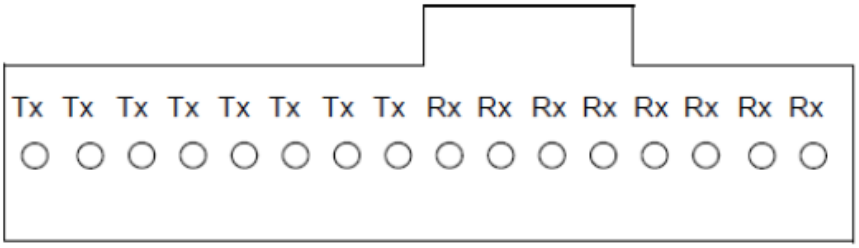
1. QSFP-DD uses common ground (GND) for all signals and supply power. All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in the Optical Characteristics. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor-Specific, Reserved, and Not Connected pins may be terminated with 50Ω to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

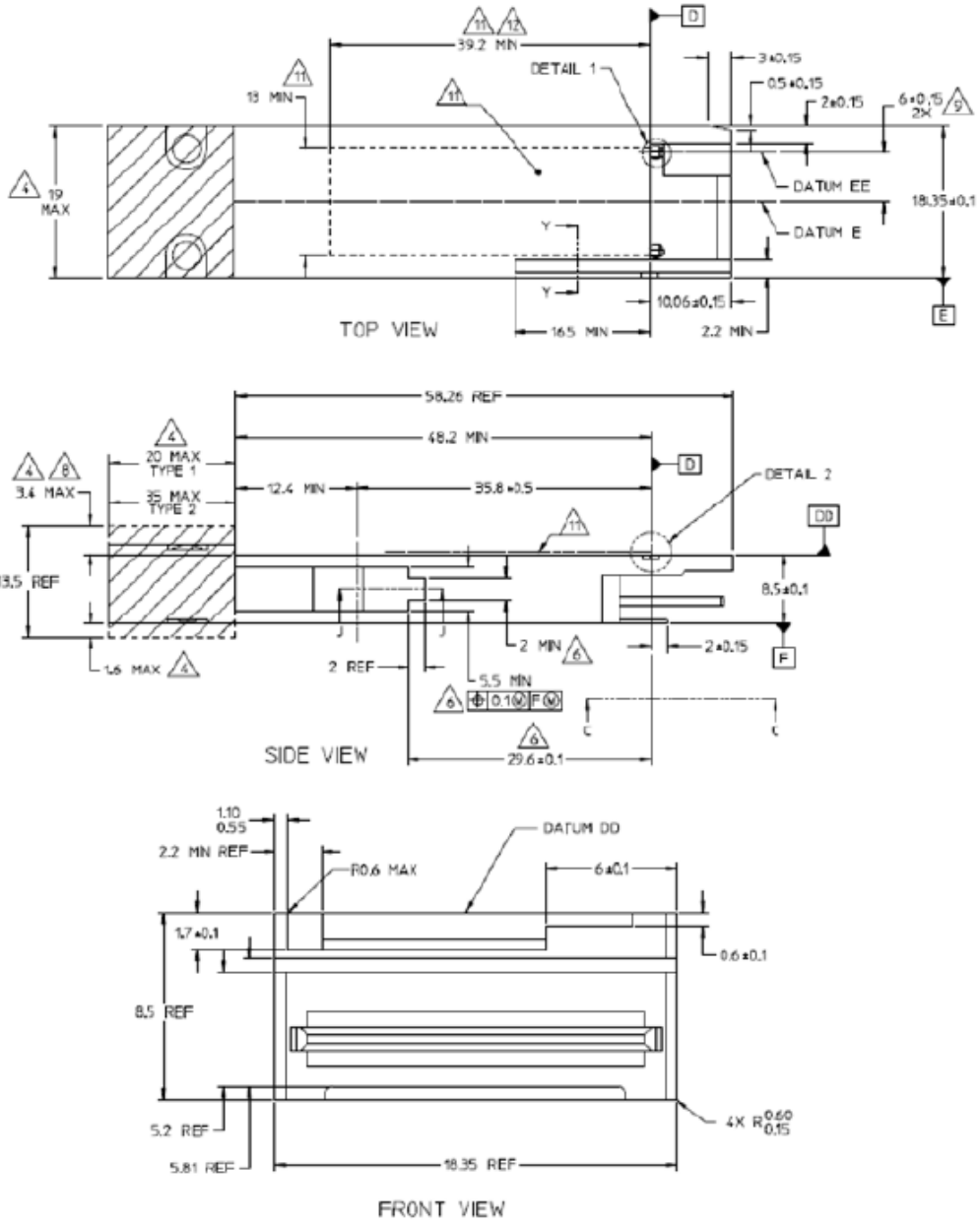
Pin-Out Details



MPO Connector Receptacle



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



U.S. Headquarters

Email: sales@addonnetworks.com

Telephone: +1 877.292.1701

Fax: 949.266.9273

Europe Headquarters

Email: salesemea@addonnetworks.com

Telephone: +44 1285 842070