MCA4J80-N004-AO

NVIDIA® MCA4J80-N004 Compatible TAA 800GBase-CU OSFP to OSFP Direct Attach Cable (Active Twinax, 4m) Infiniband Only

Features:

- Compliant to OSFP MSA Specifications
- Infiniband NDR Compatible
- PAM4 106.25Gbps Transmission Per Channel
- Enables Auto-Negotiation and Link Training
- 3.3V Power Supply
- Low Power Consumption
- Low Latency:
- Linear PAM4 Programmable Equalizer Optimized for 56GBaud Copper Link
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius



Applications:

- 800GBase Ethernet

Product Description

This is an NVIDIA® MCA4J80-N004 compatible 800GBase-CU OSFP to OSFP direct attach cable that operates over active copper with a maximum reach of 4.0m (13.1ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

General Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Tstg	-40		85	℃
Operating Case Temperature	Tc	0		70	℃
Supply Voltage	Vcc	-0.3	3.3	3.6	V
Relative Operating Humidity	RH	5		85	%
Data Rate	DR		800		Gbps

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Length	L			4	M	
AWG			25		AWG	
Jacket Material		Plastic Braided Mesh Technology Net				

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.1	3.3	3.5		
Input Amplitude		800		1200	mVp-p	
Input Low Voltage	VIL	-0.3		0.35 x Vcc	V	
Input High Voltage	VIH	0.65 x Vcc		Vcc + 0.3	V	
Output Logic - Low	VOL			0.25 x Vcc	V	
I2C Master-Mode Output			400		kHz	
Power Consumption			1.2	1.5	W	
Raw Cable Impedance	Zca	90	100	110	Ω	
Mated Connector Impedance	Zmated	85	100	115	Ω	
Maximum Insertion Loss @26.56GHz	SDD21	11		19.75	dB	
Differential to Common-Mode Return Loss	SDD11/22	$RLcd(f) \geq \begin{cases} 22 - 10(f/26.56) & 0.05 \leq f < 26.56 \\ 15 - 3(f/26.56) & 26.56 \leq f \leq 40 \end{cases}$			dB	1
Differential to Common-Mode Conversion Loss	SCD11/22	$Conversion_loss(f) - \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14 - 0.3108f & 12.89 \leq f \leq 40 \end{cases}$			dB	1
Common-Mode to Common-Mode Return Loss	SCD21-SDD21	$RLcc(f) \geq 1.08$			dB	1
Minimum COM	COM	3			dB	
Minimum Cable Assembly	ERL	8.25			dB	
BER				2.4×10^{-4}		

Notes:

1. For $0.05 \leq f \leq 40$GHz, where f is the frequency in GHz.

Pin Descriptions

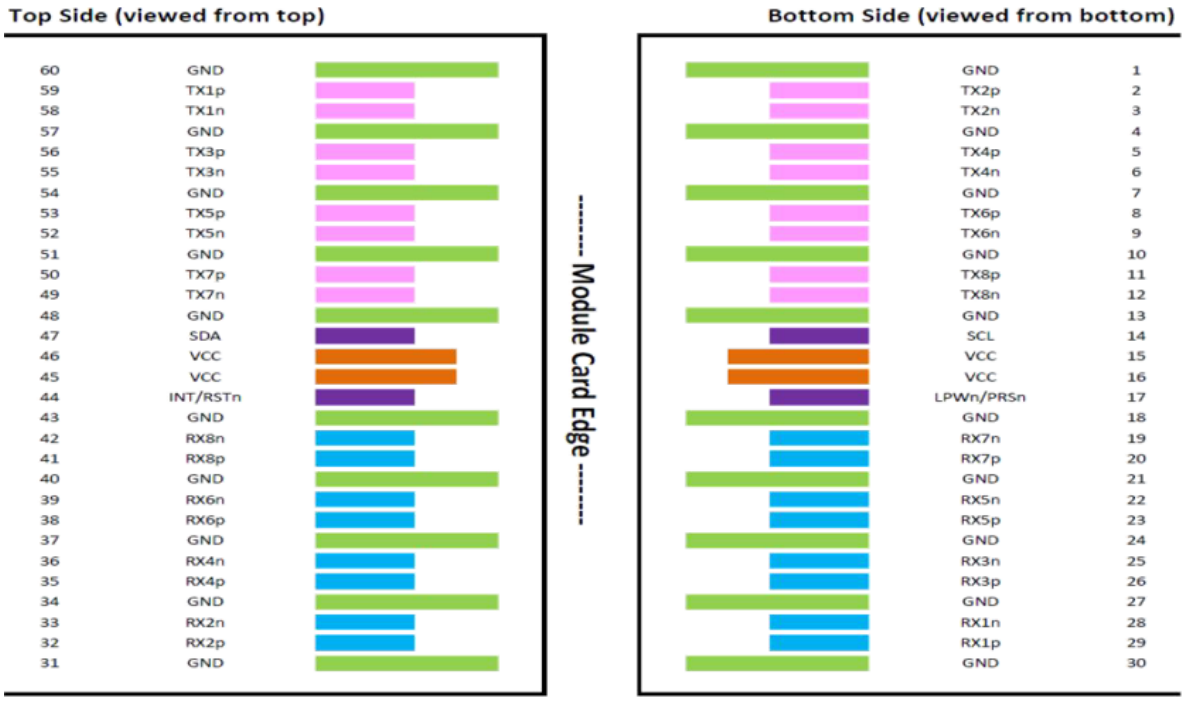
Pin	Symbol	Name/Description	Logic	Plug Sequence	Direction	Notes
1	GND	Module Ground.		1		
2	Tx2+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
3	Tx2-	Transmitter Data Inverted.	CML-I	3	Input from Host	
4	GND	Module Ground.		1		
5	Tx4+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
6	Tx4-	Transmitter Data Inverted.	CML-I	3	Input from Host	
7	GND	Module Ground.		1		
8	Tx6+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
9	Tx6-	Transmitter Data Inverted.	CML-I	3	Input from Host	
10	GND	Module Ground.		1		
11	Tx8+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
12	Tx8-	Transmitter Data Inverted.	CML-I	3	Input from Host	
13	GND	Module Ground.		1		
14	SCL	2-Wire Serial Interface Clock.	LVCMOS-I/O	3	Bi-Directional	1
15	Vcc	+3.3V Power.		2	Power from Host	
16	Vcc	+3.3V Power.		2	Power from Host	
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3	Bi-Directional	2
18	GND	Module Ground.		1		
19	Rx7-	Receiver Data Inverted.	CML-O	3	Output from Host	
20	Rx7+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
21	GND	Module Ground.		1		
22	Rx5-	Receiver Data Inverted.	CML-O	3	Output from Host	
23	Rx5+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
24	GND	Module Ground.		1		
25	Rx3-	Receiver Data Inverted.	CML-O	3	Output from Host	
26	Rx3+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
27	GND	Module Ground.		1		
28	Rx1-	Receiver Data Inverted.	CML-O	3	Output from Host	
29	Rx1+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
30	GND	Module Ground.		1		
31	GND	Module Ground.		1		
32	Rx2+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
33	Rx2-	Receiver Data Inverted.	CML-O	3	Output from Host	
34	GND	Module Ground.		1		
35	Rx4+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	

36	Rx4-	Receiver Data Inverted.	CML-O	3	Output from Host	
37	GND	Module Ground.		1		
38	Rx6+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
39	Rx6-	Receiver Data Inverted.	CML-O	3	Output from Host	
40	GND	Module Ground.		1		
41	Rx8+	Receiver Data Non-Inverted.	CML-O	3	Output from Host	
42	Rx8-	Receiver Data Inverted.	CML-O	3	Output from Host	
43	GND	Module Ground.		1		
44	INT/RSTn	Module Interrupt/Module Reset.	Multi-Level	3	Bi-Directional	2
45	Vcc	+3.3V Power.		2	Power from Host	
46	Vcc	+3.3V Power.		2	Power from Host	
47	SDA	2-Wire Serial Interface Data.	LVCMOS-I/O	3	Bi-Directional	1
48	GND	Module Ground.		1		
49	Tx7-	Transmitter Data Inverted.	CML-I	3	Input from Host	
50	Tx7+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
51	GND	Module Ground.		1		
52	Tx5-	Transmitter Data Inverted.	CML-I	3	Input from Host	
53	Tx5+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
54	GND	Module Ground.		1		
55	Tx3-	Transmitter Data Inverted.	CML-I	3	Input from Host	
56	Tx3+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
57	GND	Module Ground.		1		
58	Tx1-	Transmitter Data Inverted.	CML-I	3	Input from Host	
59	Tx1+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
60	GND	Module Ground.		1		

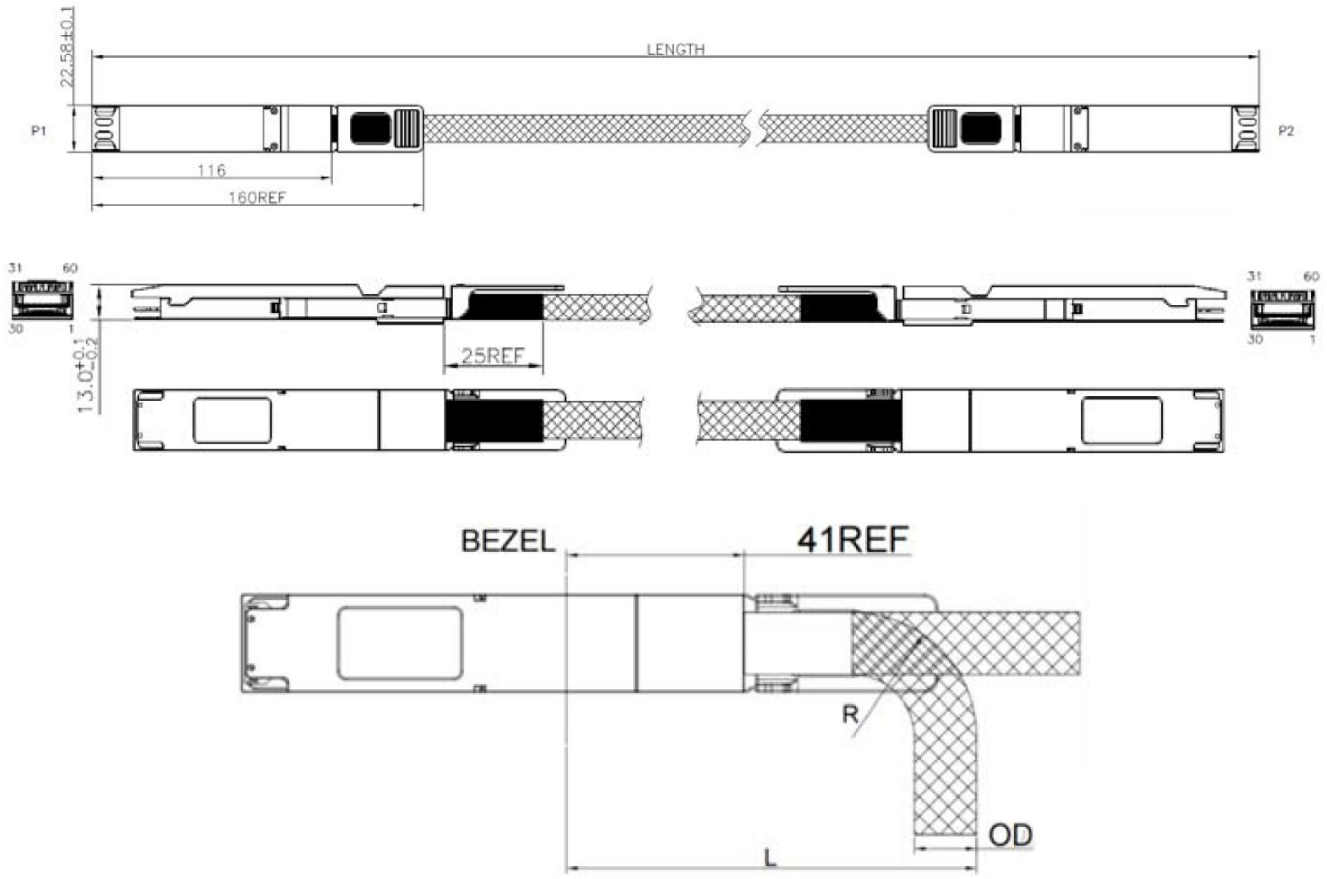
Notes:

1. Open-drain with pull-up resistor on the host.
2. See “Pin Assignments” below for the required circuit.

Pin Assignments



Mechanical Specifications



Bending Radius

Wire Gauge	OD (Ref.)	Bend Radius "R"	Min. Bend Radius "L"
25AWG	12.1mm	25mm	86mm

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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