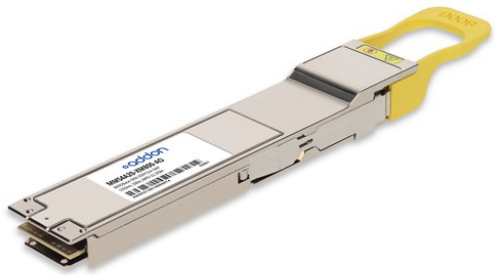
MMS4A20-XM800-AO

NVIDIA® MMS4A20-XM800 Compatible TAA 800GBase-DR4 OSFP224-RHS Transceiver (SMF, 1310nm, 500m, MPO-12, DOM, CMIS 5.3)

Features:

- OSFP MSA Package
- 4x212Gbps PAM4 Electrical Interface
- Low EMI and Excellent ESD Protection
- Power Consumption: 15W
- 3.3V Power Supply
- Up to 500m Transmission on Single-Mode Fiber
- Operating Temperature: 0 to 70 Celsius
- Hot-Pluggable
- RoHS Compliant and Lead-Free



Applications:

- 800GBase Ethernet

Product Description

This NVIDIA® MMS4A20-XM800 compatible OSFP224 transceiver provides 800GBase-DR4 throughput up to 500m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a MPO-12 connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Operating Relative Humidity	RH	5		85	%	
Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Receiver Damage Threshold Per Lane		5			dBm	
Data Rate Per Lane	DR	106.25 ± 50ppm			GBd	
Modulation Format		PAM4				

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Supply Current	Icc			4785	mA	
Power Dissipation	PD			15	W	
Transmitter						
Differential Pk-Pk Input Voltage	VIN,pp			1	V	
DC Common-Mode Voltage	Vcm	0		1	V	
Differential Termination Resistance Mismatch	Rdm	-10		10	%	
Receiver						
Differential Pk-Pk Input Voltage	VOUT,pp			1	V	
DC Common-Mode Voltage	Vcm	0		1	V	
Differential Termination Resistance Mismatch		-10		10	%	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λ	1304.5	1311	1317.5	nm	
Average Launch Power Per Lane	Pavg	-3.3		4	dBm	
Optical Modulation Amplitude (OMA) Per Lane	OMA	-0.3		4.2	dBm	
Extinction Ratio	ER	3.5			dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Launch Power in OMA Minus TDECQ Per Lane		-1.2			dB	
Transmitter and Dispersion Eye Closure for PAM4 Per Lane	TDECQ			3.4	dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of Off Transmitter Per Lane				-15	dBm	
Receiver						
Center Wavelength	λC	1304.5	1311	1317.5	nm	
Average Receiver Power Per Lane	PIN	-6.3		4	dBm	
Receiver Power Per Lane (OMA)				4.2	dBm	
Receiver Sensitivity (OMAouter) Per Lane	SEN			Max. (-3.4, TECQ-4.3)	dBm	1
Stressed Receiver Sensitivity (OMAouter) Per Lane Maximum				-0.9	dBm	
Receiver Reflectance				-26	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-Assert	LOSD			-9	dBm	
LOS Hysteresis	LOSH	0.5		3	dB	

Notes:

1. Receiver sensitivity (OMAouter), per lane (maximum), is informative and defined for a transmitter with TECQ of 0.9dB. Receiver sensitivity (OMAouter) per lane for TECQ<0.9dB, maximum=3.4dBm. For 0.9dB≤TECQ≤SECQ, maximum=TECQ-4.3dBm.

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
MgmtInitDuration	Max. MgmtInitDuration			2000	ms	1
ResetL Assert Time	t_reset_init	10			µs	2
IntL Assert Time	ton_IntL			200	ms	3
IntL De-Assert Time	toff_IntL			500	µs	4
Rx_LOS Assert Time	ton_los			100	ms	5
Flag Assert Time	ton_flag			200	ms	6
Mask Assert Time	ton_mask			100	ms	7
Mask De-Assert Time	toff_mask			100	ms	8

Notes:

1. Time from power on, hot plug, or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
4. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes de-assert times for Rx_LOS, Tx_Fault, and other flag bits.
5. Time from Rx_LOS state to Rx_LOS bit is set (value=1b), and the IntL is asserted.
6. Time from occurrence of condition triggering flag to associated flag bit is set (value=1b), and the IntL is asserted.
7. Time from mask bit is set (value=1b) until the associated IntL assertion is inhibited.
8. Time from mask bit is cleared (value=0b) until the associated IntL operation resumes.

Surge Current Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Power Supply Voltage Including Ripple, Droop, and Noise Below 100kHz	Vcc_Module	3.135	3.3	3.465	V	
Host Power Supply Voltage Including Ripple, Droop, and Noise Below 100kHz	Vcc_Host	3.135	3.3	3.465	V	
Module Power Supply Noise Tolerance 10Hz to 10MHz (Peak-to-Peak) Voltage Drop Across Mated Connector (Vcc_Host – Vcc_Module)	Vcc_drop			66	mV	
Total Current for Vcc Pins	Icc_module			10	A	1
Host RMS Noise Output 10Hz to 10MHz	e N_Host			25	mV	
Module RMS Noise Output 10Hz to 10MHz	e N_Mod			15	mV	
Module In-Rush to Instantaneous Peak Duration	T_ip			50	µs	
Module In-Rush to Initialization Time	T_init			500	ms	
In-Rush and Discharge Current	I_didt			100	mA/µs	2
High-Power Mode to Low-Power Mode Transition Time From Assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs	

Notes:

1. Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure that the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.
2. The specified in-rush and discharge current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power, and high-power to low-power.

Pin Descriptions

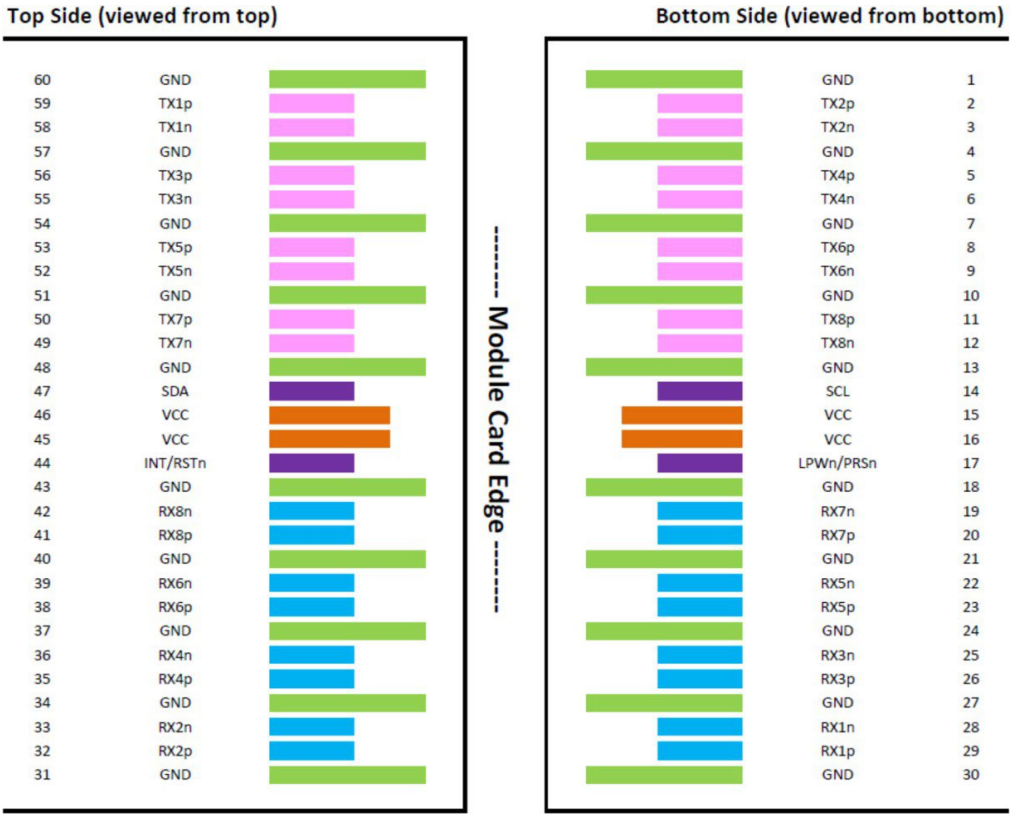
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2+	Transmitter Non-Inverted Data.	3	
3	CML-I	Tx2-	Transmitter Inverted Data.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4+	Transmitter Non-Inverted Data.	3	
6	CML-I	Tx4-	Transmitter Inverted Data.	3	
7		GND	Module Ground.	1	1
8					
9					
10		GND	Module Ground.	1	1
11					
12					
13		GND	Module Ground.	1	1
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	2
15		Vcc	+3.3V Power Supply.	2	
16		Vcc	+3.3V Power Supply.	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	3	3
18		GND	Module Ground.	1	1
19					
20					
21		GND	Module Ground.	1	1
22					
23					
24		GND	Module Ground.	1	1
25	CML-O	Rx3-	Receiver Inverted Data.	3	
26	CML-O	Rx3+	Receiver Non-Inverted Data.	3	
27		GND	Module Ground.	1	1
28	CML-O	Rx1-	Receiver Inverted Data.	3	
29	CML-O	Rx1+	Receiver Non-Inverted Data.	3	
30		GND	Module Ground.	1	1
31		GND	Module Ground.	1	1
32	CML-O	Rx2+	Receiver Non-Inverted Data.	3	
33	CML-O	Rx2-	Receiver Inverted Data.	3	
34		GND	Module Ground.	1	1
35	CML-O	Rx4+	Receiver Non-Inverted Data.	3	

36	CML-O	Rx4-	Receiver Inverted Data.	3	
37		GND	Module Ground.	1	1
38					
39					
40		GND	Module Ground.	1	1
41					
42					
43		GND	Module Ground.	1	1
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	3	3
45		Vcc	+3.3V Power Supply.	2	
46		Vcc	+3.3V Power Supply.	2	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	2
48		GND	Module Ground.	1	1
49					
50					
51		GND	Module Ground.	1	1
52					
53					
54		GND	Module Ground.	1	1
55	CML-I	Tx3-	Transmitter Inverted Data.	3	
56	CML-I	Tx3+	Transmitter Non-Inverted Data.	3	
57		GND	Module Ground.	1	1
58	CML-I	Tx1-	Transmitter Inverted Data.	3	
59	CML-I	Tx1+	Transmitter Non-Inverted Data.	3	
60		GND	Module Ground.	1	1

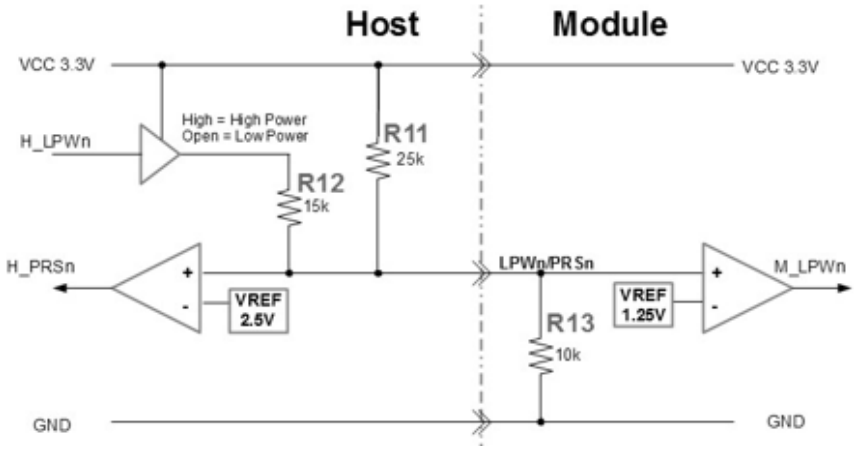
Notes:

1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. SCL and SDA are 2-wire serial interfaces between the host and the module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal, and SDA is defined as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1kΩ to 4.7kΩ depending on the capacitive load.
3. LPWn/PRSn is a dual-function signal that allows the host to signal low-power mode and allows the module to indicate that the module is present. The circuit shown in the “LPWn/PRSn Circuit” enables multi-level signaling to provide direct signal control in both directions. Low-power mode is an active-low signal on the host which gets converted to an active-low signal on the module. “Module Present” is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

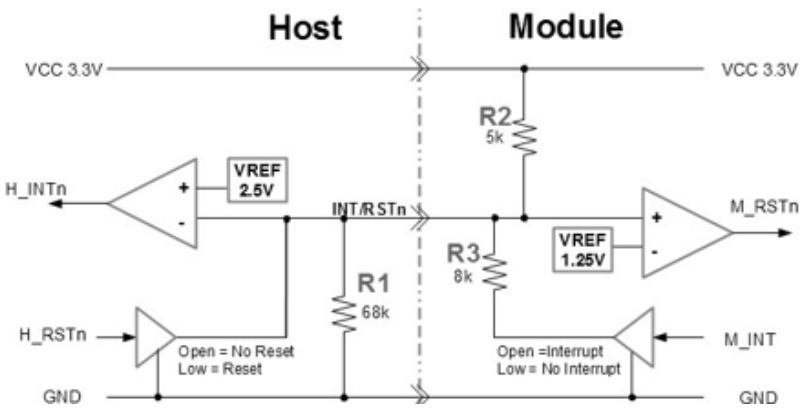
Host Board Connector



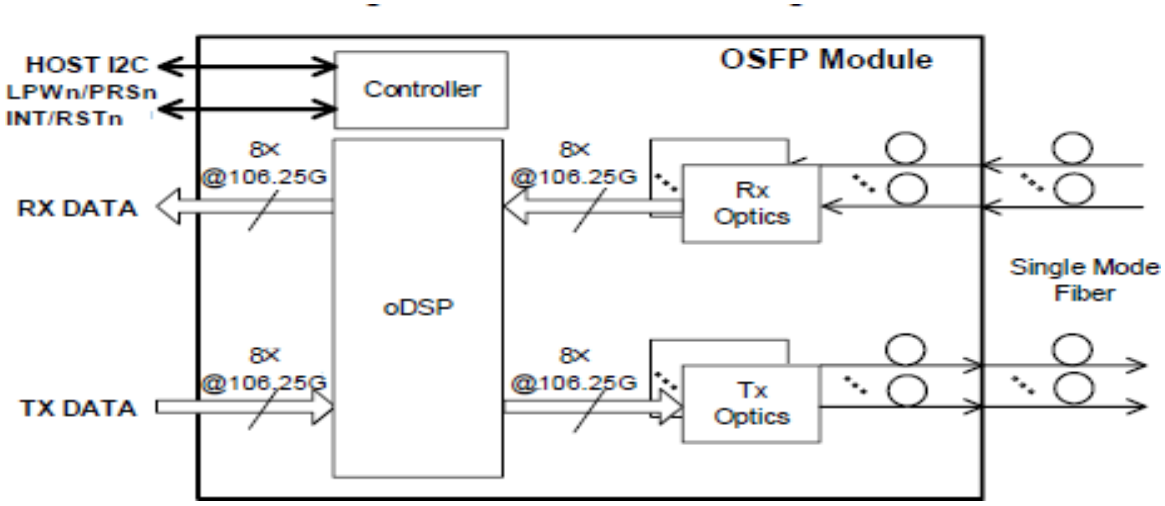
LPWn/PRSn Circuit



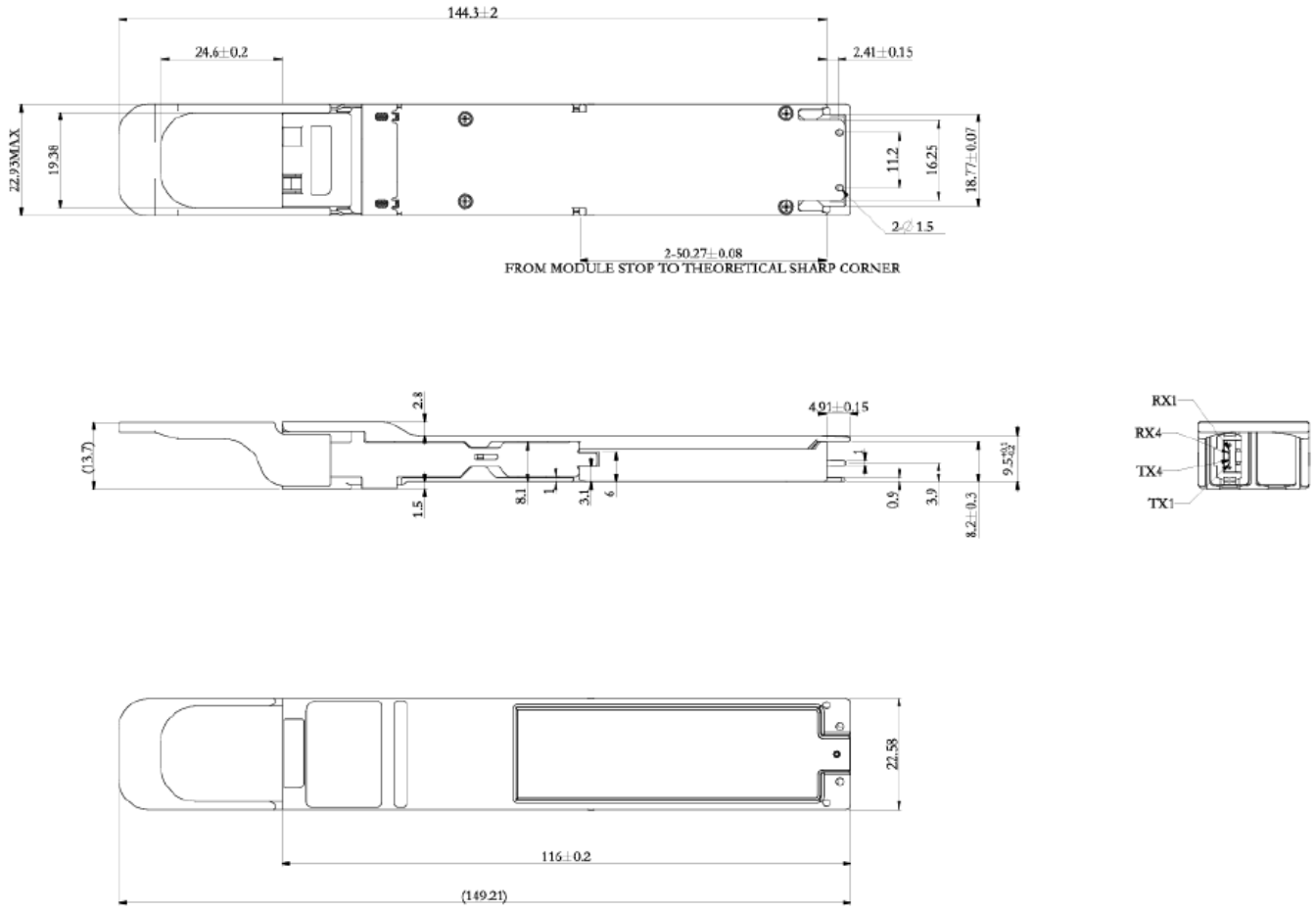
INT/RSTn Circuit



Block Diagram



Mechanical Specifications



Notes:

1. Tolerance: +/- 0.1MM.
2. Other according with OSFP MSA.
3. Light port according with fiber connector specifications.
4. Unit: mm.

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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