QDD4-400GB-SR4-MX-AO

NVIDIA® Compatible TAA 400GBase-SR4 PAM4 112G QSFP-DD Transceiver (MMF, 850nm, 100m, MPO-12, DOM, CMIS 4.0)

Features:

- 53.125 GBd PAM4 4 channel 400G-SR4 Optical interface
- Compliant with IEEE 802.3ck and IEEE 802.3db
- 26.5625 GBd PAM4 8 channel 400G AUI-8 C2M Electrical interface
- Multi-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- QSFP-DD MSA package with MPO-12 APC
- Metal with Lower EMI
- Hot Pluggable
- CMIS Rev4.0
- Excellent ESD Protection
- RoHS Compliant and Lead Free



Applications:

- 400GBase Ethernet

Product Description

This NVIDIA® compatible QSFP-DD transceiver provides 400GBase-SR4 throughput up to 100m over multi-mode fiber (MMF) PAM4 112G using a wavelength of 850nm via an MPO-12 connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with NVIDIA®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	Vcc	3.1	3.3	3.5	V	
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Operating Relative Humidity	RH	5		85	%	1
Optical Input Power	PIN			5	dBm	

Notes:

1. Non-condensing.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			2640	mA	
Module Power Dissipation	P			8	W	
Transmitter						
Differential Input Impedance	ZIN		100		Ω	
Receiver						
Differential output Impedance	Zos	90	100	110	Ω	
Common-Mode to Differential-Mode Return Loss	RLdc		Note 1		dB	
Transition Time, 20 to 80%	Tr, Tf	8.5			ps	

Notes:

1. $$RLdc(f) \geq \begin{cases} 25 - 22(f/53.125) & 0.05 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases}$$

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Optical Data Rate per channel (PAM4)	DR		53.125		GBd	
Frequency Tracking	Ft	-100		100	ppm	
Center Wavelength	λC	844	850	863	nm	
RMS Spectral Width				0.6	nm	1
Laser Off Power	Poff			-30	dBm	
Average Optical Power	Pavg	-4.6		4	dBm	
Extinction Ratio	ER	2.5			dB	
Transmitter and Dispersion Eye Closure	TDECQ			4.4	dB	
Outer Optical Modulation Amplitude	OMAouter	-2.6		3.5	dBm	2
Encircled Flux, Each Lane			≥ 86% @ 19 μm ≤ 30% @ 4.5 μm		dB	3
Optical Return Loss Tolerance	ORLT			14	dB	
Receiver						
Electrical Data Rate Per Channel (PAM4)	DR		26.5625		GBd	
Frequency Tracking	Ft	-100		100	ppm	
Center Wavelength	λr	842	850	948	nm	
Damage Threshold		5			dBm	
Average Receive Power		-6.4		4	dBm	4
Receiver Reflectance				-15	dB	
Differential Data Output Voltage Peak to Peak Swing	Vopp	600		845	mV	
Receiver Sensitivity (OMAouter) (max) **For TECQ≤1.8dB** **For 1.8dB＜TECQ≤4.4dB**	RS			 -4.6 -6.4+TECQ	 dBm dBm	
Eye Height	EH	15			mV	
Vertical Eye Closure	VEC			12	dB	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Even if the TDECQ<1.8dB, the OMA (min) must exceed this value.
3. If measured into type A1a.2, type A1a.3 or type A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
   Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.6dB.

Pin Descriptions

Pin	Logic	Symbol	Name/Descriptions	Notes
1		GND	Ground	
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	3.3V Power Supply Receiver	2
11	LVCMOS–I/O	SCL	2 Wire Serial Interface Clock	
12	LVCMOS–I/O	SDA	2 Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3n	Transmitter Inverted Data Output	
15	CML-O	Rx3p	Transmitter Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1n	Transmitter Inverted Data Output	
18	CML-O	Rx1p	Transmitter Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Transmitter Inverted Data Output	
22	CML-O	Rx2p	Transmitter Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Transmitter Inverted Data Output	
25	CML-O	Rx4p	Transmitter Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccRx	3.3V Power Supply Transmitter	2
30		Vcc l	3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	
32		GND	Ground	1
33	CML-I	Tx1n	Transmitter Inverted Data Input	
34	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1n	Transmitter Inverted Data Input	

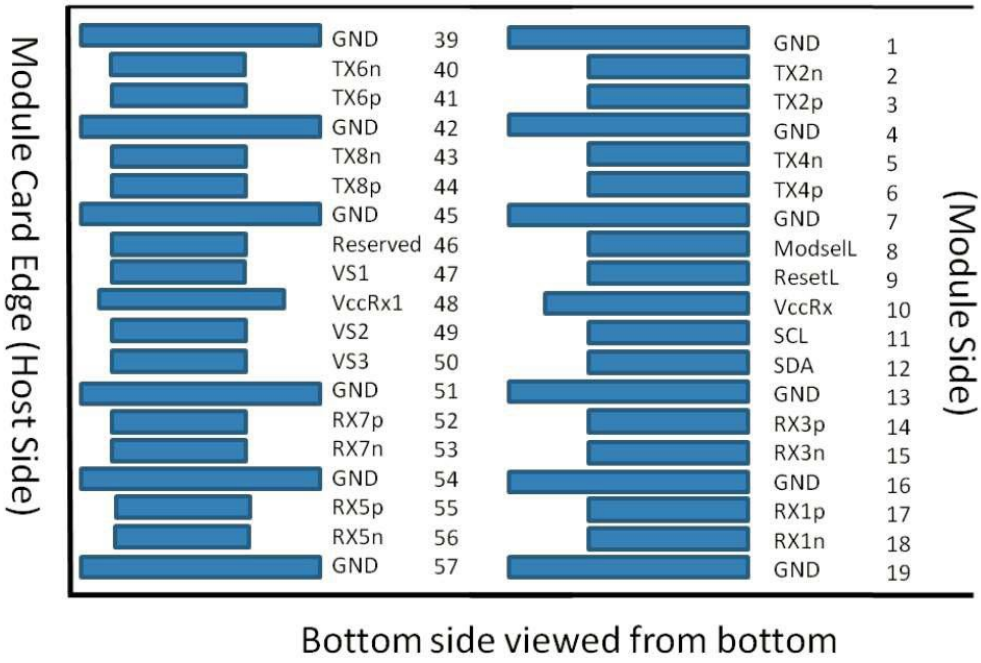
37	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	NC	3
47		VS1	NC	3
48		VccRx1	3.3V Power Supply	2
49		VS2	NC	3
50		VS3	NC	3
51		GND	Ground	1
52	CML-O	Rx7n	Transmitter Inverted Data Output	
53	CML-O	Rx7p	Transmitter Non-Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5n	Transmitter Inverted Data Output	
56	CML-O	Rx5p	Transmitter Non-Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Transmitter Inverted Data Output	
60	CML-O	Rx6p	Transmitter Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Transmitter Inverted Data Output	
63	CML-O	Rx8p	Transmitter Non-Inverted Data Output	
64		GND	Ground	1
65		NC	NC	3
66		Reserved	NC	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	NC	3
70		GND	Ground	1
71	CML-I	Tx7n	Transmitter Inverted Data Input	
72	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5n	Transmitter Inverted Data Input	
75	CML-I	Tx5p	Transmitter Non-Inverted Data Input	

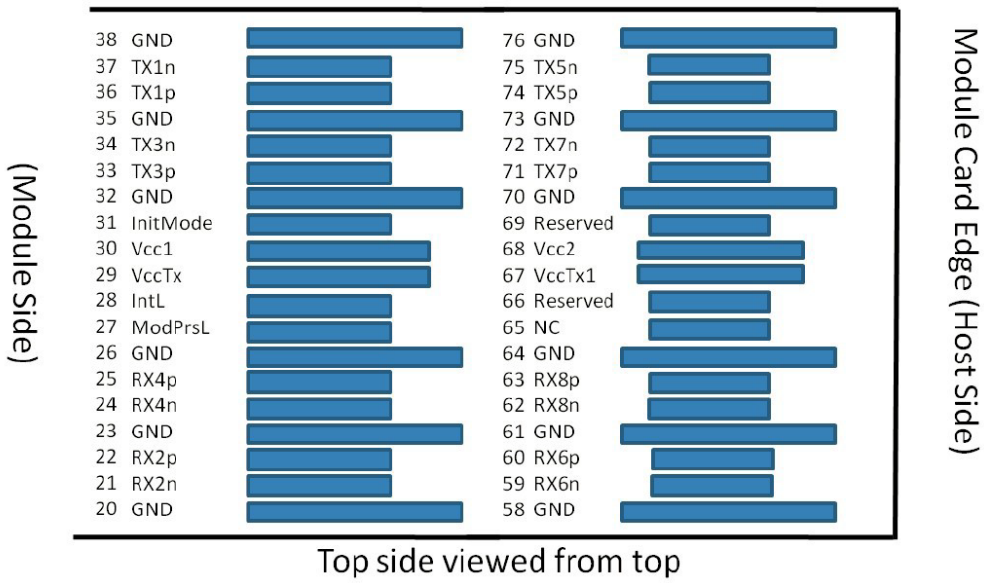
76		GND	Ground	1

Notes:

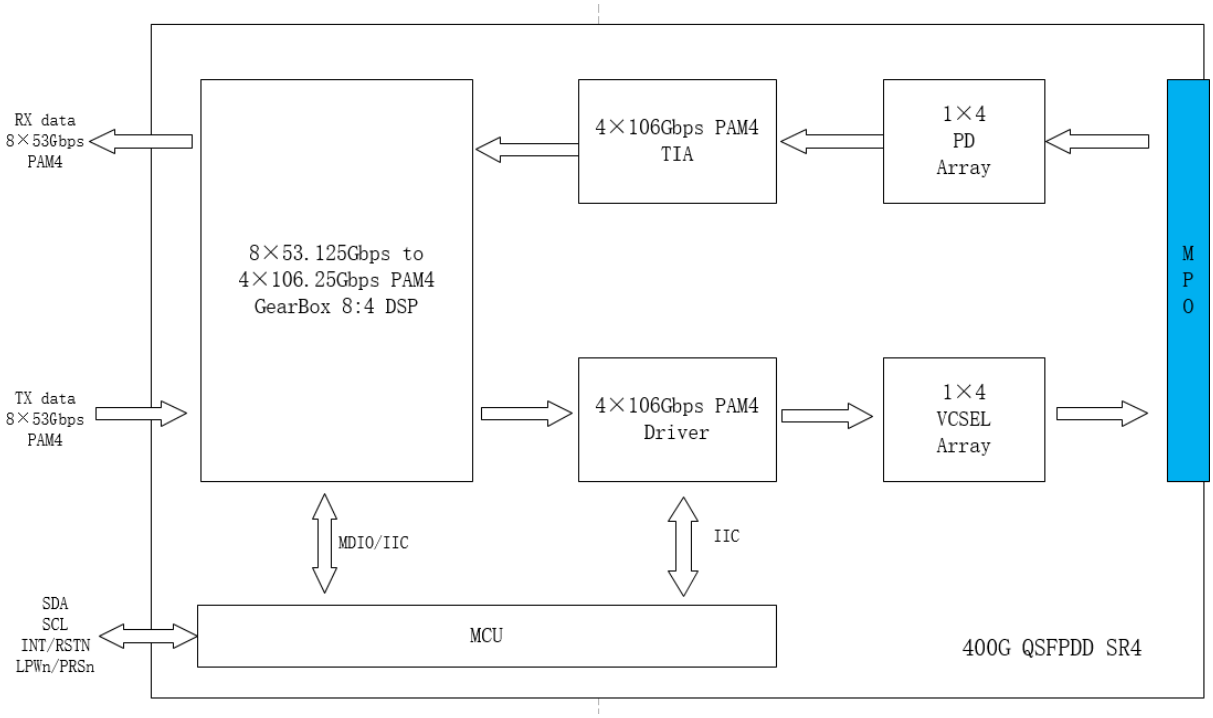
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Electrical Pin-Out Details

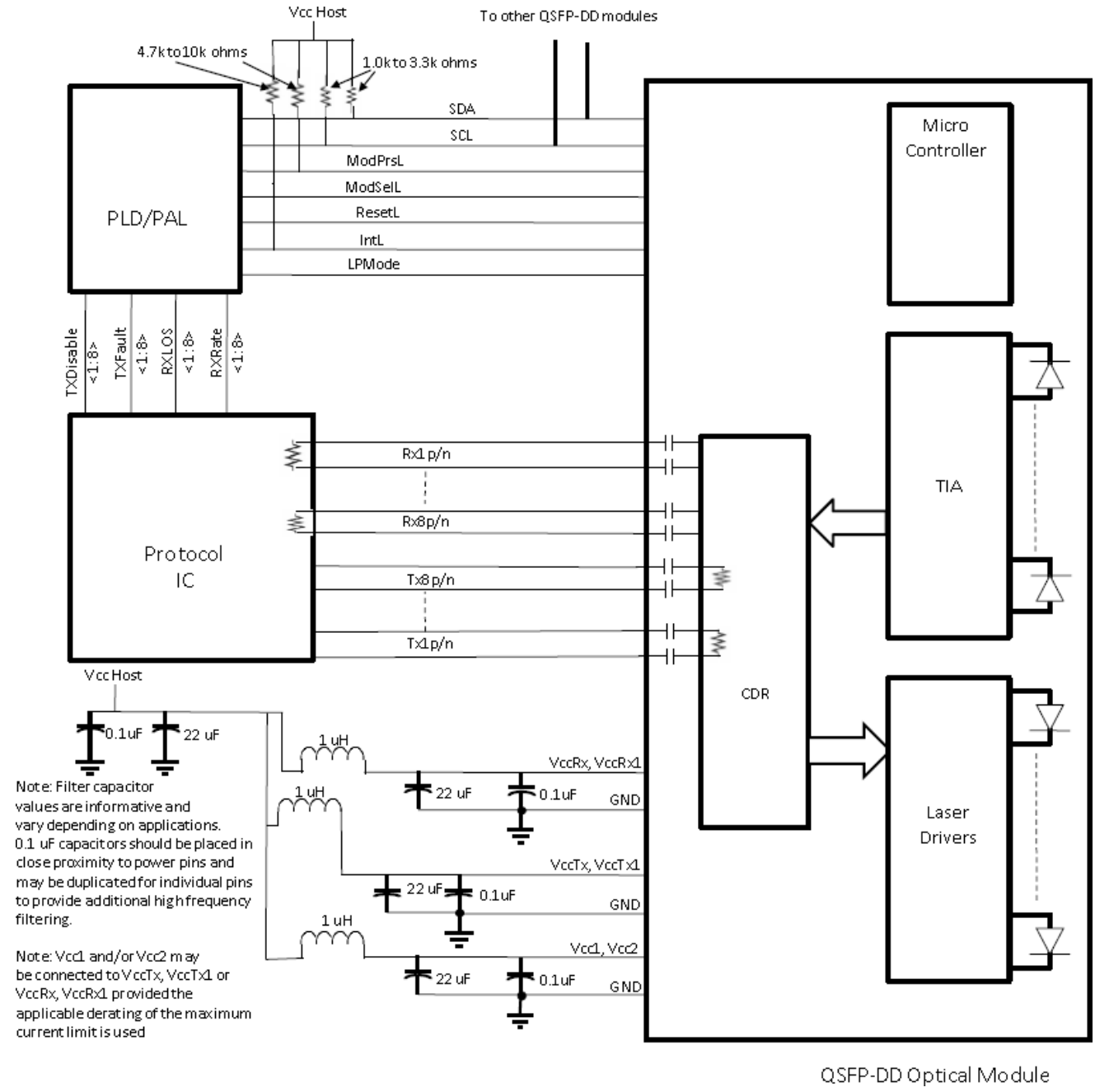




Transceiver Block Diagram

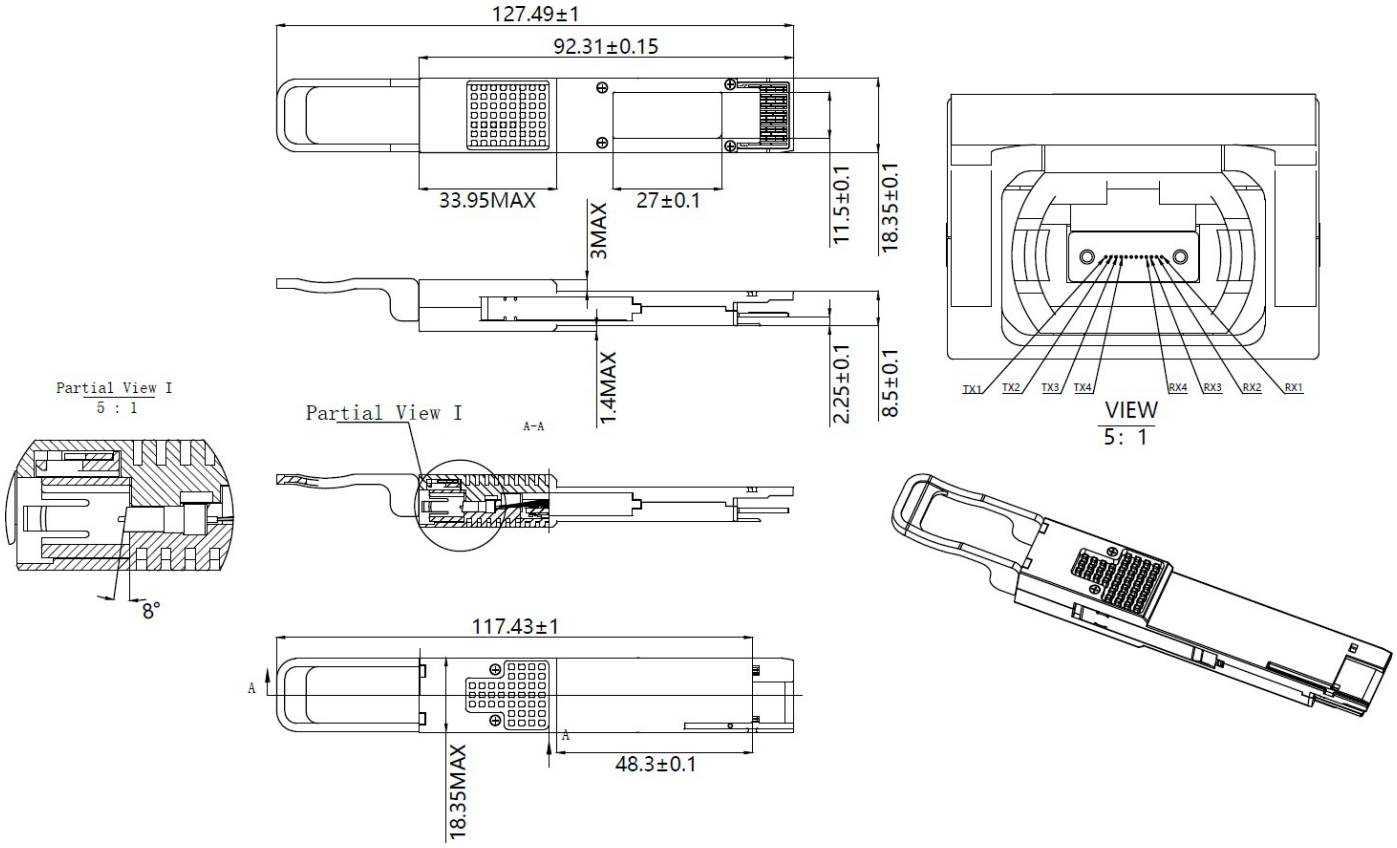


Recommended Interface Circuit



QSFP-DD Optical Module

Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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