**OSFPRHS-400GB-VR4-VDM-MX-AO**

NVIDIA® Compatible TAA 400GBase-VR4 PAM4 OSFP112 RHS Transceiver (MMF, 850nm, 50m, MPO-12, DOM, CMIS 5.2, VDM)

**Features:**

- 4 x100Gbps MMF Optical Interface
- Up to 50m Link on OM4 Multi-Mode Fiber
- Each Electrical Channel Data Rate Up to 53.125Gbaud w/CDR
- CML Compatible Electrical I/O
- OSFP MSA Compliant
- 850nm VCSEL and PD Array Technology
- MPO-12 APC Optical Receptacle Type
- CMIS 5.2 Compliant
- Operating Temperature: 15 to 70 Celsius
- Hot-Pluggable
- RoHS Compliant and Lead-Free



**Applications:**

- Advance Monitoring Capable Transceiver
- 400GBase Ethernet

**Product Description**

This NVIDIA® compatible OSFP112 RHS transceiver provides 400GBase-VR4 throughput up to 50m over multi-mode fiber (MMF) using a wavelength of 850nm via a MPO-12 connector with VDM. It can operate at temperatures between 15 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with NVIDIA®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

**Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| **Storage Temperature** | Tstg | -40 | +85 | °C | |
| **Relative Humidity – Storage** | RHs | 0 | 85 | % | 1 |
| **Relative Humidity – Operating** | RHo | 0 | 85 | % | 1 |
| **Module Supply Voltage** | Vcc | -0.5 | 3.6 | V | |

**Notes:**

1. RH is a non-condensing condition.
2. Exceeding the Absolute Maximum Ratings may cause irreversible damage to the device. The device is not intended to be operated under the condition of simultaneous Absolute Maximum Ratings, a condition which may cause irreversible damage to the device.

**Recommended Operating Conditions**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Operating Case Temperature** | Tc | 15 | 25 | 70 | °C | 1 |
| **Module Supply Voltage** | Vcc | 3.135 | 3.3 | 3.465 | V | |
| **Power Consumption** | P | | | 10 | W | 2 |
| **Module Supply Current** | $I_{IN}$ | | 2424 | | mA | |
| **Electrical Signal Rate** | Se | | 53.125 | | GBd | 3 |
| **Optical Signal Rate** | So | | 53.125 | | GBd | 3 |

**Notes:**

1. Temperature range = C.
2. Power Class 5.
3. ±100ppm, each lane.

## Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| **Signaling Rate** | SR | | 53.125 | | GBd | 1 |
| **Tx_Data Differential Input Voltage** | VIN | | | 900 | mV | |
| **Tx_Data Differential Input Impedance** | ZIN | | 100 | | Ω | |
| **Receiver** | | | | | | |
| **Signaling Rate** | SR | | 53.125 | | GBd | 1 |
| **Rx_Data Differential Output Voltage** | VOUT | | | 900 | mV | |
| **Rx_Data Differential Output Impedance** | ZOUT | | 100 | | Ω | |

**Notes:**

1. ±100ppm, each lane.

## Optical Characteristics

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | | |
| **Signaling Rate** | | SR | | 53.125 | | GBd | 1 |
| **Modulation Format** | | MF | | PAM4 | | | |
| **Center Wavelength** | | λ | 840 | | 870 | nm | |
| **RMS Spectral Width** | | Δλ | | | 0.65 | nm | |
| **Average Launch Power** | | POUT | -4.6 | | 4 | dBm | 2 |
| **Outer Optical Modulation Amplitude** | **For Max. (TECQ, TDECQ) ≤ 1.8dB** | OMAouter | -2.6 | | 3.5 | dBm | 2 |
| | **For 1.8 ≤ Max. (TECQ, TDECQ) ≤ 4.4dB** | | -4.4 + Max. (TECQ, TDECQ) | | | | |
| **Transmitter and Dispersion Eye Closure for PAM4** | | TDECQ | | | 4.4 | dB | 2 |
| **Transmitter Eye Closure for PAM4 (TECQ)** | | TECQ | | | 4.4 | dB | 2 |
| **Over/Under-Shoot** | | O/Ushoot | | | 29 | % | 2 |
| **Transmitter Power Excursion** | | TPE | | | 2.3 | dB | 2 |
| **Extinction Ratio** | | ER | 2.5 | | | dB | 2 |
| **Transmitter Transition Time** | | Time | | | 17 | ps | 2 |
| **Average Launch Power of Off Transmitter** | | Poff | | | -30 | dBm | 2 |
| **$RIN_{14}OMA$** | | $RIN_{14}OMA$ | | | -132 | dB/Hz | |
| **Optical Return Loss Tolerance** | | ORLT | | | 14 | dB | |
| **Encircled Flux** | | EF | >=86% at 19μm<br><=30% at 4.5μm | | | | |

| Receiver | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Signaling Rate** | | SR | | 53.125 | | GBd | 1 |
| **Modulation Format** | | MF | | PAM4 | | | |
| **Center Wavelength** | | λ | 842 | | 948 | nm | |
| **Damage Threshold** | | PDamage | 5 | | | dBm | |
| **Average Receive Power** | | PIN | -6.3 | | 4 | dBm | 3 |
| **Receive Power (OMAouter)** | | PIN(OMAouter) | | | 3.5 | dBm | 2 |
| **Receiver Reflectance** | | RF | | | -15 | dB | |
| **Receiver Sensitivity (OMAouter)** | **For TECQ ≤ 1.8dB** | Sens(OMAouter) | | | -4.4 | dBm | 4 |
| | **For 1.8B ≤ TECQ ≤ 3.4dB** | | | | -6.2+TECQ | | |
| **Stressed Receiver Sensitivity (OMAouter) Per Lane** | | Stressed-Sens (OMAouter) | | | -1.8 | dBm | 4 |

**Notes:**

1. ±100ppm, each lane.
2. Each lane.
3. Each lane. Average receive power, per lane (minimum), is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Each lane. BER @ $2.4E^{-4}$.

**Pin Descriptions**

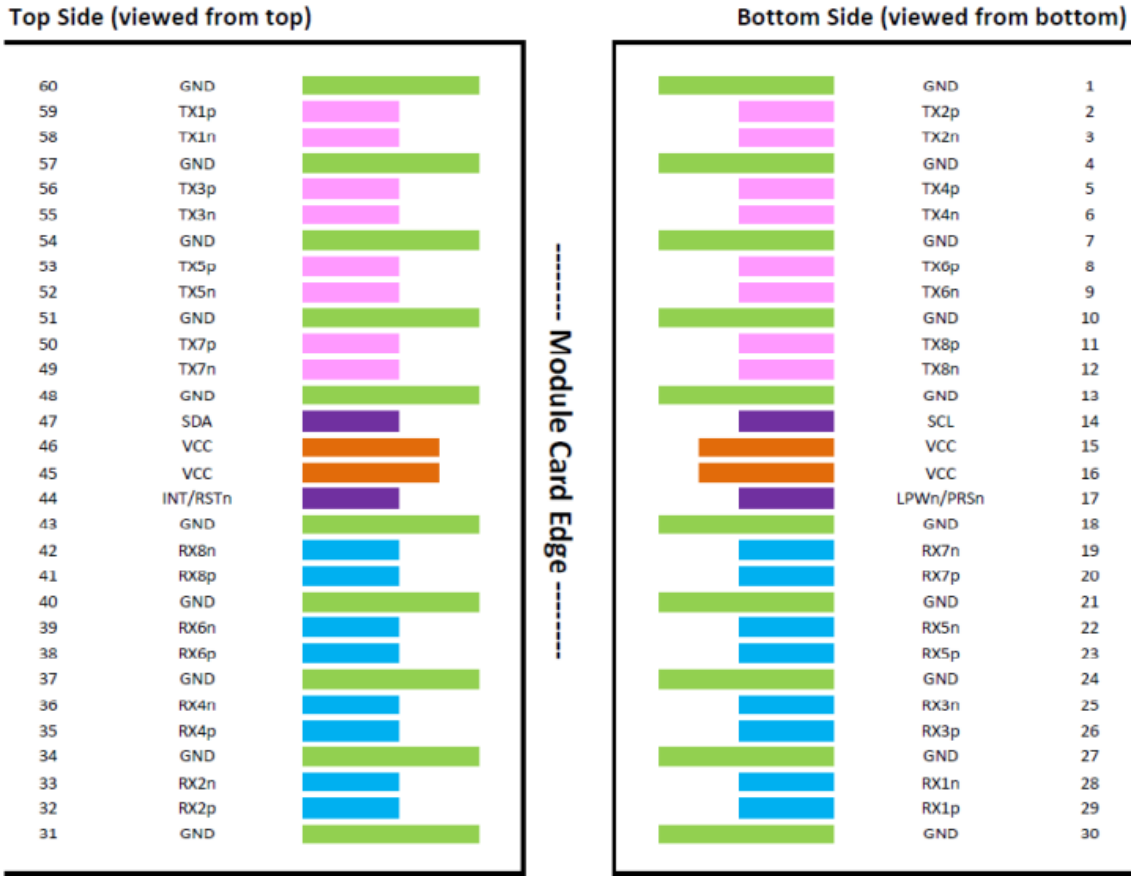
| Pin | Logic | Symbol | Name/Description | Direction | Plug Sequence | Notes |
|---|---|---|---|---|---|---|
| **1** | | GND | Module Ground. | | 1 | |
| **2** | CML-I | Tx2p | CH2 Transmitter Non-Inverted Data. | Input from Host | 3 | |
| **3** | CML-I | Tx2n | Ch2 Transmitter Inverted Data. | Input from Host | 3 | |
| **4** | | GND | Module Ground. | | 1 | |
| **5** | CML-I | Tx4p | CH4 Transmitter Non-Inverted Data. | Input from Host | 3 | |
| **6** | CML-I | Tx4n | CH4 Transmitter Inverted Data. | Input from Host | 3 | |
| **7** | | GND | Module Ground. | | 1 | |
| **8** | CML-I | Tx6p | Not Connected. | Input from Host | 3 | |
| **9** | CML-I | Tx6n | Not Connected. | Input from Host | 3 | |
| **10** | | GND | Module Ground. | | 1 | |
| **11** | CML-I | Tx8p | Not Connected. | Input from Host | 3 | |
| **12** | CML-I | Tx8n | Not Connected. | Input from Host | 3 | |
| **13** | | GND | Module Ground. | | 1 | |
| **14** | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock. | Bi-Directional | 3 | 1 |
| **15** | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| **16** | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| **17** | Multi-Level | LPWn/PRSn | Low-Power Mode/Module Present. | Bi-Directional | 3 | 2 |
| **18** | | GND | Module Ground. | | 1 | |
| **19** | CML-O | Rx7n | Not Connected. | Output from Host | 3 | |
| **20** | CML-O | Rx7p | Not Connected. | Output from Host | 3 | |
| **21** | | GND | Module Ground. | | 1 | |
| **22** | CML-O | Rx5n | Not Connected. | Output from Host | 3 | |
| **23** | CML-O | Rx5p | Not Connected. | Output from Host | 3 | |
| **24** | | GND | Module Ground. | | 1 | |
| **25** | CML-O | Rx3n | CH3 Receiver Inverted Data. | Output from Host | 3 | |
| **26** | CML-O | Rx3p | CH3 Receiver Non-Inverted Data. | Output from Host | 3 | |
| **27** | | GND | Module Ground. | | 1 | |
| **28** | CML-O | Rx1n | CH1 Receiver Inverted Data. | Output from Host | 3 | |
| **29** | CML-O | Rx1p | CH1 Receiver Non-Inverted Data. | Output from Host | 3 | |
| **30** | | GND | Module Ground. | | 1 | |
| **31** | | GND | Module Ground. | | 1 | |
| **32** | CML-O | Rx2p | CH2 Receiver Non-Inverted Data. | Output from Host | 3 | |
| **33** | CML-O | Rx2n | CH2 Receiver Inverted Data. | Output from Host | 3 | |
| **34** | | GND | Module Ground. | | 1 | |
| **35** | CML-O | Rx4p | CH4 Receiver Non-Inverted Data. | Output from Host | 3 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| **36** | CML-O | Rx4n | CH4 Receiver Inverted Data. | Output from Host | 3 | |
| **37** | | GND | Module Ground. | | 1 | |
| **38** | CML-O | Rx6p | Not Connected. | Output from Host | 3 | |
| **39** | CML-O | Rx6n | Not Connected. | Output from Host | 3 | |
| **40** | | GND | Module Ground. | | 1 | |
| **41** | CML-O | Rx8p | Not Connected. | Output from Host | 3 | |
| **42** | CML-O | Rx8n | Not Connected. | Output from Host | 3 | |
| **43** | | GND | Module Ground. | | 1 | |
| **44** | Multi-Level | INT/RSTn | Module Input/Module Reset. | Bi-Directional | 3 | 3 |
| **45** | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| **46** | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| **47** | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data. | Bi-Directional | 3 | 1 |
| **48** | | GND | Module Ground. | | 1 | |
| **49** | CML-I | Tx7n | Not Connected. | Input from Host | 3 | |
| **50** | CML-I | Tx7p | Not Connected. | Input from Host | 3 | |
| **51** | | GND | Module Ground. | | 1 | |
| **52** | CML-I | Tx5n | Not Connected. | Input from Host | 3 | |
| **53** | CML-I | Tx5p | Not Connected. | Input from Host | 3 | |
| **54** | | GND | Module Ground. | | 1 | |
| **55** | CML-I | Tx3n | CH3 Transmitter Inverted Data. | Input from Host | 3 | |
| **56** | CML-I | Tx3p | CH3 Transmitter Non-Inverted Data. | Input from Host | 3 | |
| **57** | | GND | Module Ground. | | 1 | |
| **58** | CML-I | Tx1n | Ch1 Transmitter Inverted Data. | Input from Host | 3 | |
| **59** | CML-I | Tx1p | CH1 Transmitter Non-Inverted Data. | Input from Host | 3 | |
| **60** | | GND | Module Ground. | | 1 | |

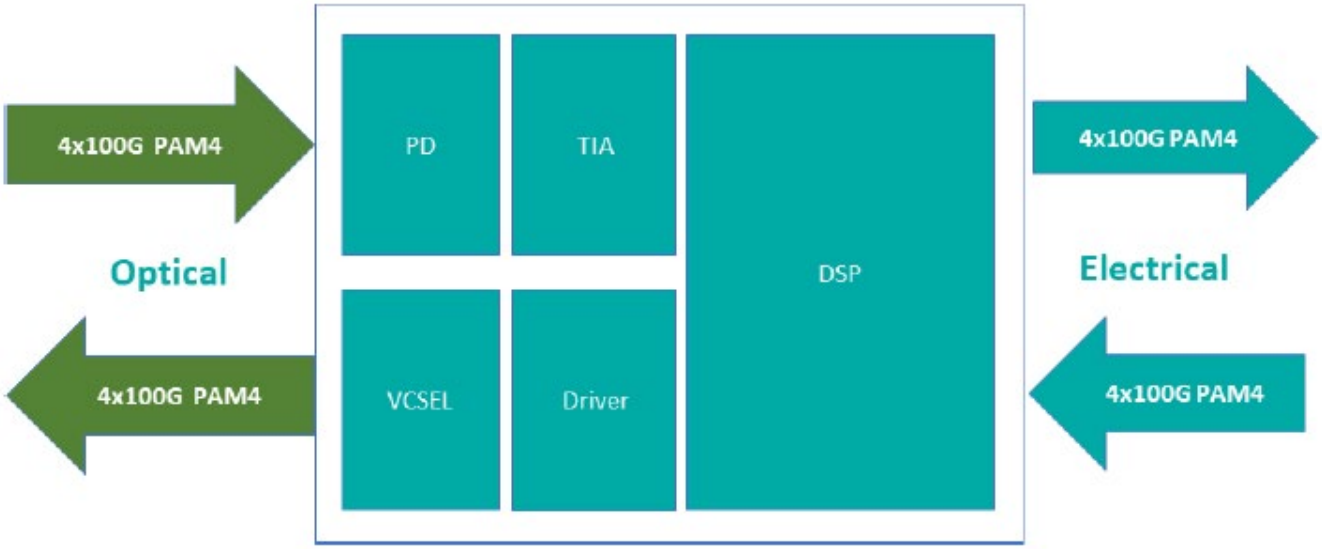
**Notes:**

1. Open-drain with pull-up resistor on the host.
2. LPWn/PRSn is a dual function signal that allows the host to signal low-power mode and allows the module to indicate that the module is present.
3. INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module.

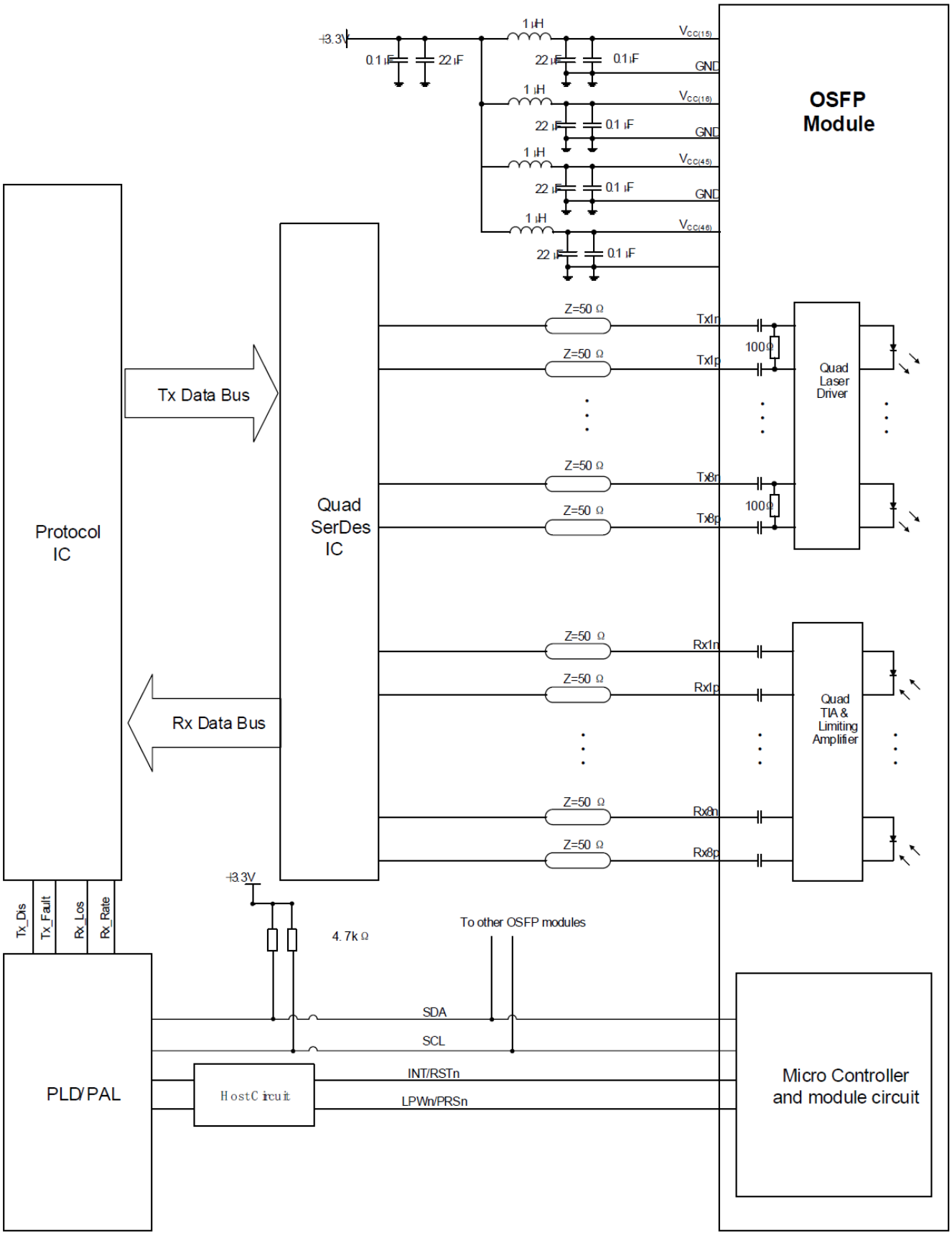
**Pin Assignment**



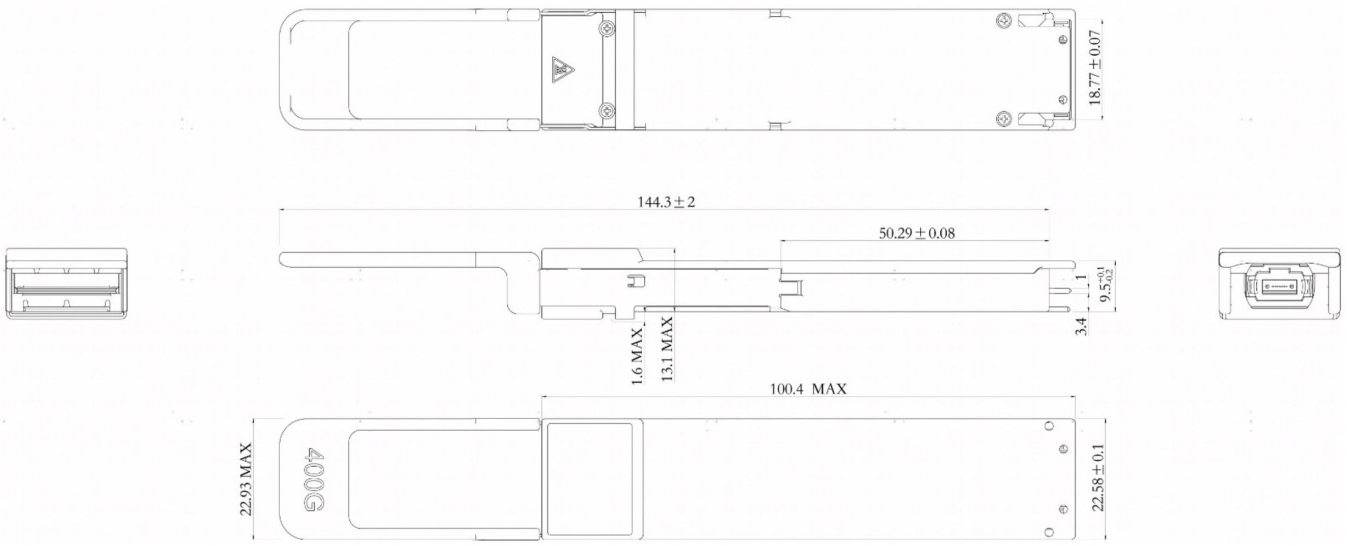

**Transceiver Block Diagram**



**Electrical Interface**



**Mechanical Specifications**




**Notes:**

1. Tolerance: ± 0.1mm.
2. Others according with OSFP MSA or customer specifications.
3. Optical port according to fiber connector specifications.

**About AddOn Networks**

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.




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