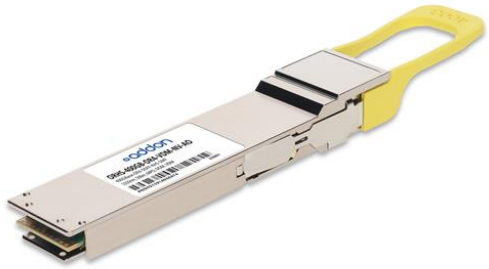
ORHS-400GB-DR4-VDM-NV-AO

NVIDIA® Compatible TAA 400GBase-DR4 PAM4 OSFP-RHS Transceiver (SMF, 1310nm, 500m, MPO, DOM, CMIS 5.0, VDM)

Features:

- Compliant with OSFP MSA 5.0
- Compliant with GR-468-CORE
- Compliant with IEEE 802.3ck and IEEE 802.3bs
- 4x106.25Gbps PAM4 Electrical Interface
- Maximum Power Consumption: 9W
- Compliant with CMIS 5.0
- Up to 500m Transmission on Single-Mode Fiber
- 1xMPO-12 APC Connector
- Operating Temperature: 0 to 70 Celsius
- Single 3.3V Power Supply
- RoHS Compliant and Lead-Free



Applications:

- 400GBase InfiniBand
- 400GBase Ethernet
- Data Center Applications
- Advance Monitoring Capable Transceiver

Product Description

This NVIDIA® compatible OSFP-RHS transceiver provides 400GBase-DR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with NVIDIA®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Relative Humidity	RH	5		85	%	1
Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Receiver Damage Threshold Per Lane		5			dBm	

Notes:

1. Non-condensing.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Case Temperature	Tc	0		70	°C	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			4466	mA	1
Module Power Dissipation	PD			9	W	1

Notes:

1. Tc = 70°C.

Optical, Electrical Operating Characteristics (1311nm DFB and PIN, 500m)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Optical Data Rate Per Lane		53.125 ± 100ppm			GBd	
Modulation Format		PAM4				
Line Wavelength	λ	1304.5	1311	1317.5	nm	
Average Launch Power Per Lane	P_{AVG}	-2.9		4	dBm	
Optical Modulation Amplitude (OMA) Per Lane	OMA	-0.8		4.2	dBm	
Extinction Ratio	ER	3.5			dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Launch Power in OMA Minus TDECQ Per Lane		-2.2			dBm	
Transmitter and Dispersion Eye Closure for PAM4 Per Lane	TDECQ			3.4	dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of Off Transmitter Per Lane				-15	dBm	

Electrical Data Rate Per Lane		53.125 ± 100ppm			GBd	
Differential Pk-Pk Input Voltage Tolerance	Vpp	800			mV	
DC Common-Mode Voltage	Vcm	-350		2850	mV	2
Differential Termination Resistance Mismatch	Rdm			10	%	
Effective Return Loss				8.5	dB	
Differential to Common Mode Input Return Loss		IEEE 802.3ck Equation (120G-2)			dB	
Module Stressed Input Test		IEEE 802.3ck 120G.3.4.2				3
Receiver						
Optical Data Rate Per Lane		53.125 ± 100ppm			GBd	
Modulation Format		PAM4				
Line Wavelength	λ	1304.5	1311	1317.5	nm	
Average Receiver Power Per Lane		-5.9		4	dBm	
Receiver Power Per Lane (OMA)				4.2	dBm	
Receiver Sensitivity (OMAouter) Per Lane				Max. (-3.9, SECQ-5.3)	dBm	4
Stressed Receiver Sensitivity (OMAouter) Per Lane (Maximum)				-1.9	dBm	
Receiver Reflectance				-26	dB	
Electrical Data Rate Per Lane		53.125 ± 100ppm			GBd	
Differential Termination Resistance Mismatch		-10		10	%	
Differential Output Voltage Pk-Pk	Vpp			845	mV	
DC Common-Mode Voltage	Vcm	-350		2850	mV	2
Effective Return Loss	ERL	8.5			dB	
Transition Time		8.5			ps	
Common-Mode to Differential Return Loss		IEEE 802.3ck Equation (120G-1)			dB	

Notes:

1. Tested under recommended operating conditions, unless otherwise noted.
2. DC common-mode voltage is generated by the host. Specification includes the effects of ground offset voltage.
3. BER specified in IEEE 802.3ck 120G.1.1.
4. Receiver sensitivity (OMAouter), per lane (maximum), is informative and is defined for a transmitter with SECQ of 0.9dB. Receiver sensitivity (OMAouter), per lane: for TDECQ<1.4dB, max.=-3.9dBm. For 1.4dB≤TDECQ≤3.4dB, max.=SECQ-5.3dBm.

Digital Diagnostic Functions

Parameter	Symbol	Min.	Max.	Unit	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	1
Supply Voltage Monitor Absolute Error	DMI_Vcc	-3%	3%	V	2
Bias Current Monitor Absolute Error	DMI_Ibias	-10%	10%	mA	
Laser Power Monitor Absolute Error	DMI_Tx	-3	3	dB	
Rx Power Monitor Absolute Error	DMI_Rx	-3	3	dB	

Notes:

1. Temperature here is depending on module case around maximum power dissipation. Temperature monitor is done over operating temperature.
2. Supply voltage monitor is done over operating voltage.

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInitDuration	Max. MgmtInitDuration		2000	ms	1
ResetL Assert Time	t_reset_init	10		µs	2
IntL Assert Time	ton_IntL		200	ms	3
IntL De-Assert Time	toff_IntL		500	µs	4
Rx LOS Assert Time	ton_los		100	ms	5
Flag Assert Time	ton_flag		200	ms	6
Mask Assert Time	ton_mask		100	ms	7
Mask De-Assert Time	toff_mask		100	ms	8

Notes:

1. Time from power on, hot plug, or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
4. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes de-assert times for Rx LOS, Tx Fault, and other flag bits.
5. Time from Rx LOS state to Rx LOS bit is set (value=1b) and IntL is asserted.
6. Time from occurrence of condition triggering flag to associated flag bit is set (value=1b) and IntL is asserted.
7. Time from mask bit is set (value=1b) until the associated IntL assertion is inhibited.
8. Time from mask bit is cleared (value=0b) until the associated IntL operation resumes.

Surge Current Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Power Supply Voltage Including Ripple, Droop, and Noise Below 100kHz	Vcc_Module	3.135	3.3	3.465	V	
Host Power Supply Voltage Including Ripple, Droop, and Noise Below 100kHz	Vcc_Host	3.135	3.3	3.465	V	
Module Power Supply Noise Tolerance 10Hz to 10MHz (Pk-Pk) Voltage Drop Across Mated Connector (Vcc_Host Minus Vcc_Module)	Vcc_drop			66	mV	
Total Current for Vcc Pins	Icc_module			10	A	1
Host RMS Noise Output 10Hz to 10MHz	e N_Host			25	mV	
Module RMS Noise Output 10Hz to 10MHz	e N_Mod			15	mV	
Module In-Rush - Instantaneous Peak Duration	T_ip			50	µs	
Module In-Rush - Initialization Time	T_init			500	ms	
In-Rush and Discharge Current	I_didt			100	mA/µs	2
High-Power Mode to Low-Power Mode Transition Time From Assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs	
Power Class 5 Module (High-Power Mode)						
Power Consumption	P_5		10		W	
Instantaneous Peak Current at High Power Enable	Icc_ip_5		4000		mA	
Sustained Peak Current at High Power Enable	Icc_sp_5		3333		mA	
Steady State Current	Icc_5		3190		mA	3

Notes:

1. Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure that the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.
2. The specified In-Rush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power-to-high-power, and high-power-to-low-power.
3. Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

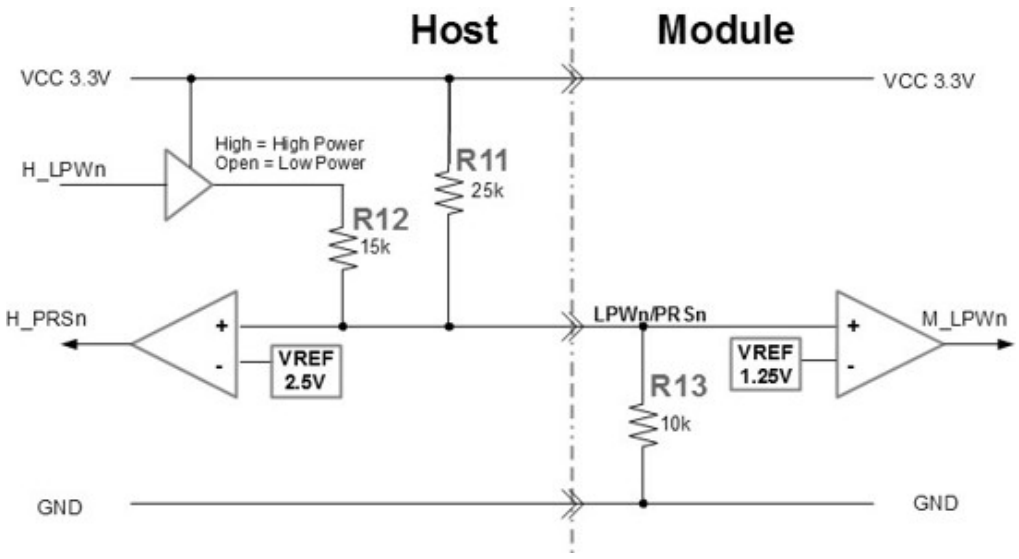
Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Ground.	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted.	3	
3	CML-I	Tx2n	Transmitter Data Inverted.	3	
4		GND	Ground.	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted.	3	
6	CML-I	Tx4n	Transmitter Data Inverted.	3	
7		GND	Ground.	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted.	3	
9	CML-I	Tx6n	Transmitter Data Inverted.	3	
10		GND	Ground.	1	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted.	3	
12	CML-I	Tx8n	Transmitter Data Inverted.	3	
13		GND	Ground.	1	1
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	2
15		VCC	+3.3V Power.	2	
16		VCC	+3.3V Power.	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	3	3
18		GND	Ground.	1	1
19	CML-O	Rx7n	Receiver Data Inverted.	3	
20	CML-O	Rx7p	Receiver Data Non-Inverted.	3	
21		GND	Ground.	1	1
22	CML-O	Rx5n	Receiver Data Inverted.	3	
23	CML-O	Rx5p	Receiver Data Non-Inverted.	3	
24		GND	Ground.	1	1
25	CML-O	Rx3n	Receiver Data Inverted.	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted.	3	
27		GND	Ground.	1	1
28	CML-O	Rx1n	Receiver Data Inverted.	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted.	3	
30		GND	Ground.	1	1
31		GND	Ground.	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted.	3	
33	CML-O	Rx2n	Receiver Data Inverted.	3	
34		GND	Ground.	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted.	3	

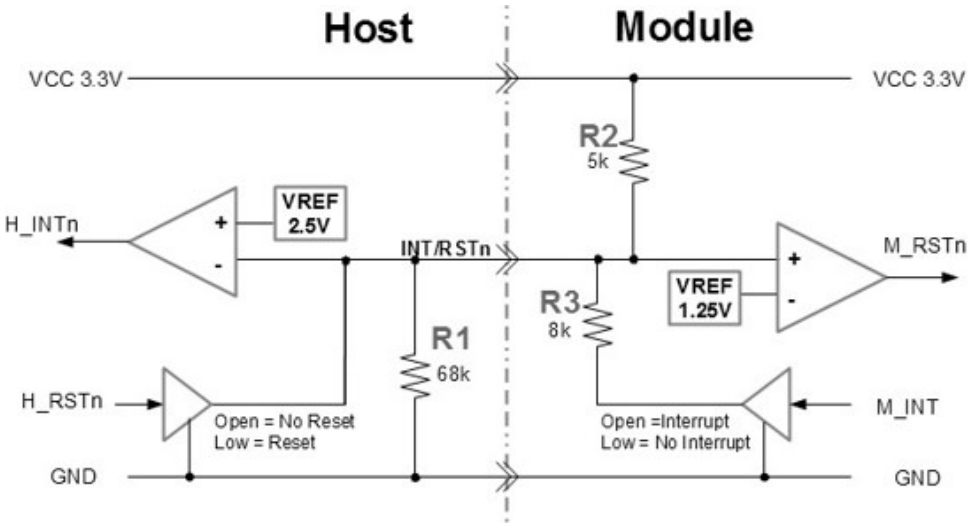
36	CML-O	Rx4n	Receiver Data Inverted.	3	
37		GND	Ground.	1	1
38	CML-O	Rx6p	Receiver Data Non-Inverted.	3	
39	CML-O	Rx6n	Receiver Data Inverted.	3	
40		GND	Ground.	1	1
41	CML-O	Rx8p	Receiver Data Non-Inverted.	3	
42	CML-O	Rx8n	Receiver Data Inverted.	3	
43		GND	Ground.	1	1
44	Multi-Level	INT/RSTn	Module Interrupt/Module Reset.	3	4
45		VCC	+3.3V Power.	2	
46		VCC	+3.3V Power.	2	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	2
48		GND	Ground.	1	1
49	CML-I	Tx7n	Transmitter Data Inverted.	3	
50	CML-I	Tx7p	Transmitter Data Non-Inverted.	3	
51		GND	Ground.	1	1
52	CML-I	Tx5n	Transmitter Data Inverted.	3	
53	CML-I	Tx5p	Transmitter Data Non-Inverted.	3	
54		GND	Ground.	1	1
55	CML-I	Tx3n	Transmitter Data Inverted.	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted.	3	
57		GND	Ground.	1	1
58	CML-I	Tx1n	Transmitter Data Inverted.	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted.	3	
60		GND	Ground.	1	1

Notes:

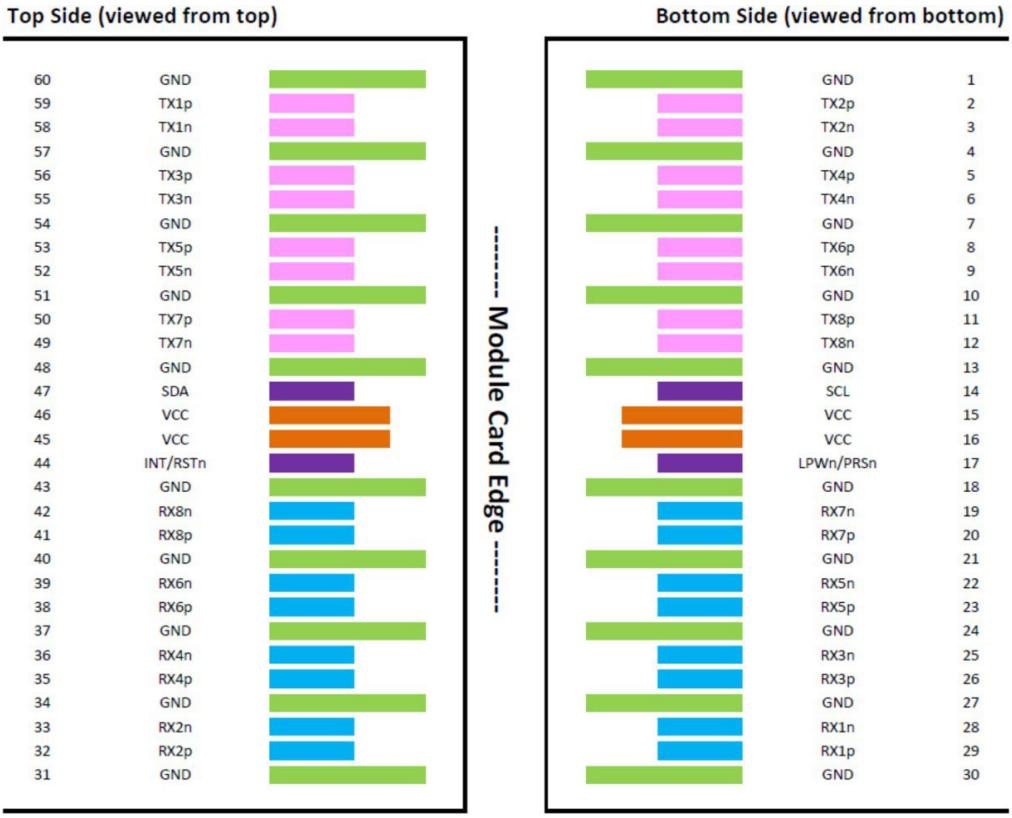
1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. SCL and SDA are 2-wire serial interfaces between the host and the module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1kΩ to 4.7kΩ depending on the capacitive load.
3. LPWn/PRSn is a dual-function signal that allows the host to signal low-power mode and allows the module to indicate “Module Present.” The circuit shown below enables multi-level signaling to provide direct signal control in both directions. Low-power mode is an active-low signal on the host that gets converted to an active-low signal on the module. “Module Present” is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.



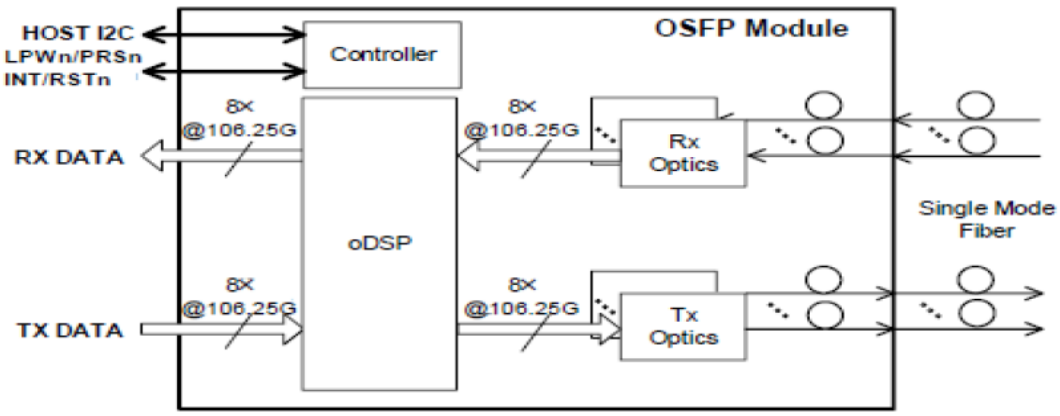
4. INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown below enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.



Pin-Out Definitions



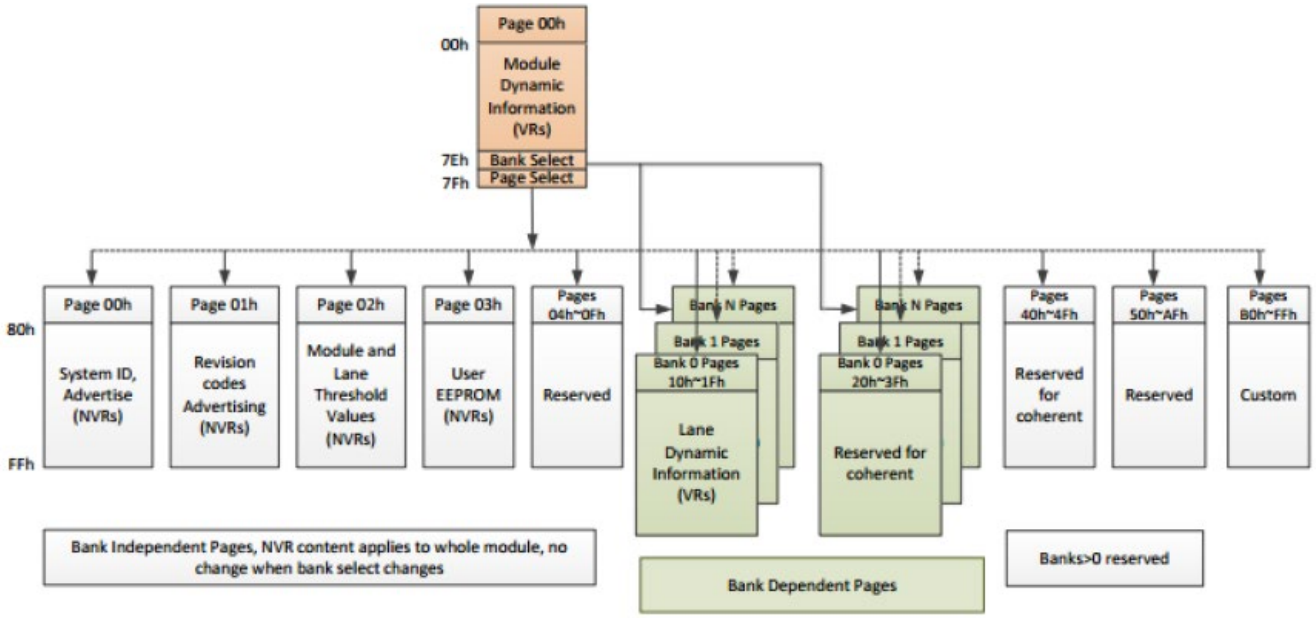
Block Diagram of Transceiver

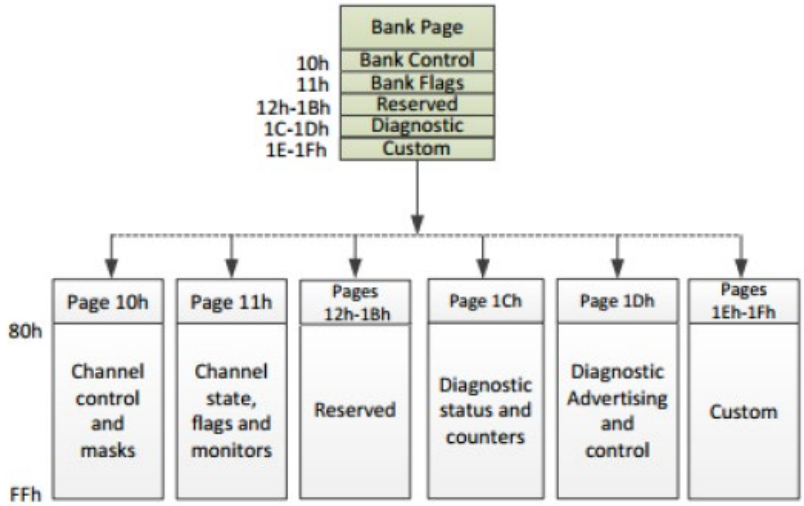


Notes:

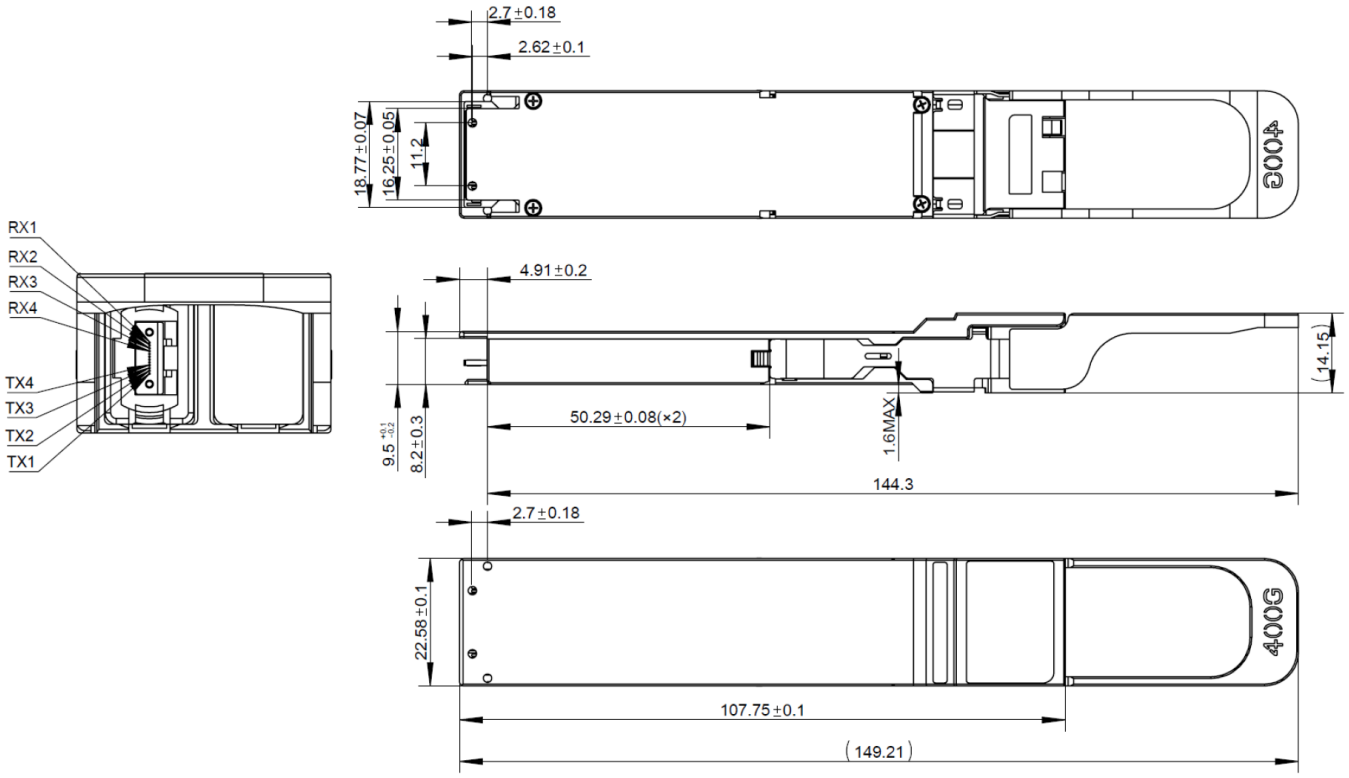
1. Transmitter Section: The transceiver converts 8-channel 106.25Gbps electrical data to 8-channel 1311nm 106.25Gbps optical signals for 850Gbps optical transmission.
2. Receiver Section: Similarly, it optically converts 8-channel 1311nm 106.25Gbps optical signals to 8-channel electrical data output on the receiver side.

Digital Diagnostic Memory Map





Mechanical Specifications



Unit: mm

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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