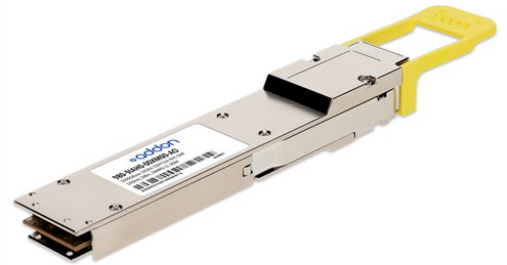


980-9IAH0-00XM00-AO

NVIDIA® 980-9IAH0-00XM00 Compatible 1.6T 2xDR4 PAM4 OSFP224-RHS Transceiver (SMF, 1310nm, 500m, 2xMPO-12, DOM, CMIS 5.3)

Features:

- OSFP MSA Compliant
- Compliant with IEEE P802.3dj
- CMIS 5.3 Compliant
- 8x212Gbps PAM4 Electrical Interface
- Up to 500m Transmission on Single-Mode Fiber
- OIF CEI-224G-VSR-PAM4 Compliant
- 3.3V Power Supply
- Power Consumption: 28W Max
- Operating Temperature: 0 to 70 Celsius
- Hot-Pluggable
- RoHS Compliant and Lead-Free



Applications:

- 2x800GBase Ethernet
- 16x100GBase Ethernet
- InfiniBand

Product Description

This NVIDIA® 980-9IAH0-00XM00 compatible OSFP224-RHS transceiver provides 1600GBase-2xDR4 throughput up to 500m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO-12 connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		+85	°C	
Maximum Supply Voltage	Vcc	-0.3		3.6	V	
Operating Relative Humidity	RH	0		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	Tc	0		+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	+3.465	V	
Power Consumption	PC			28	W	
Supply Current				7.576	A	
Data Rate Accuracy		-50		50	ppm	
Link Distance (SMF)				500	m	

Electrical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Host-to-Module (Module Input)							
Single-Ended Voltage Tolerance			-0.4		1.4	V	
DC Common-Mode Voltage Tolerance			0.15		1.05	V	
Pk-Pk AC Common-Mode Voltage Tolerance	Low-Frequency (VCMLF)				32	mV	
	Full-Band (VCMFB)				80		
Differential-Mode to Common-Mode Return Loss		RLcd	Equation 179-20			dB	1
Effective Return Loss		ERL	8.5			dB	
Interference Tolerance					Table 176D-9		1
Jitter Tolerance					Table 176D-10		1
Module-to-Host at TP4 (Module Output)							
Differential Pk-Pk Voltage	Output Disabled				30	mV	
	Output Enabled				1000	mV	
DC Common-Mode Voltage Tolerance			0.15		1.05	V	
AC Common-Mode Pk-Pk Voltage	Low-Frequency (VCMLF)	Vcm			15	mV	
	Full-Band (VCMFB)				60		
Effective Return Loss		ERL	8.5			dB	
Common-Mode to Common-Mode Return Loss		RLcc	Equation 179-12			dB	1
Common-Mode to Differential-Mode Return Loss		RLdc	Equation 179-13			dB	1
Transmitter Steady-State Voltage		Vf	0.4		0.5	V	
Linear Fit Pulse Peak Ratio		Rpeak	0.456				
Level Separation Mismatch RLM			0.95				
Transmitter Output Waveform	Absolute Value of Step Size for All Taps		0.005				
	Absolute Value of Step Size for All Taps				0.025		
	Value at Minimum State for c(-3)				-0.06		
	Value at Maximum State for c(-2)		0.12				
	Value at Minimum State for c(-1)				-0.34		
	Value at Minimum State for c(0)				0.5		
	Value at Minimum State for c(1)				-0.2		
Signal-to-Noise-and-Distortion Ratio		SNDR	Table 179-9			dB	1
Signal-to-Residual-Intersymbol-Interference Ratio		SNRISI	28			dB	
Output Jitter	JRMS				0.023	UI	
	EOJ03				0.025	UI	
	J4u03				0.117	UI	

Notes:

1. See IEEE P802.3dj.

Optical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter							
Signaling Rate Per Lane				106.25±50ppm		GBd	
Modulation Format				PAM4			
Lane Wavelength			1304.5		1317.5	nm	
Side-Mode Suppression Ratio Per Lane		SMSR	30			dB	
Average Launch Power Per Lane			-3.1		4	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}) Per Lane	For Max. (TECQ,TDECQ) <0.9dB		-0.1		4.2	dBm	
	For 0.9dB< Max. (TECQ,TDECQ) <3.4dB		-1+ max (TECQ,TDECQ)				
Transmitter and Dispersion Eye Closure for PAM4 Per Lane		TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 Per Lane		TECQ			3.4	dB	
TDECQ - TECQ Per Lane					2.5	dB	
Transmitter Functional Symbol Error Histogram Per Lane					Table 180-17		3
Transmitter Overshoot and Undershoot Per Lane					22	%	
Transmitter Power Excursion Per Lane					2.3	dBm	
Extinction Ratio Per Lane		ER	3.5			dB	
Transmitter Transition Time Per Lane					8	ps	
Average Launch Power of OFF Transmitter Per Lane					-15	dBm	
RIN _{21.4} OMA Per Lane					-139	dB/Hz	
Optical Return Loss Tolerance Per Lane					21.4	dB	
Transmitter Reflectance Per Lane					-26	dB	
Receiver							
Signaling Rate Per Lane				106.25±50ppm		GBd	
Modulation Format				PAM4			
Lane Wavelength			1304.5		1317.5	nm	
Damage Threshold			5			dBm	
Average Receiver Power Per Lane			-6.1		4	dBm	
Receiver Power(OMA _{outer}) Per Lane					4.2	dBm	
Receiver Sensitivity (OMA _{outer}) Per Lane	For TECQ <0.9dB				-3.4	dBm	1
	For 0.9dB <TECQ <SECQ				-4.3+TECQ		
Stressed Receiver Sensitivity (OMA _{outer}) Per Lane					-0.9	dBm	2
Conditions of Stress Receiver Sensitivity Test							
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test				3.4			

OMAouter of Each Aggressor Lane			4.2			
---------------------------------	--	--	-----	--	--	--

Notes:

1. Measured with conformance test signal (from Rx overload point to Rx sensitivity point) for Pre-FEC Bit Error Ratio < 1E-6, Post-FEC Bit Error Ratio = 0 and FEC symbol error distribution below 7.
2. Measured with conformance test signal for Pre-FEC Bit Error Ratio < 2.4E-4.
3. See IEEE P802.3dj.

Digital Diagnostic Monitoring Interface

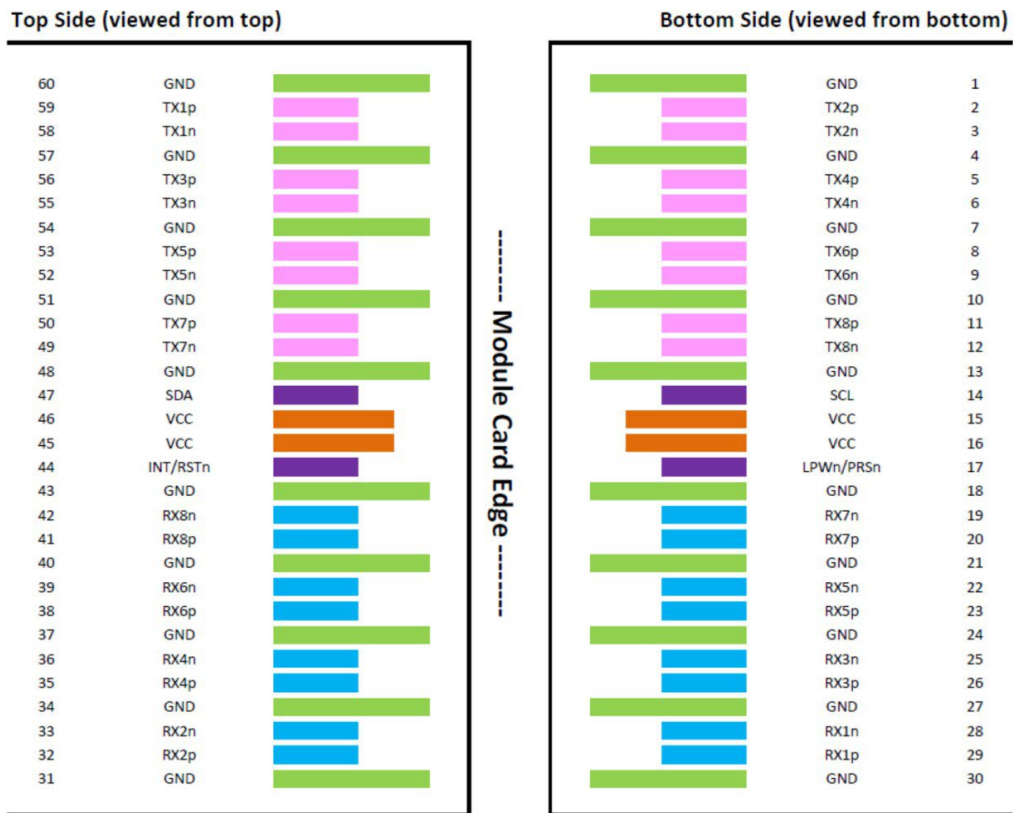
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3		3	°C	
Supply Voltage Monitor Absolute Error	DMI_VCC	-3		3	%	
Bias Current Monitor Absolute Error	DMI_I Bias	-10		10	%	
Tx Power Monitor Absolute Error	DMI_TX	-3		3	dB	
Rx Power Monitor Absolute Error	DMI_RX	-3		3	dB	

Pin Descriptions

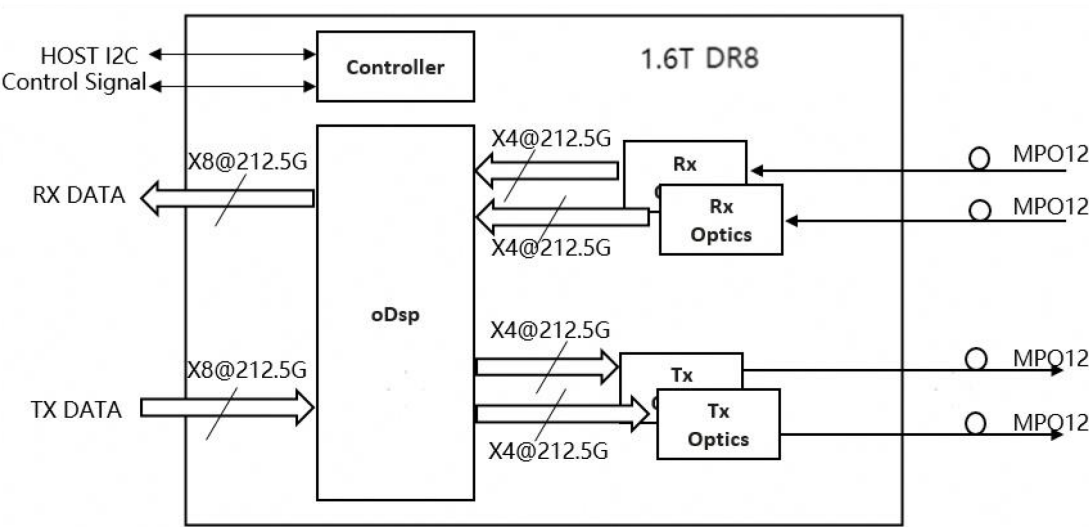
Pin	Symbol	Name/Description	Logic	Plug Sequence
1	GND	Module Ground.		1
2	Tx2p	Transmitter Non-Inverted Data.	CML-I	3
3	Tx2n	Transmitter Inverted Data.	CML-I	3
4	GND	Module Ground.		1
5	Tx4p	Transmitter Non-Inverted Data.	CML-I	3
6	Tx4n	Transmitter Inverted Data.	CML-I	3
7	GND	Module Ground.		1
8	Tx6p	Transmitter Non-Inverted Data.	CML-I	3
9	Tx6n	Transmitter Inverted Data.	CML-I	3
10	GND	Module Ground.		1
11	Tx8p	Transmitter Non-Inverted Data.	CML-I	3
12	Tx8n	Transmitter Inverted Data.	CML-I	3
13	GND	Module Ground.		1
14	SCL	2-Wire Serial Interface Clock.	LVCMOS-I/O	3
15	Vcc	+3.3V Power Supply.		2
16	Vcc	+3.3V Power Supply.		2
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3
18	GND	Module Ground.		1
19	Rx7n	Receiver Inverted Data.	CML-O	3
20	Rx7p	Receiver Non-Inverted Data.	CML-O	3
21	GND	Module Ground.		1
22	Rx5n	Receiver Inverted Data.	CML-O	3
23	Rx5p	Receiver Non-Inverted Data.	CML-O	3
24	GND	Module Ground.		1
25	Rx3n	Receiver Inverted Data.	CML-O	3
26	Rx3p	Receiver Non-Inverted Data.	CML-O	3
27	GND	Module Ground.		1
28	Rx1n	Receiver Inverted Data.	CML-O	3
29	Rx1p	Receiver Non-Inverted Data.	CML-O	3
30	GND	Module Ground.		1
31	GND	Module Ground.		1
32	Rx2p	Receiver Non-Inverted Data.	CML-O	3
33	Rx2n	Receiver Inverted Data.	CML-O	3
34	GND	Module Ground.		1
35	Rx4p	Receiver Non-Inverted Data.	CML-O	3
36	Rx4n	Receiver Inverted Data.	CML-O	3

37	GND	Module Ground.		1
38	Rx6p	Receiver Non-Inverted Data.	CML-O	3
39	Rx6n	Receiver Inverted Data.	CML-O	3
40	GND	Module Ground.		1
41	Rx8p	Receiver Non-Inverted Data.	CML-O	3
42	Rx8n	Receiver Inverted Data.	CML-O	3
43	GND	Module Ground.		1
44	INT/RSTn	Module Input/Module Reset.	Multi-Level	3
45	Vcc	+3.3V Power Supply.		2
46	Vcc	+3.3V Power Supply.		2
47	SDA	2-Wire Serial Interface Data.	LVCMOS-I/O	3
48	GND	Module Ground.		1
49	Tx7n	Transmitter Inverted Data.	CML-I	3
50	Tx7p	Transmitter Non-Inverted Data.	CML-I	3
51	GND	Module Ground.		1
52	Tx5n	Transmitter Inverted Data.	CML-I	3
53	Tx5p	Transmitter Non-Inverted Data.	CML-I	3
54	GND	Module Ground.		1
55	Tx3n	Transmitter Inverted Data.	CML-I	3
56	Tx3p	Transmitter Non-Inverted Data.	CML-I	3
57	GND	Module Ground.		1
58	Tx1n	Transmitter Inverted Data.	CML-I	3
59	Tx1p	Transmitter Non-Inverted Data.	CML-I	3
60	GND	Module Ground.		1

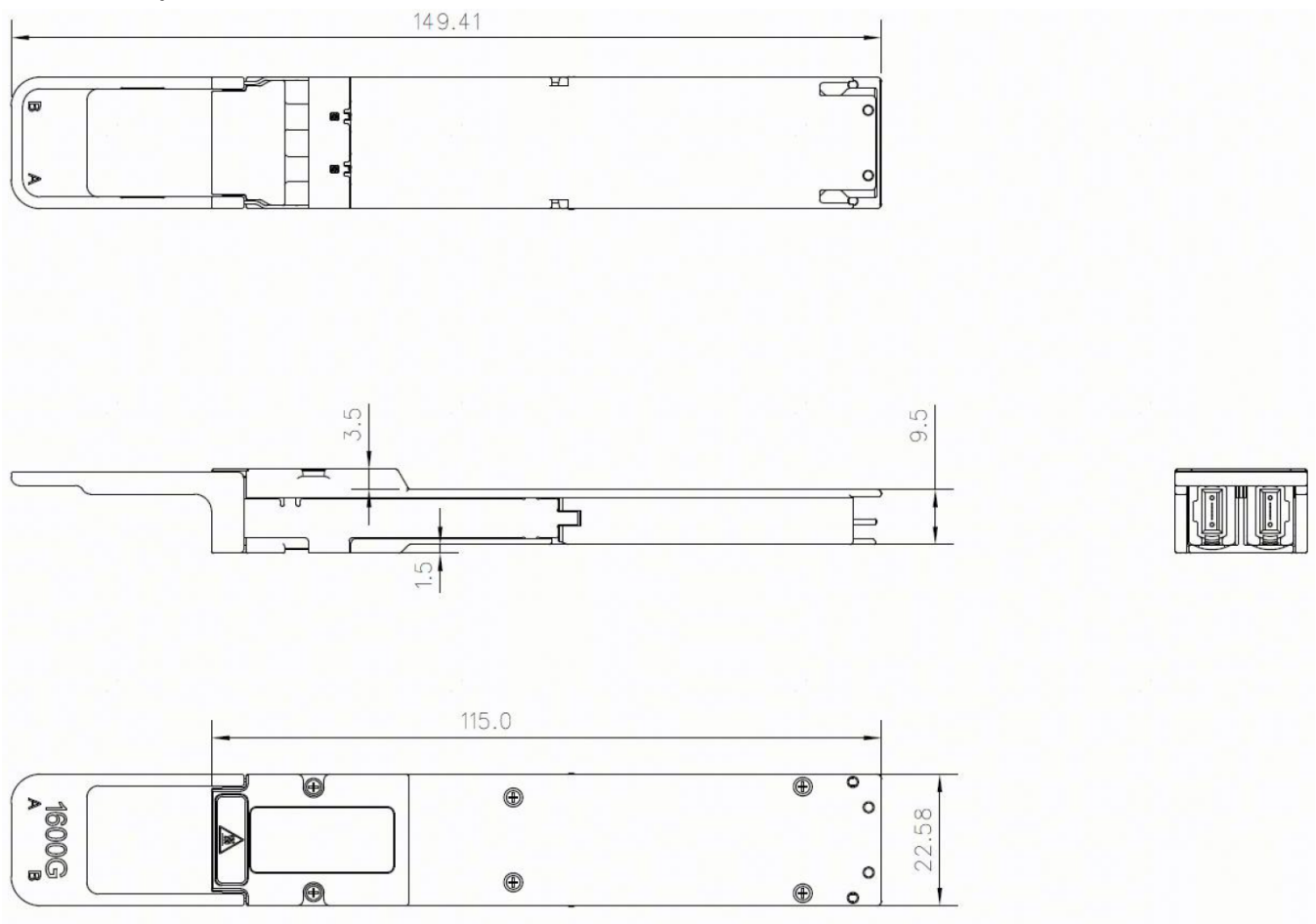
Host Board Connector



Block Diagram



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



U.S. Headquarters

Email: sales@addonnetworks.com

Telephone: +1 877.292.1701

Fax: 949.266.9273

Europe Headquarters

Email: salesemea@addonnetworks.com

Telephone: +44 1285 842070