QSFP-100G-CLR4-OPC

Alcatel-Lucent Nokia® Compatible TAA 100GBase-CLR4 QSFP28 Transceiver (SMF, 1310nm, 2km, LC, DOM)

Features

- Compliant with QSFP28 MSA
- Supports 100Gbps
- Single 3.3V Power Supply
- Power Dissipation is
- 4*25Gbps DFB-based CWDM transmitter
- PIN and TIA array on the receiver side
- 4x25G Electrical Interface
- Duplex LC Connector
- Single-mode Fiber
- Commercial Temperature 0 to 70 Celsius
- RoHS Compliant and Lead Free

Applications:

- 100GBase Ethernet

Product Description

This Alcatel-Lucent Nokia® compatible QSFP28 transceiver provides 100GBase-CLR4 throughput up to 2km over single-mode fiber (SMF) using a wavelength of 1310nm via an LC connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Alcatel-Lucent Nokia®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage		Vcc	-0.5	3.3	3.6	V	
Power Supply Voltage		Vcc	3.135	3.3	3.465	V	
Power Supply Noise					66	mVp-p	1
Power Dissipation		P_{DISS}			3.5	W	
Storage Temperature		Tstg	-40		85	oC	
Operating Case Temperature		Tc	0	25	70	oC	2
Relative Humidity		RH	5		85	%	
Data Input Voltage	**Single-Ended**		-0.5		Vcc+0.5	V	
	Differential				0.8	V	3
Receiver Damage Threshold Per Lane		Rxdmg	3.3			dBm	

Notes:

1. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See below for the recommended power supply filter.
2. The position of the case temperature measurement is shown below. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order to not degrade reliability.
3. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600mV peak-to-peak differential.
4. Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment. Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.
5. Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.
6. Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to a dirty connector. If contamination occurs, use standard LC port cleaning methods.
7. Exceeding the Absolute Maximum Ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under Absolute Maximum Ratings will affect the reliability of the device.

Electrical Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Unit	Notes
Transceiver Power Consumption				3.5	W	
Transceiver Power Supply Total Current				1120	mA	
AC Coupling Capacitors (Internal)			0.1		µF	
Input Characteristics						
Signaling Rate Per Lane	TP1	25.78125 ± 100ppm			GBd	1
Differential pk-pk Input Voltage Tolerance	TP1a	900			mV	
Single-Ended Voltage Tolerance Range	TP1a	-0.4		3.3	V	
DC Common-Mode Output Voltage	TP1	-350		2850	mV	2
Differential Input Return Loss (Minimum)	TP1	Equation (83E-5)			dB	3
Differential- to Common-Mode Input Return Loss (Minimum)	TP1	Equation (83E-6)			dB	3
Differential Termination Mismatch	TP1			10	%	
Module Stressed Input Test	TP1a					4
Eye Width			0.46		UI	
Applied pk-pk Sinusoidal Jitter		Table 88-13				3
Eye Height			95		mV	
Output Characteristics						
Signaling Speed Per Lane	TP4	25.78125 ± 100ppm			GBd	1
AC Common-Mode Output Voltage (RMS)	TP4		17.5		mV	
DC Common-Mode Voltage	TP4	-350		2850	mV	5
Differential Output Voltage	TP4			900	mV	
Differential Output Return Loss (Minimum)	TP4	Equation (83E-2)			dB	
Common- to Differential-Mode Conversion Return Loss (Minimum)	TP4	Equation (83E-3)			dB	
Differential Termination Mismatch	TP4			10	%	
Transition Time (20-80%)	TP4	12			ps	
Eye Width	TP4	0.57			UI	
Eye Height Differential	TP4	228			mV	
Vertical Eye Closure	TP4			5.5	dB	

Notes:

1. CAUI-4 operation with host-generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
2. DC common-mode voltage is generated by the host. Specification includes the effects of ground offset voltage.
3. 802.3bm.
4. Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

5. DC common-mode voltage is generated by the host. Specification includes the effects of ground offset voltage.
6. Unless otherwise stated, the above characteristics are defined under recommended operating conditions.
7. For control signal timing, including ModSelL, ResetL, LPMode/TxDis, ModPrsL, IntL/RxLOSL, SCL, and SDA, see Control Interface Section.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Speed Per Lane	BRAVE		25.78125		Gbps	1
Data Rate Variation		-100		100	ppm	
Modulation Format			NRZ			
Lane 0 Center Wavelength	λC0	1264.5		1277.5	nm	
Lane 1 Center Wavelength	λC1	1284.5		1297.5	nm	
Lane 2 Center Wavelength	λC2	1304.5		1317.5	nm	
Lane 3 Center Wavelength	λC3	1324.5		1337.5	nm	
Total Average Output Power	Po			8.3	dBm	
Average Launch Power Per Lane	Peach	-6.5		2.3	dBm	2
Transmit OMA Per Lane	TxOMA	-4.0		2.5	dBm	3
Launch Power in OMA Minus TDP Per Lane	OMA-TDP	-5.0			dBm	
Average Launch Power of Off Transmitter Per Lane	Poff			-30	dBm	
Transmitter and Dispersion Penalty Per Lane	TDP			3	dB	4
Side-Mode Suppression Ratio	SMSR	30			dB	
Optical Return Loss Tolerance	ORLT			20	dB	
Transmitter Reflectance				-12	dB	5
Extinction Ratio	ER	3.5			dB	
RIN OMA	RIN			-130	dB/Hz	
Transmitter Eye Mask Definition: X1, X2, X3, Y1, Y2, Y3	(0.25, 0.4, 0.45, 0.25, 0.28, 0.4)					6
Receiver						
Signaling Speed Per Lane	BRAVE		25.78125		Gbps	1
Data Rate Variation		-100		100	ppm	
Receiver Differential Data Output Load		100			Ω	
Damage Threshold	Rxdmg	3.3			dBm	
Lane 0 Center Wavelength	λC0	1264.5		1277.5	nm	
Lane 1 Center Wavelength	λC1	1284.5		1297.5	nm	

Lane 2 Center Wavelength	λC2	1304.5		1317.5	nm	
Lane 3 Center Wavelength	λC3	1324.5		1337.5	nm	
Average Receive Power Per Lane	Rxpow	-10		2.3	dBm	7
Receive Power (OMA) Per Lane	RxOMA			2.5	dBm	
Unstressed Receive Sensitivity (OMA) With FEC Per Lane	Rxsens_FEC			-11	dBm	8
Unstressed Receiver Sensitivity (OMA) Without FEC Per Lane	Rxsens			-8.5	dBm	8
Stressed Receiver Sensitivity (OMA) With FEC Per Lane	RxSRS_FEC			-8.5	dBm	9
Stressed Receiver Sensitivity (OMA) Without FEC Per Lane	RxSRS			-6	dBm	9
Receiver Reflectance				-26	dB	
Conditions of Stressed Receiver Sensitivity Test						
Vertical Eye Closure Penalty	VECP			2.5	dB	10
Stressed J2 Jitter With FEC	J2			TBD	UI	10
Stressed J4 Jitter With FEC	J4			TBD	UI	10
Stressed J2 Jitter Without FEC	J2			0.3	UI	11
Stressed J9 Jitter Without FEC	J9			0.47	UI	11
LOS Assert	LOSA	-25			dBm	
LOS De-Assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. 100G FR4 operation with the host-generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.1.
2. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Even if the TDP<1.0dB, the OMA (minimum) must exceed this value.
4. TDP does not include a penalty for multi-path interference (MPI).
5. Transmitter reflectance is defined looking into the transmitter.
6. With FEC hit ratio of $5x10^{-5}$. Without FEC hit ratio of $1x10^{-12}$.
7. Average receive power, per lane (minimum), is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
8. With FEC sensitivity is specified at $5x10^{-5}$ BER. Without FEC sensitivity is specified at $1x10^{-12}$ BER.
9. With FEC measured with conformance test signal at TP3 for BER=$5x10^{-5}$. Without FEC measured with conformance test signal at TP3 for BER=$1x10^{-12}$.
10. Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
11. Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J9 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

12. Unless otherwise stated, the above characteristics are defined under recommended operating conditions.
13. Power supply specifications, instantaneous, sustained, and steady state current compliant with QSFP28 MSA Power Classification.

Pin Descriptions

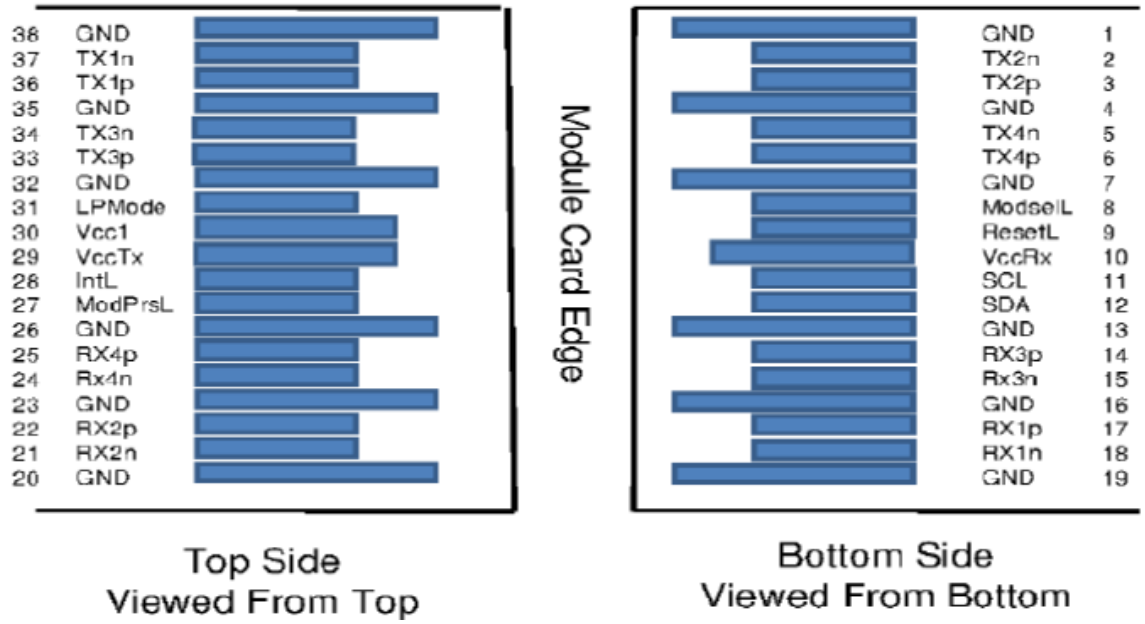
Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
1		GND	Module Ground.	1	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Power Supply Receiver.	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1
27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL	Interrupt.	3	
29		VccTx	+3.3V Transmitter Power Supply.	2	2
30		Vcc1	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMode	Low-Power Mode.	3	
32		GND	Module Ground.	1	1

33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3	
35		GND	Module Ground.	1	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

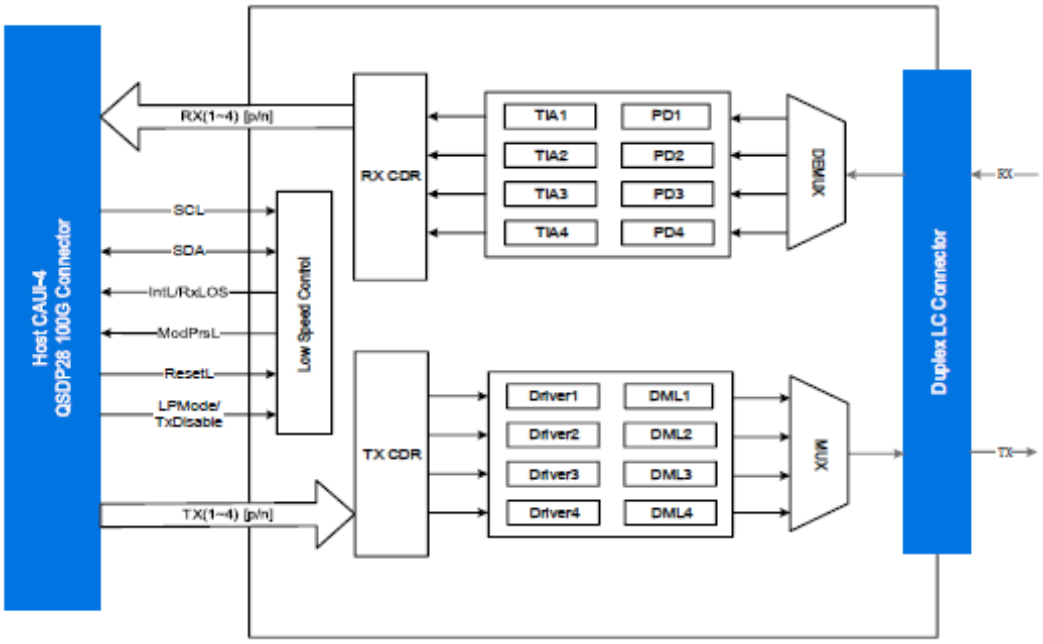
Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, Vcc1, and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1A.
3. The control signal interface is compliant with QSFP28 MSA. The following pins are provided to control the module or display the module's status: ModSelL, ResetL, LPMode/TxDis, ModPrsL, and IntL/RxLOSL. In addition, there is an industry standard 2-wire serial interface scaled for 3.3V LVTTL. The definition of the control signal interface and the registers of the serial interface memory are defined in the Control Interface Electrical Specifications section.

Electrical Pad Layout



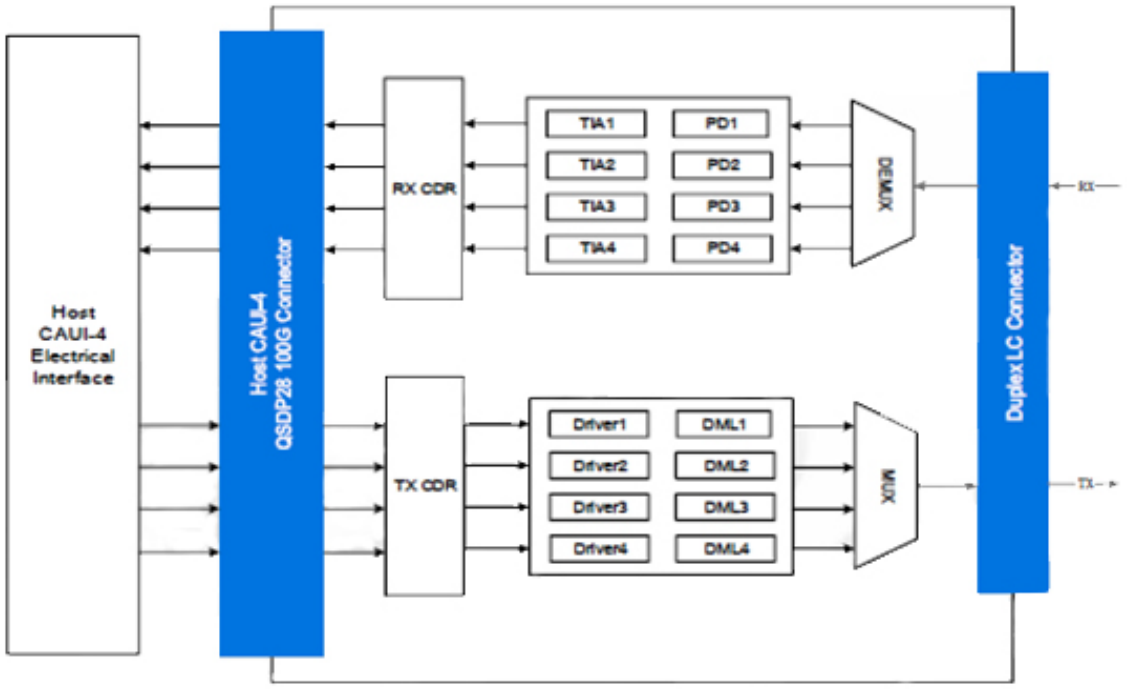
Transceiver Block Diagram



Notes:

1. The transmitter path of the transceiver contains a 4x25Gbps, CAUI-4 electrical input with equalization (EQ) block, optical multiplexer, 4 channels directly modulated lasers (DML), laser driver, clock and recovery (CDR), and diagnostic monitoring. The transmitter converts 4 channels of 25Gbps electrical input data to 4 channels of 25Gbps CWDM optical signals. The optical multiplexer multiplexes them into a single channel for 100Gbps optical transmission.
2. The receiver path of the transceiver contains 4-channel PIN photodiodes (PD), trans-impedance amplifiers (TIA), de-multiplexer, clock and recovery (CDR), and 4x25G CAUI-4 compliant electrical output blocks. The receiver optically de-multiplexes a 100Gbps optical input into 4 channels of CWDM optical signals, converts 4 channels of 25Gbps CWDM optical signals to 4 channels of 25Gbps electrical output data.

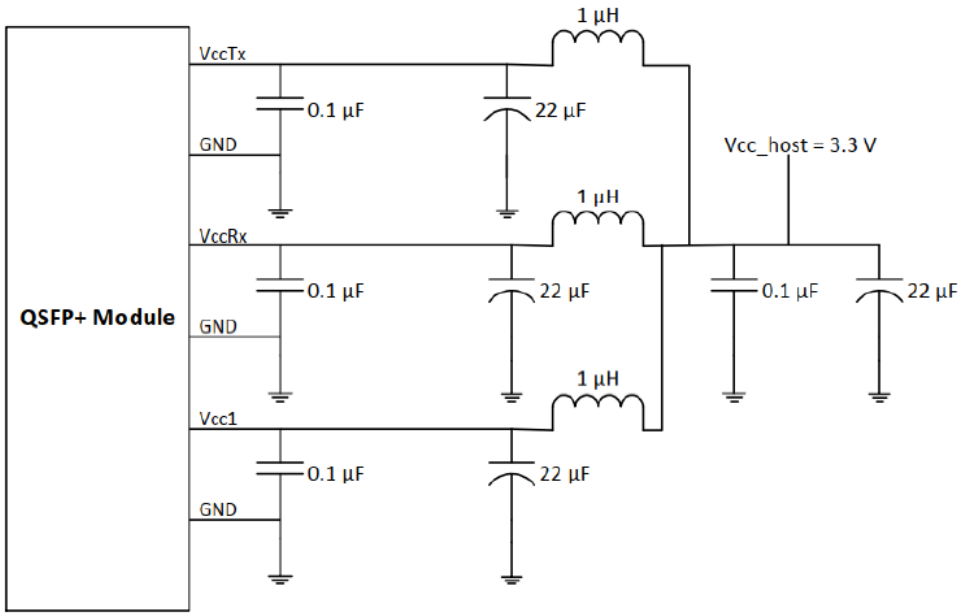
Application Reference Diagram



Notes:

1. The interface between the QSFP28 module and ASIC/SerDes is shown above. The high-speed signal lines are internally AC coupled, and the electrical inputs are internally terminated to 100Ω differential. All transmitter and receiver electrical channels are compliant to module CAUI-4 specifications per IEEE 802.3bm.

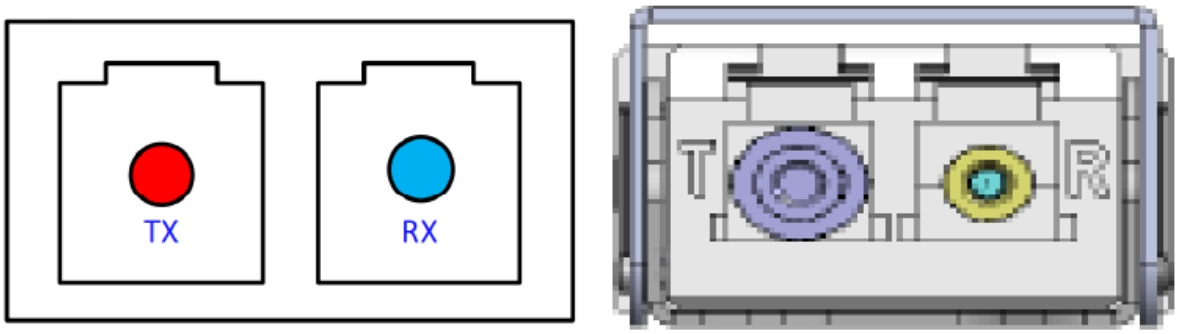
Host Board Power Supply Filter



Notes:

1. During power transient events, the host should ensure that any neighboring modules sharing the same supply stay within their specified supply voltage limits. The host should also ensure that the intrinsic noise of the power rail is filtered in order to guarantee the correct operation of the optical modules. The reference power supply filter is shown above.

Module Optical Interface

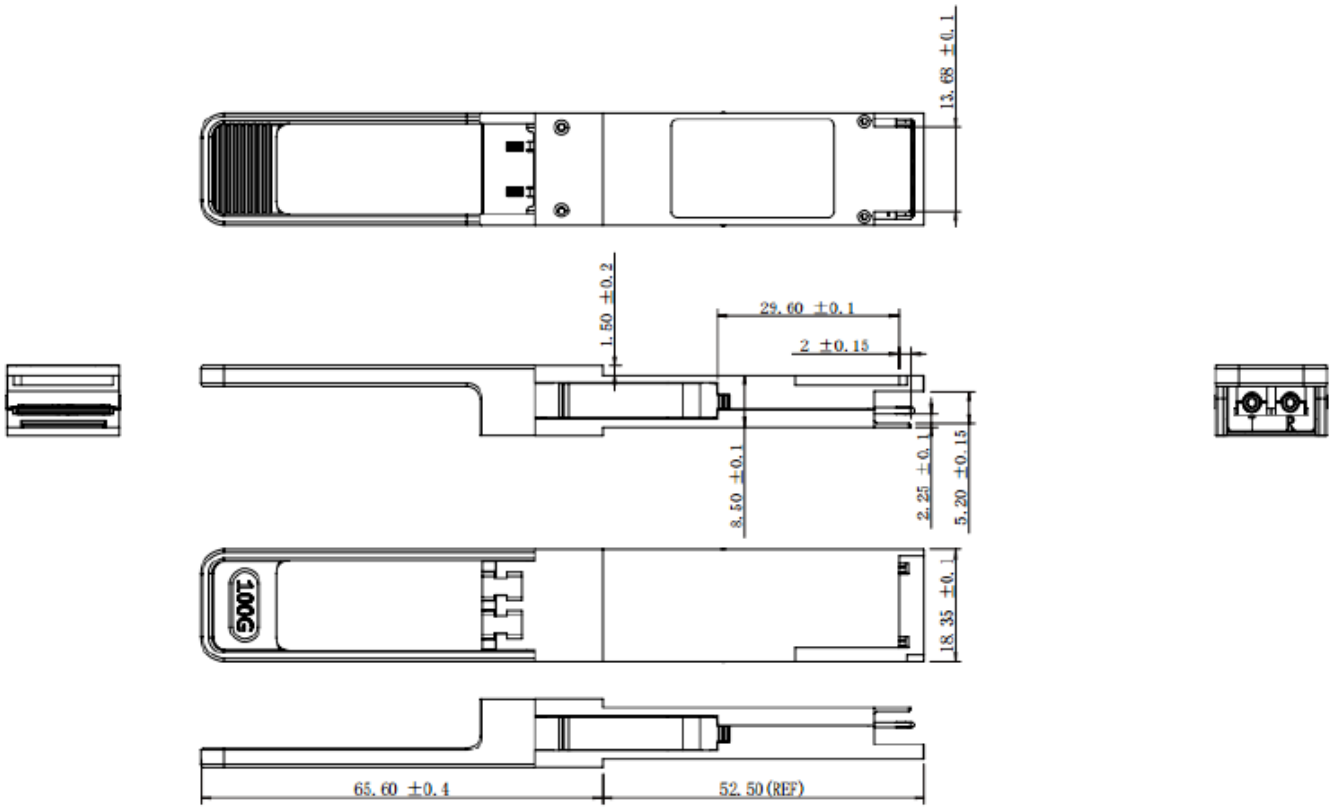


Notes:

1. Looking into the optical port. The optical interface port is a duplex LC connector as specified in IEC 61754-20.

Mechanical Specifications

The module is designed to meet the requirements defined by the QSFP28 MSA specifications.



All dimensions are in mm.