OSFP-400GB-DCO-ZR-OPC

MSA and TAA 400GBase-ZR Coherent OSFP Transceiver (SMF, 1528.77nm to 1567.13nm, 40km, LC, DOM)

Features

- OSFP MSA Compliant
- Supports OIF C-FEC
- Duplex LC Connector
- Module Thermal Protection
- Low-Power 7nm Coherent DSP
- Full C-band supporting 100GHz and 75GHz spacing
- High-performance tunable laser and COSA
- CMIS Rev 5.0 and Coherent CMIS (C-CMIS) 1.0 Compliant
- Telcordia GR-468-CORE Reliability Compliant
- OIF Implementation Agreement 400ZR 1.0 Compliant
- Commercial Temperature 0 to 70 Celsius
- RoHS Compliant and Lead Free

Applications:

- 400GBase Ethernet
- Access and Enterprise

Product Description

This MSA compliant OSFP transceiver provides 400GBase-ZR throughput up to 40km over single-mode fiber (SMF) using a wavelength of 1528.77nm to 1567.13nm via an LC connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	-0.3		3.6	V	
Operating Power Supply Voltage	3.135	3.3	3.465	V	
Storage Temperature	-40		85	°C	
Operating Case Temperature	0		70	°C	1
Relative Storage Humidity	5		85	%	2
Relative Operating Humidity	5		85	%	2
Target Reach (Application Code 0x01)	80		120	km	3
Module Insertion force			90	N	4
Module Extraction Force			50	N	5
Module Retention in Cage	90			N	6
Module Cycles	50			Cycles	7
Connector/Cage Cycles	100			Cycles	8
Receiver Total Optical Power			17	dBm	9
Input Channel Optical Power			10	dBm	9
ESD Sensitivity (HBM)			1000	V	10
			2000	V	11

Notes:

1. Operation guaranteed. Specification guaranteed from 20°C to 75°C.
2. Non-condensing.
3. Amplified, point-to-point, or DWDM noise-limited links. G.652 fiber.
4. Module is to be inserted into the connector and cage with the latch mechanism engaged.
5. Module is to be removed from the connector and cage with the latch mechanism disengaged.
6. No functional damage to the module, connector, or cage with the latching mechanism activated.
7. Number of cycles for an individual module is to be tested with the cage, connector, and module. Latches may be locked out during testing.
8. Number of cycles for the connector and cage with multiple modules to be tested with the cage, connector, and module. Latches may be locked out during testing.
9. Damage threshold.
10. High-speed pins ≥5Gbps.
11. Low-speed pins <5Gbps.
12. Absolute maximum ratings represent the damage threshold of the device. Damage may occur if the device is operated above the limits stated here except for brief excursions. Performance is not guaranteed, and reliability is not implied for operation at any condition outside of the recommended operating limits.

Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
SCL and SDA	VOL	0	0.4	V	1
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Signal	Ci		14	pF	
Total Bus Capacitance Load for SCL and SDA	Cb		100	pF	2
			200	pF	3
LPMode	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
ResetL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
LPMode, ResetL	|in|		360	uA	4
Module Inrush – Instantaneous Peak Duration			50	µs	5
Module Inrush – Initialization Time			500	ms	6
Inrush and Discharge Current			100	mA/µs	7
Module Power Supply Noise Tolerance (pk-pk)			66	mV	8
Module RMS Noise Output			30	mV	8
Sustained Peak Current at Hot Plug (Low-Power Mode)			500	mA	9
Steady State Current at Low-Power Mode			475	mA	10
Power Consumption at Low-Power Mode			1.5	W	10
Instantaneous Peak Current at High-Power Enable			7600	mA	11
Sustained Peak Current at High-Power Enable			6500	mA	12
Steady State Current at High-Power Enable			6400	mA	10
Power Consumption at High-Power Enable		17	19	W	13
Channel Frequency	191.3	193.7	196.1	THz	14
Channel Spacing	100			GHz	15
	75			GHz	16
	75			GHz	17
Network/Line Side Interface	478.75Gbps ± 10ppm				18
	OIF 400ZR				19
	DP-16QAM				20
	14.8% C-FEC				21
	$1.00E^{-15}$				22

Host/Client-Side Interface	425Gbps ± 100ppm	23
	GAUI-8 400GE	19
	PAM4	20
	RS(544, 514)	21

Notes:

1. iol (maximum) = 3mA for fast-mode or 20mA for fast-mode plus.
2. For 400KHz clock rate, used 3kΩ pull-up resistor, maximum. For 1000KHz clock rate, refer to QSFP-DD MSA.
3. For 400KHz clock rate, used 1.6kΩ pull-up resistor, maximum. For 1000KHz clock rate, refer to QSFP-DD MSA.
4. 0V<VIN<Vcc.
5. T_ip: refer to OSFP MSA.
6. T_init: refer to OSFP MSA.
7. T_didt: refer to OSFP MSA.
8. 10Hz to 10MHz.
9. Icc_sp_1: refer to OSFP MSA.
10. Refer to OSFP MSA.
11. Icc_ip_8: refer to OSFP MSA.
12. Icc_sp_8: refer to OSFP MSA.
13. Refer to OSFP MSA. C-FEC operating mode.
14. ITU-T grid.
15. 100GHz fixed grid per ITU-T G694.1.
16. 75GHz fixed grid per ITU-T G694.1.
17. Flexible DWDM grid per ITU-T G694.1.
18. Nominal C-FEC data rate.
19. Interface.
20. Modulation format.
21. FEC coding.
22. Post-FEC BER rate.
23. Nominal data rate.
24. Default fixed grid setting for OSFP modules.

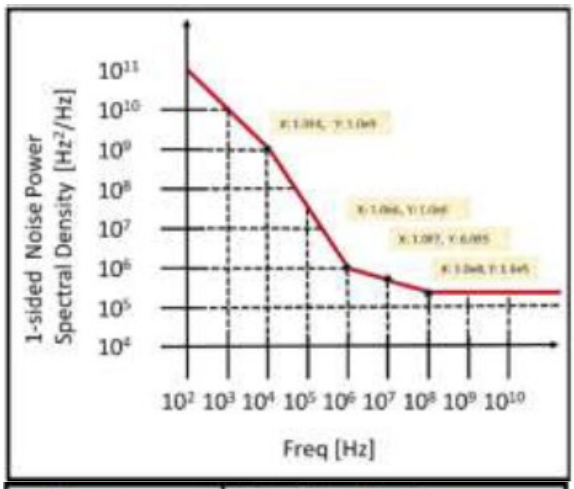
Optical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Notes
Transmitter					
Laser Frequency Accuracy	-1.8		1.8	GHz	1
Tx Spectral Excursion			32	GHz	
Laser Frequency Noise			See Mask		2
Laser RIN			-145	dB/Hz	3
			-140	dB/Hz	4
Maximum Output Signal Power Window	-10			dBm	5
Output Power Tuning Range	-14			dBm	
Output Optical Power Tuning Step Size	0.1			dB	
Total Output Power with Tx Disabled			-30	dBm	6
Total Output Power During Wavelength Switching			-30	dBm	
Inband (IB) OSNR	40			dB/0.1nm	7
Output-of-Band (OOB) OSNR	40			dB/0.1nm	8
Transmitter Reflectance			-20	dB	9
Transmitter Back Reflectance Tolerance			-24	dB	10
Transmitter Polarization Dependent Power Difference			1.5	dB	11
X-Y Skew			5	ps	12
DC I-Q Offset (Mean Per Polarization)			-26	dB	
I-Q Instantaneous Offset			-20	dB	
Mean I-Q Amplitude Imbalance			1	dB	
I-Q Phase Imbalance	-5		5	Degree	
I-Q Skew			0.75	ps	
Receiver					
Frequency Offset Between Received Carrier and LO	-3.6		3.6	GHz	13
Input Optics Power Range	-12		0	dBm	14
	-17		0	dBm	15
OSNR Tolerance			26	dB/0.1nm	16
Optical Return Loss	20			dB	17
CD Tolerance	2,400			ps/nm	18
Optical Path OSNR Penalty Tolerance			0.5	dB	19
Average PMD Tolerance (DGD, SOPMD)	10			ps	20
Peak PDL Tolerance	3.5			dB	21

Tolerance to Change in SOP	50			krad/s	22
Optical Input Power Transient Tolerance	±2			dB	23
Optical Rx_LOS Assert Threshold	-20	-18	-16	dBm	24
Optical Rx_LOS Hysteresis		1.0	2.5	dB	25

Notes:

1. Offset from channel frequency set point. The receiver LO has the same frequency accuracy.
2. No modulation. Mask does not apply to spurs. Measurement Resolution BW shall be between $10E^{-1}$ and $10E^{-6}$ of the frequency of interest. High-frequency component of the phase noise (100MHz and above) is consistent with a 500KHz laser linewidth. The receiver LO has the same linewidth.



Frequency [Hz]	1- sided Noise power spectral density [Hz²/Hz]
1.0e+02	1.0e+11
1.0e+04	1.0e+09
1.0e+06	1.0e+06
1.0e+07	6.0e+05
1.0e+08	1.6e+05
1.0e+09	1.6e+05

3. 0.2GHz≤f≤10GHz (average).
4. 0.2GHz≤f≤10GHz (peak).
5. Measured at Tx optical connector.
6. Tx_Disable = True.
7. Inband OSNR is defined within the bandwidth of the Tx spectral excursion given in (Tx Spectral Excursion). The 0.1nm bandwidth for the Inband OSNR refers to 12.5GHz optical bandwidth.
8. Channel total power over peak noise power in the whole frequency range measure with 0.1nm resolution bandwidth. The 0.1nm bandwidth for the OOB OSNR refers to 12.5GHz optical bandwidth.
9. Looking into the Tx.
10. Light reflected relative to the Tx output power back to the transmitter while still meeting Tx optical

performance requirements.

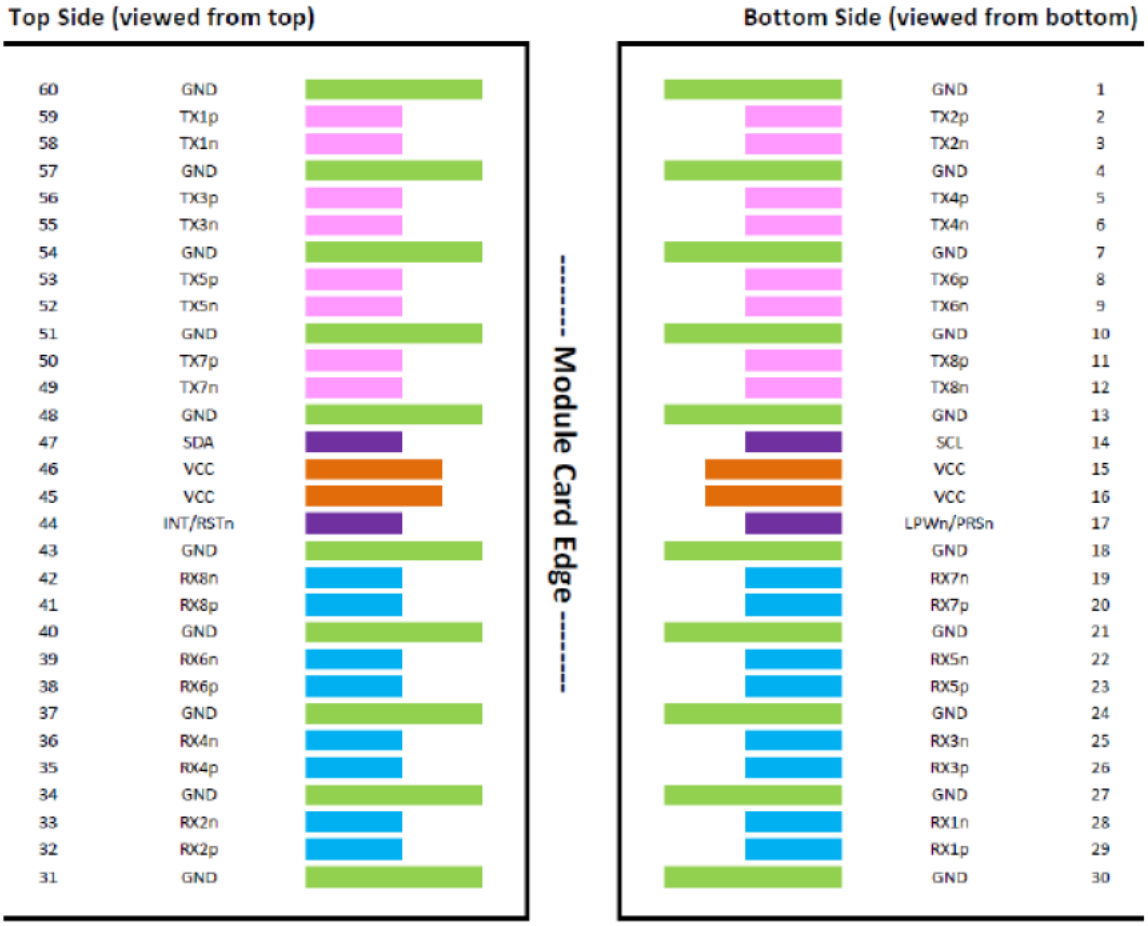
11. Power difference between X and Y polarization.
12. X-Y skew.
13. Acquisition range.
14. Signal power of the channel at the OSNR performance defined in frequency offset between received carrier and LO.
15. At 35dB OSNR performance.
16. At C-FEC threshold. The OSNR tolerance is referenced to an optical bandwidth of 0.1nm or 12.5GHz.
17. Optical reflectance at Rx optical connector.
18. Tolerance to Chromatic Dispersion.
19. OSNR tolerance penalty over 26dB/0.1nm due to reflections and dispersion. Range from 0ps/nm to 2,400ps/nm.
20. Minimum tolerance limits include the transmitter maximum X-Y skew. Tolerance to PMD with ≤0.5dB penalty to OSNR sensitivity when change in SOP is ≤1rad/ms. PMD (average) is equivalent to DGDmean. DGDmax occurs when SOPMD=0ps2. Due to the statistical nature of PMD, the DGDmax to DGDmean ratio is calculated at 3.3 ($4.1x10E^{-6}$; probability that the DGDmean is greater than DGDmax).
21. Tolerance to peak PDL with ≤1.3dB penalty to OSNR sensitivity when change in SOP is ≤1rad/ms.
22. Tolerance to change in SOP with ≤0.5dB additional OSNR penalty over all PMD and PDL values defined in Average PMD Tolerance (DGD, SOPMD) and Peak PDL Tolerance.
23. Tolerance to change in input power with ≤0.5dB penalty to OSNR sensitivity when transient received power is within range defined by input power range. Rise/fall time of power change defined by 20-80% of 50µs or slower.
24. Channel power. Optical Rx_LOS thresholds must be programmable to support different ranges for each application.
25. Rx_LOS cleared.

Pin Descriptions

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground.
2	CML-I	Tx2+	Transmitter Non-Inverted Data.
3	CML-I	Tx2-	Transmitter Inverted Data.
4		GND	Module Ground.
5	CML-I	Tx4+	Transmitter Non-Inverted Data.
6	CML-I	Tx4-	Transmitter Inverted Data.
7		GND	Module Ground.
8	CML-I	Tx6+	Transmitter Non-Inverted Data.
9	CML-I	Tx6-	Transmitter Inverted Data.
10		GND	Module Ground.
11	CML-I	Tx8+	Transmitter Non-Inverted Data.
12	CML-I	Tx8-	Transmitter Inverted Data.
13		GND	Module Ground.
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.
15		Vcc	+3.3V Power Supply.
16		Vcc	+3.3V Power Supply.
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.
18		GND	Module Ground.
19	CML-O	Rx7-	Receiver Inverted Data.
20	CML-O	Rx7+	Receiver Non-Inverted Data.
21		GND	Module Ground.
22	CML-O	Rx5-	Receiver Inverted Data.
23	CML-O	Rx5+	Receiver Non-Inverted Data.
24		GND	Module Ground.
25	CML-O	Rx3-	Receiver Inverted Data.
26	CML-O	RX3+	Receiver Non-Inverted Data.
27		GND	Module Ground.
28	CML-O	Rx1-	Receiver Inverted Data.
29	CML-O	Rx1+	Receiver Non-Inverted Data.
30		GND	Module Ground.
31		GND	Module Ground.
32	CML-O	Rx2+	Receiver Non-Inverted Data.
33	CML-O	Rx2-	Receiver Inverted Data.
34		GND	Module Ground.
35	CML-O	Rx4+	Receiver Non-Inverted Data.
36	CML-O	Rx4-	Receiver Inverted Data.

37		GND	Module Ground.
38	CML-O	Rx6+	Receiver Non-Inverted Data.
39	CML-O	Rx6-	Receiver Inverted Data.
40		GND	Module Ground.
41	CML-O	Rx8+	Receiver Non-Inverted Data.
42	CML-O	Rx8-	Receiver Inverted Data.
43		GND	Module Ground.
44	Multi-Level	INT/RSTn	Module Interrupt/Module Reset.
45		Vcc	+3.3V Power Supply.
46		Vcc	+3.3V Power Supply.
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.
48		GND	Module Ground.
49	CML-I	Tx7-	Transmitter Inverted Data.
50	CML-I	Tx7+	Transmitter Non-Inverted Data.
51		GND	Module Ground.
52	CML-I	Tx5-	Transmitter Inverted Data.
53	CML-I	Tx5+	Transmitter Non-Inverted Data.
54		GND	Module Ground.
55	CML-I	Tx3-	Transmitter Inverted Data.
56	CML-I	Tx3+	Transmitter Non-Inverted Data.
57		GND	Module Ground.
58	CML-I	Tx1-	Transmitter Inverted Data.
59	CML-I	Tx1+	Transmitter Non-Inverted Data.
60		GND	Module Ground.

Electrical Pin-Out Details



Timing Specifications of Control and Monitoring I/O

Parameter	Min.	Max.	Unit	Notes
TWI Management Interface	0	400	KHz	1
	0	1000	KHz	2
ModulePwrDn Asserting Time		500	ms	3
Tx_Disable Assert Time		100	ms	4
		100	ms	5
Tx_Disable De-Assert Time		400	ms	6
		400	ms	7
Transmitter Turn-Up Time from Warm Start		180	s	8
Transmitter Turn-Up Time from Cold Start		200	s	9
Transmitter Wavelength Switching Timing		50	s	10
Receiver Turn-Up Time from Warm Start		10	s	11
Receiver Turn-Up Time from Cold Start		200	s	12
ResetL Assert Time	10		µs	13

MgmtInitDuration		2000	ms	14
IntL Assert Time		200	ms	15
IntL De-Assert Time		500	µs	16
Rx_LOS Assert Time		100	ms	17
Flag Assert Time		1	s	18
Mask Assert Time		100	ms	19
Mask De-Assert Time		100	ms	20
Rx Squelch Assert Time		500	ms	21
Rx Squelch De-Assert Time		500	ms	22
Rx Output Disable Assert Time		500	ms	23
Rx Output Disable De-Assert Time		500	ms	24
Squelch Disable Assert Time		500	ms	25
ModulePwrUp_MaxDuration		180	s	26
ModulePwrDn_MaxDuration	500	1000	ms	27
DataPathInit_MaxDuration	10	60	s	28
DataPathDeInit_MaxDuration	1	5	s	29
DataPathTxTurnOn_MaxDuration	500	1000	ms	30
DataPathTxTurnOff_MaxDuration	10	50	ms	31
RxLinkUp_MaxDuration		8	s	32

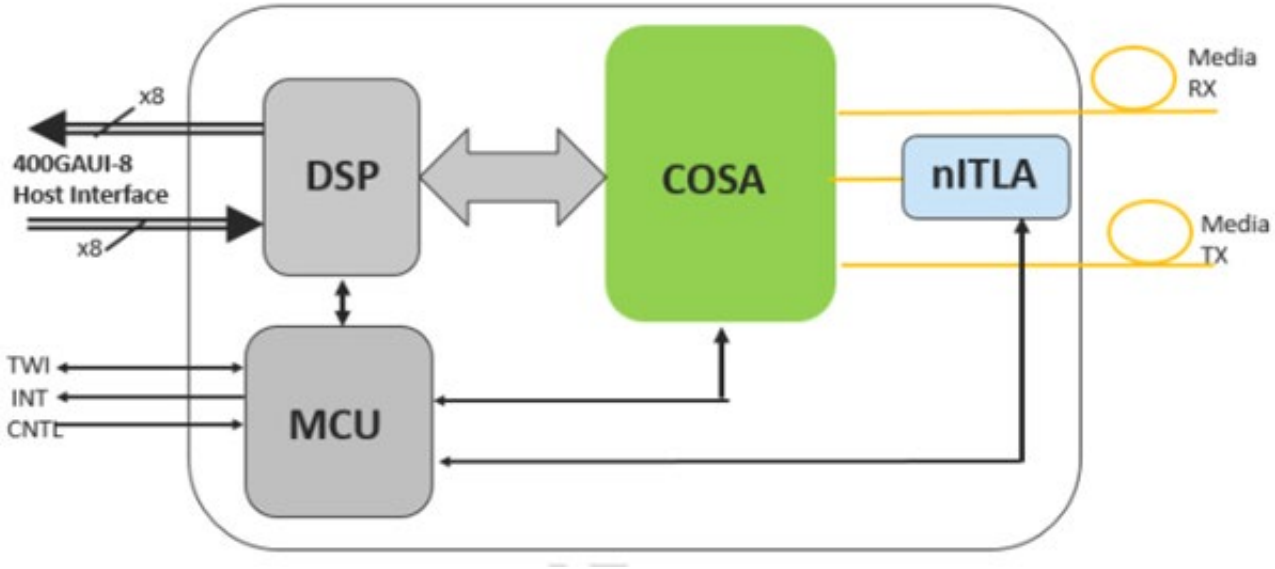
Notes:

1. Clock frequency (fast-mode).
2. Clock frequency (fast-mode plus).
3. High-power mode to low-power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr.
4. The maximum transmitter turn-off time from any condition that results in Tx_Disable = True to reach the Tx output power given by Total Output Power with Tx Disabled.
5. Time from the stop condition of the Tx_Disable write sequence until optical output falls below 10% of nominal.
6. Time from any condition that results in Tx_Disable = False to reach the Tx output power given by the Allowable Output Signal Power Window.
7. Time from Tx_Disable bit cleared (value = 0B) until optical output rises above 90% of nominal.
8. The maximum time from ModuleLowPwr de-asserted to DataPathActivated state.
9. The maximum time from de-assertion of ResetS==False to DataPathActivated state while LoPwrS=False.
10. The maximum time of change wavelengths including turn-up time.
11. Upon Rx_LOS de-assert, receiver has been turned up previously.
12. From module reset with valid optical input signal present.
13. Minimum pulse time on the ResetL signal to initiate a module reset.
14. Time from power on, hot plug, or rising edge of reset until completion of the MgmtInit State.

15. Time from occurrence of condition triggering IntL until VOUT: IntL=VOL.
16. Time from clear on read operation of associated flag until VOUT: IntL=VOH. This includes de-assert times for Rx_LOS, Tx_Fault, and other flag bits.
17. Time from Rx_LOS state to Rx_LOS bit set (value=1b) and IntL asserted. Channel power.
18. Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
19. Time from mask bit set (value=1b) until associated IntL assertion is inhibited.
20. Time from mask bit cleared (value=0b) until associated IntL operation resumes.
21. Time from loss of line-side Rx input signal until the squelched output condition is reached.
22. Time from resumption of line-side Rx input signals until normal Rx output condition is reached.
23. Time from Rx Output Disable bit set (value=1b) until Rx output falls below 10% of nominal.
24. Time from Rx Output Disable bit cleared (value=0b) until Rx output rises above 90% of nominal.
25. This applies to Rx and Tx squelch and is the time from bit set (value=1b) until squelch functionality is disabled.
26. This applies to maximum duration of the ModulePwrUp state.
27. This applies to maximum duration of the ModulePwrDn state.
28. This applies to maximum duration of the DataPathInit state.
29. This applies to maximum duration of the DataPathDeInit state.
30. This applies to maximum duration of the DataPathTxTurnOn state.
31. This applies to maximum duration of the DataPathTxTurnOff state.
32. This applies to maximum duration of the valid signal toward the host after Rx_LOS de-assert.

Block Diagram

The OSFP 400G ZR coherent transceiver incorporates a linewidth tunable laser that supports DWDM links of 400Gbps traffic over 120km. Utilizing the latest Coherent Optical Subassembly (COSA) and nano-ITLA, this module delivers the latest 7nm DSP, reduced power consumption, and engineered heatsink that assures reliability in high-density environments.



Mechanical Specifications