



QDD-400GB-ADAC8M-OPC

MSA and TAA 400GBase-CU QSFP-DD to QSFP-DD Direct Attach Cable (Active Twinax, 8m)

Features

- Module Compliant to QSFP-DD MSA
- Transmission Data Rate up to PAM4 53.125Gbps Per Channel
- Low Power Consumption, Meeting 1.5W Module LP Mode
- Enables a Transparent ACC Solution Meeting all IEEE 200GBASE-CR4 Auto-Negotiation and Link Training
- Low Latency
- Supports Device Programming by MCU with I2C
- Operates from a Single 3.3V Power Supply with an Integrated Power On Reset (POR)
- Operating Temperature: 0 to 70 Celsius
- RoHS Compliant and Lead-Free



Applications:

- 400GBase Ethernet

Product Description

This is an MSA compliant 400GBase-CU QSFP-DD to QSFP-DD direct attach cable that operates over active copper with a maximum reach of 8.0m (26.2ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V _{cc}	-0.3	3.3	3.6	V	
Storage Temperature	T _{stg}	-40		85	°C	
Operating Case Temperature	T _c	0		70	°C	
Humidity	RH	5		85	%	
Data Rate			400		Gbps	

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Length	L			8	M	
AWG			26		AWG	
Jacket Material		Plastic Braided Mesh, Orange				

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input Amplitude		800		1200	mVp-p	
Control Logic Input Low Voltage	V _{IL}	-0.3		0.35*V _{cc}	V	
Control Logic Input High Voltage	V _{IH}	0.65* V _{cc}		V _{cc} +0.3	V	
Control Logic Input Low Current	I _{IL}	-100		+100	uA	
Control Logic Input High Current	I _{IH}	-100		+100	uA	
Output Logic Low	V _{OL}			0.25* V _{cc}	V	
I2C Master Mode Output Frequency				400	kHz	

High-Speed Specifications

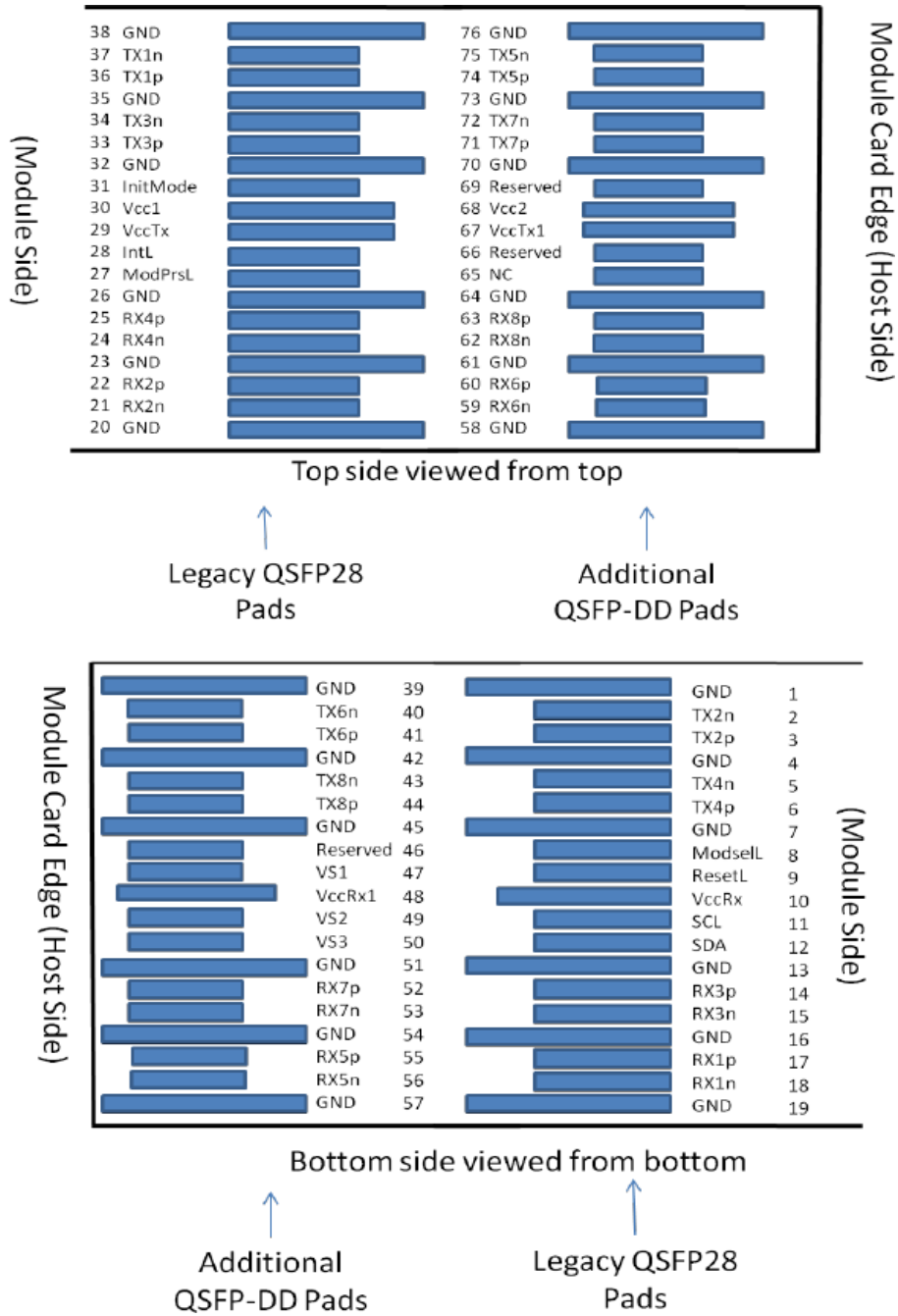
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Raw Cable Differential Impedance	Z _{ca}	90		110	Ω	
PCBA Differential Impedance	Z _{pcba}	85		115	Ω	
Maximum Insertion Loss at 13.28GHz	SDD21	8		17.16	dB	
Other SI Performance		Compliant with IEEE802.3cd&bj				
Minimum COM	COM	3			dB	
BER with FEC				2.4x10 ⁻⁴		

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence
1		GND	Module Ground.	1B
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3B
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3B
4		GND	Module Ground.	1B
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3B
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3B
7		GND	Module Ground.	1B
8	LVTTL-I	ModSelL	Module Select.	3B
9	LVTTL-I	ResetL	Module Reset.	3B
10		VccRx	+3.3V Receiver Power Supply.	2B
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3B
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3B
13		GND	Module Ground.	1B
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3B
15	CML-O	Rx3-	Receiver Inverted Data Output.	3B
16		GND	Module Ground.	1B
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3B
18	CML-O	Rx1-	Receiver Inverted Data Output.	3B
19		GND	Module Ground.	1B
20		GND	Module Ground.	1B
21	CML-O	Rx2-	Receiver Inverted Data Output.	3B
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3B
23		GND	Module Ground.	1B
24	CML-O	Rx4-	Receiver Inverted Data Output.	3B
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3B
26		GND	Module Ground.	1B
27	LVTTL-O	ModPrsL	Module Present.	3B
28	LVTTL-O	IntL	Interrupt.	3B
29		VccTx	+3.3V Transmitter Power Supply.	2B
30		Vcc1	+3.3V Power Supply.	2B
31	LVTTL-I	InitMode	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	3B
32		GND	Module Ground.	1B
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3B
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3B
35		GND	Module Ground.	1B
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3B
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3B
38		GND	Module Ground.	1B

39		GND	Module Ground.	1A
40	CML-I	Tx6-	Transmitter Inverted Data Input.	3A
41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	3A
42		GND	Module Ground.	1A
43	CML-I	Tx8-	Transmitter Inverted Data Input.	3A
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	3A
45		GND	Module Ground.	1A
46		Reserved	For Future Use.	3A
47		VS1	Module Vendor-Specific 1.	3A
48		VccRx1	+3.3V Receiver Power Supply.	2A
49		VS2	Module Vendor-Specific 2.	3A
50		VS3	Module Vendor-Specific 3.	3A
51		GND	Module Ground.	1A
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	3A
53	CML-O	Rx7-	Receiver Inverted Data Output.	3A
54		GND	Module Ground.	1A
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	3A
56	CML-O	Rx5-	Receiver Inverted Data Output.	3A
57		GND	Module Ground.	1A
58		GND	Module Ground.	1A
59	CML-O	Rx6-	Receiver Inverted Data Output.	3A
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	3A
61		GND	Module Ground.	1A
62	CML-O	Rx8-	Receiver Inverted Data Output.	3A
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	3A
64		GND	Module Ground.	1A
64		NC	Not Connected.	3A
66		Reserved	For Future Use.	3A
67		VccTx1	+3.3V Transmitter Power Supply.	2A
68		Vcc2	+3.3V Power Supply.	2A
69		Reserved	For Future Use.	3A
70		GND	Module Ground.	1A
71	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	3A
72	CML-I	Tx7-	Transmitter Inverted Data Input.	3A
73		GND	Module Ground.	1A
74	CML-I	Tx5+	Transmitter Non-Inverted Data Input.	3A
75	CML-I	Tx5-	Transmitter Inverted Data Input.	3A
76		GND	Module Ground.	1A

Electrical Pin-Out Details



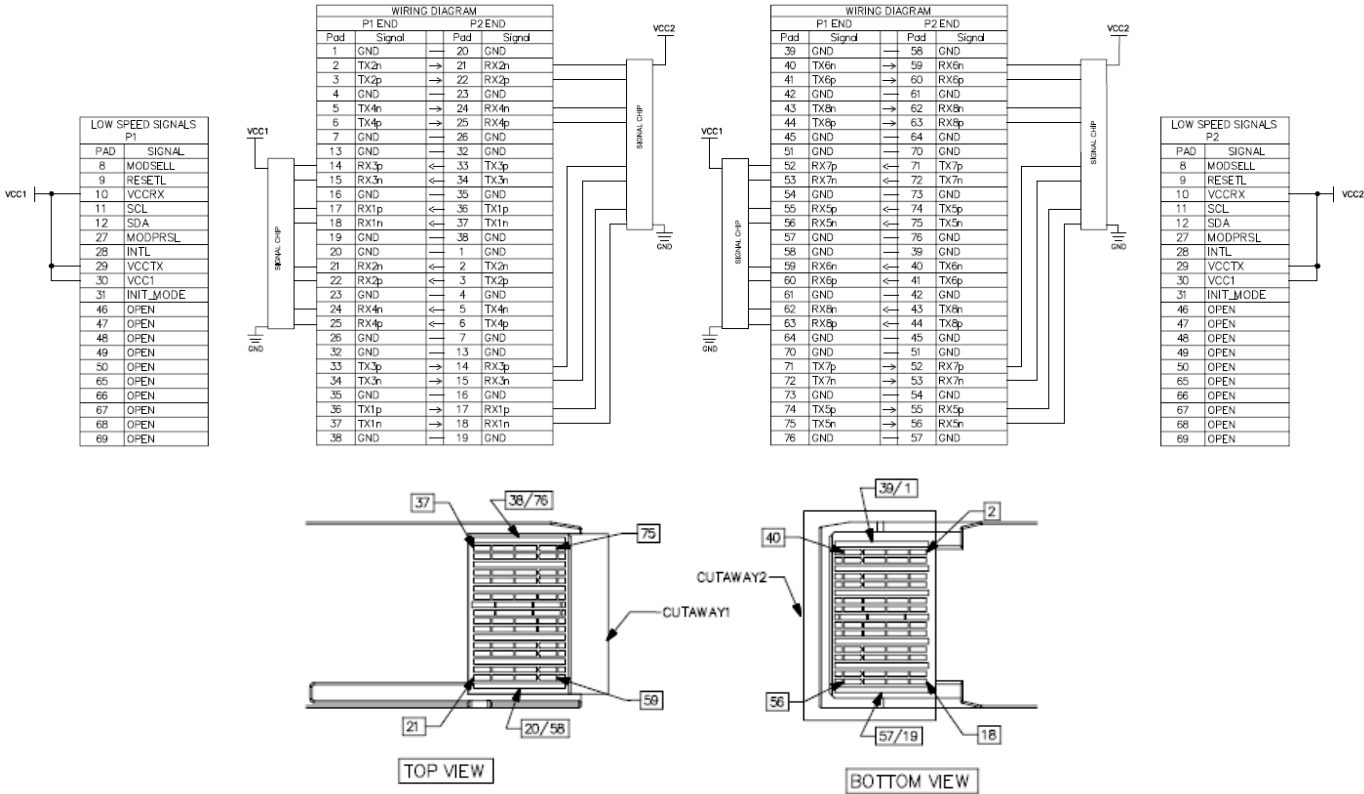
Bending Radius

Wire Gauge	OD (Ref)	Minimum Bend Radius	Bend Space
26AWG	12.1mm	24.2mm	68mm

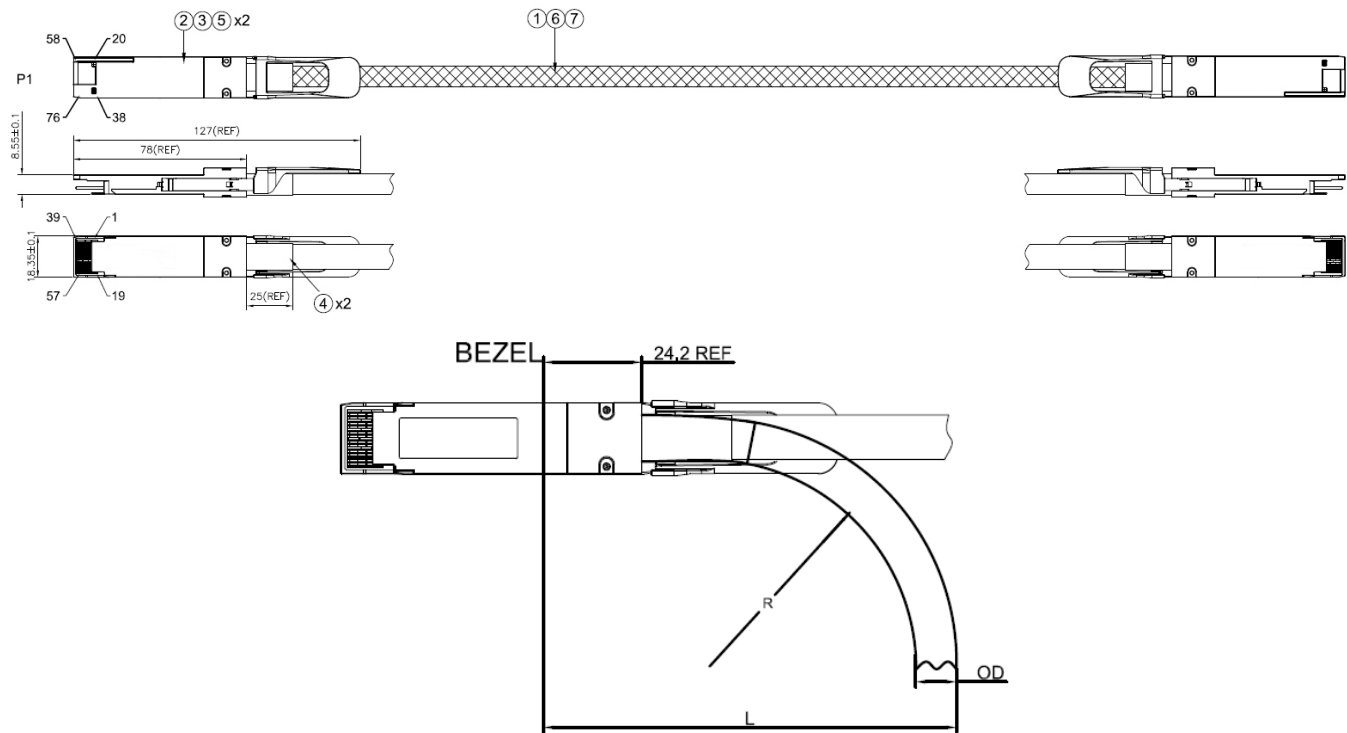
Block Diagram



Wiring Table



Mechanical Specifications



Item	Name	Description	Quantity
1	Raw Cable	SAS Cable, 56G, RoHS 2.0	A/R
2	PCBA	QSFP-DD PCBA with Signal Chip, 76 P, Gold 30u" Minimum	2
3	QSFP-DD Conn. Assembly	Zinc Alloy, Plated Nickel Over Copper + Stainless Steel Latch + Pull Tab	2
4	Heat Shrink Tube	Black	A/R
5	Back Shell Label	Black Shell Label, 29.5*10mm	2
6	Plastic Braided Mesh	Pet, Orange	A/R
7	Braid Shield	Copper, Braid	A/R

Notes:

1. Raw cable impedance: 100±10Ω.
Mated connector impedance: 100±15Ω.
Rise time: 25ps (20-80%).
2. High-frequency test according to IEEE802.3cd standard.
3. All material must comply with RoHS 2.0.

OptioConnect

Innovation for the Future of High-Speed Networking

Who We Are

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

Our Mission

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.

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