



### **QSFPDD4-400G-AOC17M-OPC**

MSA and TAA 400GBase-AOC QSFP-DD to QSFP-DD Active Optical Cable (850nm, MMF, 17m)

#### **Features**

- Compliant to QSFP-DD MSA Standards
- 8 Parallel Full-Duplex Channels
- Compliant to IEEE802.3bs
- Up to 100m OM3 MMF Transmission
- Operating Temperature: 0 to 70 Celsius
- CMIS 4.0
- 8x53.125Gbps Electrical Interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) Per Channel
- Maximum Power Consumption: 10.5W
- RoHS Compliant and Lead-Free



#### **Applications:**

- 400GBase Ethernet

#### **Product Description**

This is an MSA Compliant compatible 400GBase-AOC QSFP-DD to QSFP-DD active optical cable that operates over active fiber with a maximum reach of 17.0m (55.8ft). At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

## General Specifications

| Parameter                   | Symbol | Min. | Typ.    | Max. | Unit | Notes |
|-----------------------------|--------|------|---------|------|------|-------|
| Storage Temperature         | Tstg   | -40  |         | 85   | °C   |       |
| Operating Case Temperature  | Tc     | 0    |         | 70   | °C   |       |
| Supply Voltage              | Vcc    | -0.5 |         | 3.6  | V    |       |
| Relative Operating Humidity | RH     | 0    |         | 85   | %    |       |
| Data Rate Per Lane          |        |      | 26.5625 |      |      | PAM4  |
| Data Rate Accuracy          |        | -100 |         | 100  | ppm  |       |
| Link Distance with OM3      | D      | 0.5  |         | 100  | M    | 1     |

### Notes:

1. FEC is required on the host system to support the maximum distance.

## Electrical Specifications

| Parameter                                           | Symbol | Min.                             | Typ.  | Max.                 | Unit  | Notes |
|-----------------------------------------------------|--------|----------------------------------|-------|----------------------|-------|-------|
| Power Supply Voltage                                | Vcc    | 3.135                            | 3.3   | 3.465                | V     |       |
| Pre-FEC Bit Error Ratio                             |        |                                  |       | 2.4x10 <sup>-4</sup> |       |       |
| Post-FEC Bit Error Ratio                            |        |                                  |       | 1x10 <sup>-12</sup>  |       | 1     |
| Power Consumption                                   |        |                                  |       | 10.5                 | W     |       |
| Supply Current                                      | Icc    |                                  |       | 3.18                 | A     |       |
| <b>Transmitter</b>                                  |        |                                  |       |                      |       |       |
| Signaling Rate Per Lane                             | TP1    | 26.5625 ± 100ppm                 |       |                      | GBd   |       |
| Differential Pk-Pk Input Voltage Tolerance          | TP1a   | 900                              |       |                      | mVp-p | 2     |
| Differential Termination Mismatch                   | TP1    |                                  |       | 10                   | %     |       |
| Differential Input Return Loss                      | TP1    | IEEE 802.3-2015 Equation (83E-5) |       |                      | dB    |       |
| Differential to Common-Mode Input Return Loss       | TP1    | IEEE 802.3-2015 Equation (83E-6) |       |                      | dB    |       |
| Module Stressed Input Test                          | TP1a   | See IEEE 802.3bs 120E.3.4.1      |       |                      |       | 3     |
| Single-Ended Voltage Tolerance Range (Minimum)      | TP1a   | -0.4 to 3.3                      |       |                      | V     |       |
| DC Common-Mode Input Voltage                        | TP1    | -350                             |       | 2850                 | mV    | 4     |
| <b>Receiver</b>                                     |        |                                  |       |                      |       |       |
| Signaling Rate Per Lane                             | TP4    | 26.5625 ± 100ppm                 |       |                      | GBd   |       |
| Differential Pk-Pk Output Voltage                   | TP4    |                                  |       | 900                  | mVp-p |       |
| AC Common-Mode Output Voltage (RMS)                 | TP4    |                                  |       | 17.5                 | mV    |       |
| Differential Termination Mismatch                   | TP4    |                                  |       | 10                   | %     |       |
| Differential Output Return Loss                     | TP4    | IEEE 802.3-2015 Equation (83E-2) |       |                      |       |       |
| Common- to Differential-Mode Conversion Return Loss | TP4    | IEEE 802.3-2015 Equation (83E-3) |       |                      |       |       |
| Transition Time (20-80%)                            | TP4    | 9.5                              |       |                      | ps    |       |
| Near-End Eye Symmetry Mask Width (ESMW)             | TP4    |                                  | 0.265 |                      | UI    |       |
| Near-End Eye Height (Differential)                  | TP4    | 70                               |       |                      | mV    |       |
| Far-End Eye Symmetry Mask Width (ESMW)              | TP4    |                                  | 0.2   |                      | UI    |       |
| Far-End Eye Height (Differential)                   | TP4    | 30                               |       |                      | mV    |       |
| Far-End Pre-Cursor ISI Ratio                        | TP4    | -4.5                             |       | 2.5                  | %     |       |
| Common-Mode Output Voltage (Vcm)                    | TP4    | -350                             |       | 2850                 | mV    | 4     |

### Notes:

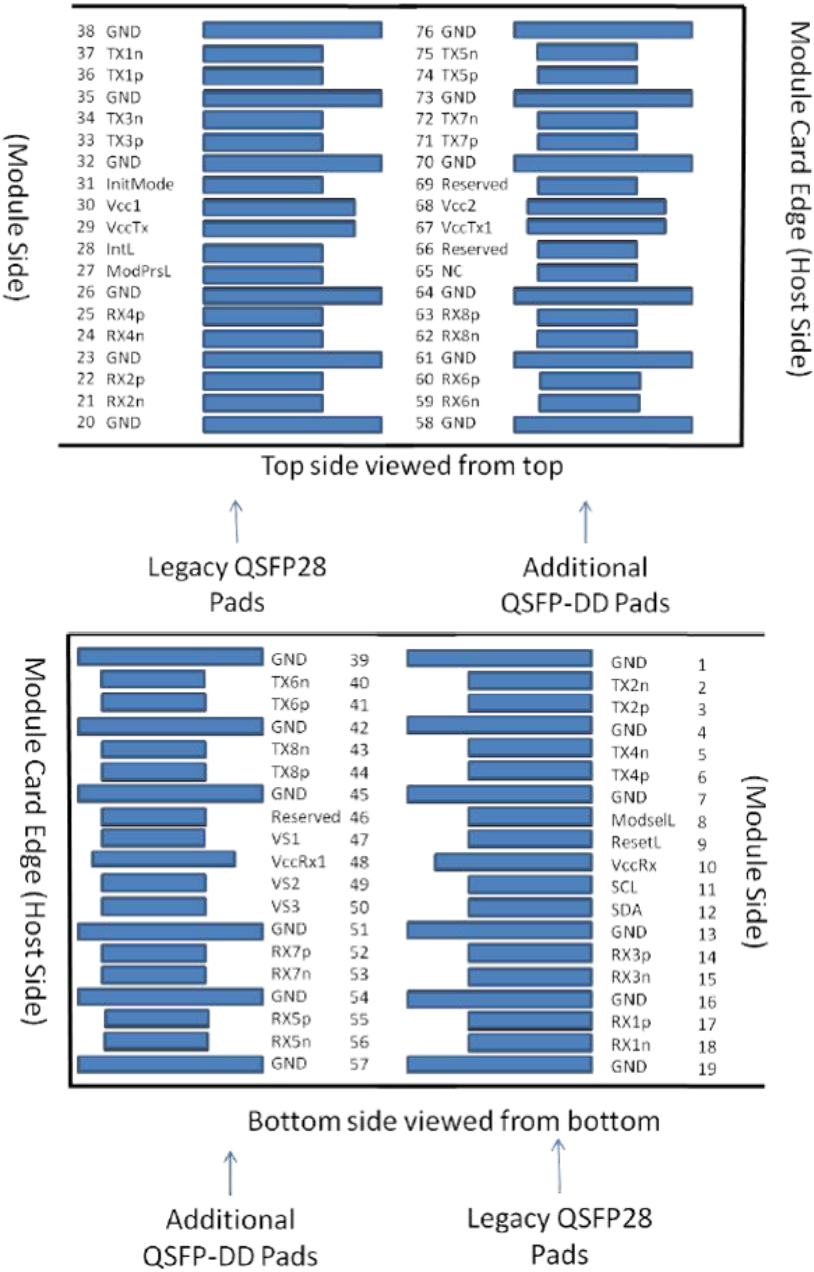
1. FEC is provided by the host system.
2. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets BER specified in IEEE 802.3bs 120E.1.1.
4. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

## Pin Descriptions

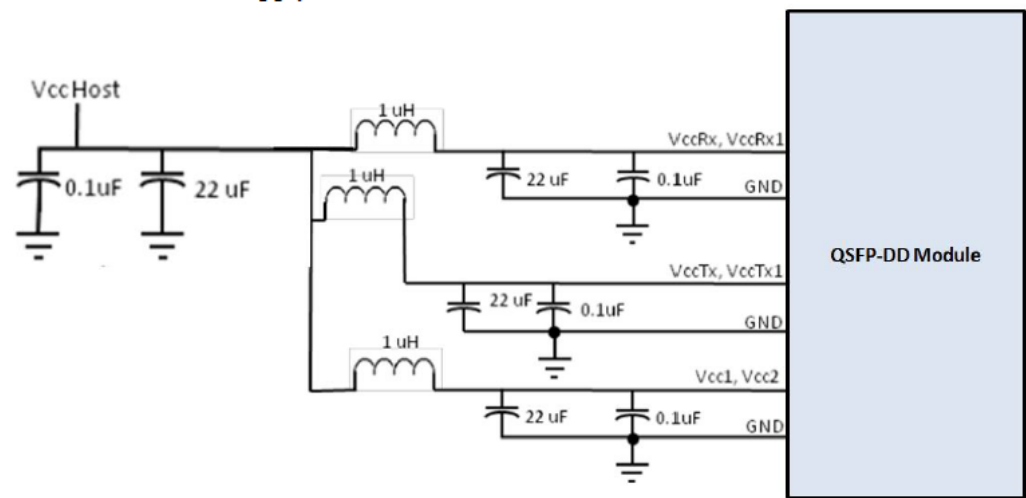
| Pin | Logic       | Symbol   | Name/Description                                                                     | Plug Sequence | Notes |
|-----|-------------|----------|--------------------------------------------------------------------------------------|---------------|-------|
| 1   |             | GND      | Module Ground.                                                                       | 1B            |       |
| 2   | CML-I       | Tx2-     | Transmitter Inverted Data Input.                                                     | 3B            |       |
| 3   | CML-I       | Tx2+     | Transmitter Non-Inverted Data Input.                                                 | 3B            |       |
| 4   |             | GND      | Module Ground.                                                                       | 1B            |       |
| 5   | CML-I       | Tx4-     | Transmitter Inverted Data Input.                                                     | 3B            |       |
| 6   | CML-I       | Tx4+     | Transmitter Non-Inverted Data Input.                                                 | 3B            |       |
| 7   |             | GND      | Module Ground.                                                                       | 1B            |       |
| 8   | LVTTTL-I    | ModSelL  | Module Select.                                                                       | 3B            |       |
| 9   | LVTTTL-I    | ResetL   | Module Reset.                                                                        | 3B            |       |
| 10  |             | VccRx    | +3.3V Receiver Power Supply.                                                         | 2B            |       |
| 11  | LVC MOS-I/O | SCL      | 2-Wire Serial Interface Clock.                                                       | 3B            |       |
| 12  | LVC MOS-I/O | SDA      | 2-Wire Serial Interface Data.                                                        | 3B            |       |
| 13  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 14  | CML-O       | Rx3+     | Receiver Non-Inverted Data Output.                                                   | 3B            |       |
| 15  | CML-O       | Rx3-     | Receiver Inverted Data Output.                                                       | 3B            |       |
| 16  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 17  | CML-O       | Rx1+     | Receiver Non-Inverted Data Output.                                                   | 3B            |       |
| 18  | CML-O       | Rx1-     | Receiver Inverted Data Output.                                                       | 3B            |       |
| 19  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 20  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 21  | CML-O       | Rx2-     | Receiver Inverted Data Output.                                                       | 3B            |       |
| 22  | CML-O       | Rx2+     | Receiver Non-Inverted Data Output.                                                   | 3B            |       |
| 23  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 24  | CML-O       | Rx4-     | Receiver Inverted Data Output.                                                       | 3B            |       |
| 25  | CML-O       | Rx4+     | Receiver Non-Inverted Data Output.                                                   | 3B            |       |
| 26  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 27  | LVTTTL-O    | ModPrsL  | Module Present.                                                                      | 3B            |       |
| 28  | LVTTTL-O    | IntL     | Interrupt.                                                                           | 3B            |       |
| 29  |             | VccTx    | +3.3V Transmitter Power Supply.                                                      | 2B            |       |
| 30  |             | Vcc1     | +3.3V Power Supply.                                                                  | 2B            |       |
| 31  | LVTTTL-I    | InitMode | Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE. | 3B            |       |
| 32  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 33  | CML-I       | Tx3+     | Transmitter Non-Inverted Data Input.                                                 | 3B            |       |
| 34  | CML-I       | Tx3-     | Transmitter Inverted Data Input.                                                     | 3B            |       |
| 35  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 36  | CML-I       | Tx1+     | Transmitter Non-Inverted Data Input.                                                 | 3B            |       |
| 37  | CML-I       | Tx1-     | Transmitter Inverted Data Input.                                                     | 3B            |       |
| 38  |             | GND      | Module Ground.                                                                       | 1B            |       |
| 39  |             | GND      | Module Ground.                                                                       | 1A            |       |
| 40  | CML-I       | Tx6-     | Transmitter Inverted Data Input.                                                     | 3A            |       |

|    |       |          |                                      |    |  |
|----|-------|----------|--------------------------------------|----|--|
| 41 | CML-I | Tx6+     | Transmitter Non-Inverted Data Input. | 3A |  |
| 42 |       | GND      | Module Ground.                       | 1A |  |
| 43 | CML-I | Tx8-     | Transmitter Inverted Data Input.     | 3A |  |
| 44 | CML-I | Tx8+     | Transmitter Non-Inverted Data Input. | 3A |  |
| 45 |       | GND      | Module Ground.                       | 1A |  |
| 46 |       | Reserved | For Future Use.                      | 3A |  |
| 47 |       | VS1      | Module Vendor-Specific 1.            | 3A |  |
| 48 |       | VccRx1   | +3.3V Receiver Power Supply.         | 2A |  |
| 49 |       | VS2      | Module Vendor-Specific 2.            | 3A |  |
| 50 |       | VS3      | Module Vendor-Specific 3.            | 3A |  |
| 51 |       | GND      | Module Ground.                       | 1A |  |
| 52 | CML-O | Rx7+     | Receiver Non-Inverted Data Output.   | 3A |  |
| 53 | CML-O | Rx7-     | Receiver Inverted Data Output.       | 3A |  |
| 54 |       | GND      | Module Ground.                       | 1A |  |
| 55 | CML-O | Rx5+     | Receiver Non-Inverted Data Output.   | 3A |  |
| 56 | CML-O | Rx5-     | Receiver Inverted Data Output.       | 3A |  |
| 57 |       | GND      | Module Ground.                       | 1A |  |
| 58 |       | GND      | Module Ground.                       | 1A |  |
| 59 | CML-O | Rx6-     | Receiver Inverted Data Output.       | 3A |  |
| 60 | CML-O | Rx6+     | Receiver Non-Inverted Data Output.   | 3A |  |
| 61 |       | GND      | Module Ground.                       | 1A |  |
| 62 | CML-O | Rx8-     | Receiver Inverted Data Output.       | 3A |  |
| 63 | CML-O | Rx8+     | Receiver Non-Inverted Data Output.   | 3A |  |
| 64 |       | GND      | Module Ground.                       | 1A |  |
| 65 |       | NC       | Not Connected.                       | 3A |  |
| 66 |       | Reserved | For Future Use.                      | 3A |  |
| 67 |       | VccTx1   | +3.3V Transmitter Power Supply.      | 2A |  |
| 68 |       | Vcc2     | +3.3V Power Supply.                  | 2A |  |
| 69 |       | Reserved | For Future Use.                      | 3A |  |
| 70 |       | GND      | Module Ground.                       | 1A |  |
| 71 | CML-I | Tx7+     | Transmitter Non-Inverted Data Input. | 3A |  |
| 72 | CML-I | Tx7-     | Transmitter Inverted Data Input.     | 3A |  |
| 73 |       | GND      | Module Ground.                       | 1A |  |
| 74 | CML-I | Tx5+     | Transmitter Non-Inverted Data Input. | 3A |  |
| 75 | CML-I | Tx5-     | Transmitter Inverted Data Input.     | 3A |  |
| 76 |       | GND      | Module Ground.                       | 1A |  |

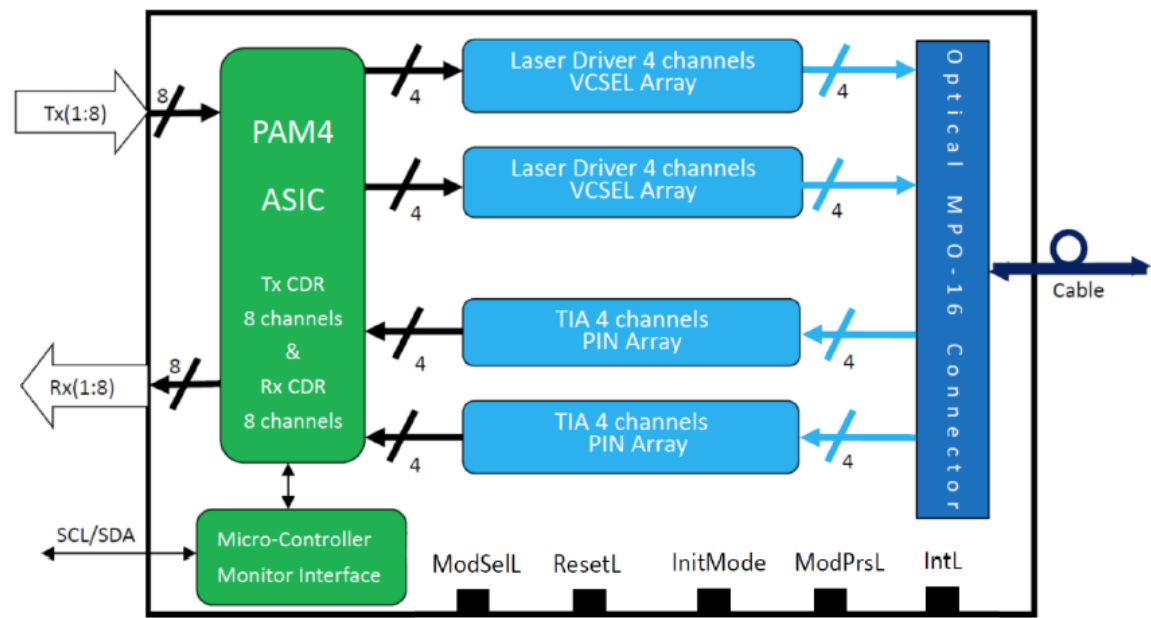
Electrical Pin-Out Details



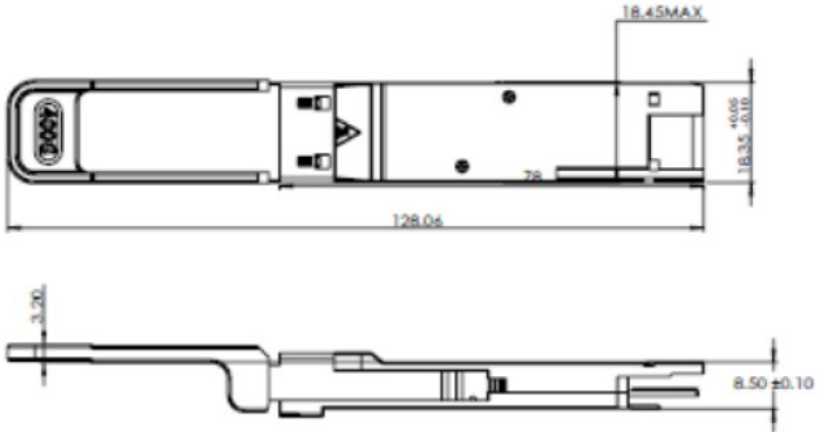
Recommended Power Supply Filter



Block Diagram



Mechanical Specifications





## **OptioConnect**

### **Innovation for the Future of High-Speed Networking**

#### **Who We Are**

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

#### **What We Do**

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

#### **Smarter Networks by Design**

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

#### **Our Team**

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

#### **Our Mission**

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

#### **Let's Connect**

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.

[www.optioconnect.com](http://www.optioconnect.com) | [info@optioconnect.com](mailto:info@optioconnect.com)

