QSFP112-400GB-SR4-50M-OPC

MSA and TAA 400GBase-SR4 QSFP112 Transceiver (MMF, 850nm, 50m, MPO, DOM, CMIS 5.0, Flat Top)

Features

- QSFP112 MSA Compliant
- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck
- Operating Temperature: 0 to 70 Celsius
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- MPO-12 APC Connector
- CMIS 5.0
- Class 1 Laser
- Hot Pluggable QSFP112 Form Factor
- RoHS Compliant and Lead-Free

Applications:

- 400GBase Ethernet

Product Description

This MSA compliant QSFP112 transceiver provides 400GBase-SR4 throughput up to 50m over multi-mode fiber (MMF) using a wavelength of 850nm via an MPO connector. It can operate at temperatures between 0 and 70C. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Tstg	-40		85	^{o}C	
Operating Case Temperature	Tc	0		70	^{o}C	
Relative Humidity (non-condensing)	RH	15		85	%	
Receiver Damage Threshold, per Lane	PRdmg	5			dBm	
Bit Rate	BR			425	Gbps	
Fiber Length on OM3 MMF				60	m	
Fiber Length on OM4 MMF				100	m	
I2C Clock Frequency		0	10	1000	kHz	

Notes:

1. Exceeding the Absolute Maximum Ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under Absolute Maximum Ratings will affect the reliability of the device.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Total Power Consumption	Pc			9	W	1
Supply Current per end				2.72	A	
Pre FEC Bit Error Ratio				2.4E-4		
Post FEC Bit Error Ratio				1E-12		
Transmitter (each lane)						
Differential pk-pk Input Voltage Tolerance		750			mV	
Differential Termination Mismatch				10	%	
Eye Height	EH	10			mV	
Common-Mode to Differential-Mode Return Loss	RLDc	IEEE802.3ck Equation (120G–1)			dB	
Vertical Eye Closure	VEC			12	dB	
Effective Return Loss	ERL	7.3			dB	
Transition Time		10			ps	
Receiver (each lane)						
Differential Data Output Swing		300		900	mVpp	
Differential Termination Mismatch				10	%	

Eye Height	EH	15			mV	
Vertical Eye Closure	VEC			12	dB	
Common-Mode to Differential-Mode Return Loss	RLDc	IEEE802.3ck Equation (120G–1)			dB	
Effective Return Loss	ERL	8.5			dB	
Transition Time		8.5			ps	

Notes:

1. Under condition of 3.465V operating supply voltage, and 70℃ case temperature.

Optical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter							
Data Rate per lane		DR		53.125		GBd	
Modulation Format				PAM4			
Center Wavelength		λ	844	850	863	nm	1
RMS Spectral Width		σ			0.6	nm	
Average Launch Power, each lane		Pavg	-4.6		4	dBm	
Optical Power OMA, each Lane， max		P_{OMA}	3.5			dBm	
OMAouter, each lane min	**max (TECQ, TDECQ) <1.8 dB**		max [-2.6 , max(TECQ,TECQ) – 4.4]			dBm	
	1.8 < max (TECQ, TDECQ) < 4.4 dB						
Transmitter and Dispersion Eye Closure (TDECQ), each lane		TDECQ			4.4	dB	
Transmitter Eye Closure for PAM4 (TECQ), each lane		TECQ			4.4	dB	
Extinction Ratio		ER	2.5			dB	
Transmitter Power Excursion, each lane					2.3	dBm	
Optical Return Loss Tolerance		ORLT			14	dB	
Optical Power for TX DISABLE					-30	dBm	
Encircled Fluxb				≥86% at 19 um ≤30% at 4.5 um			2
Receiver							
Data Rate per lane		BR		53.125		GBd	
Modulation Format				PAM4			
Center Wavelength		λ	844	850	863	nm	
Damage Threshold			5			dBm	
Average Receive Power, each Lane		AOP_R	–6.4		4	dBm	
Receive Power (OMAouter), each Lane		OMA_R			3.5	dBm	

Receiver Reflectance		RR			–15	dB	
Receiver Sensitivity, each Lane		S	RS = max (-4.6 , TECQ – 6.4)			dBm	3
Stressed Receiver Sensitivity, each Lane		SRS			-2.0	dBm	
RX LOS	**Assert**		-15			dBm	
	De-assert				-7.5	dBm	
	Hysteresis		0.5		5	dB	

Notes:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4.
3. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

QSFP-DD Rx Output Equalization Code Table

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host and Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Pin Descriptions

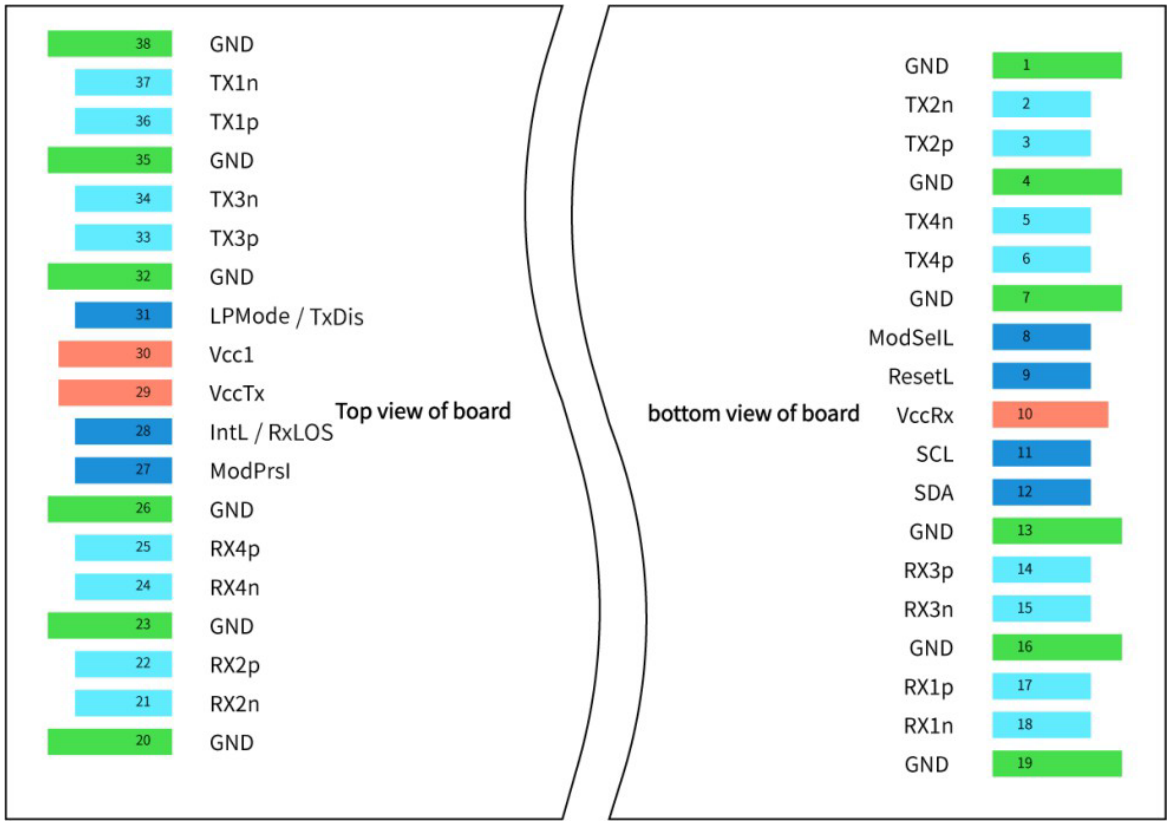
Pin	Logic	Symbol	Name/Description	Power Sequence	Notes
1		Ground	GND	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		Ground	GND	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		Ground	GND	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	

12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		Ground	GND	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		Ground	GND	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		Ground	GND	1B	1
20		Ground	GND	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		Ground	GND	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		Ground	GND	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		Ground	GND	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		Ground	GND	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		Ground	GND	1B	1

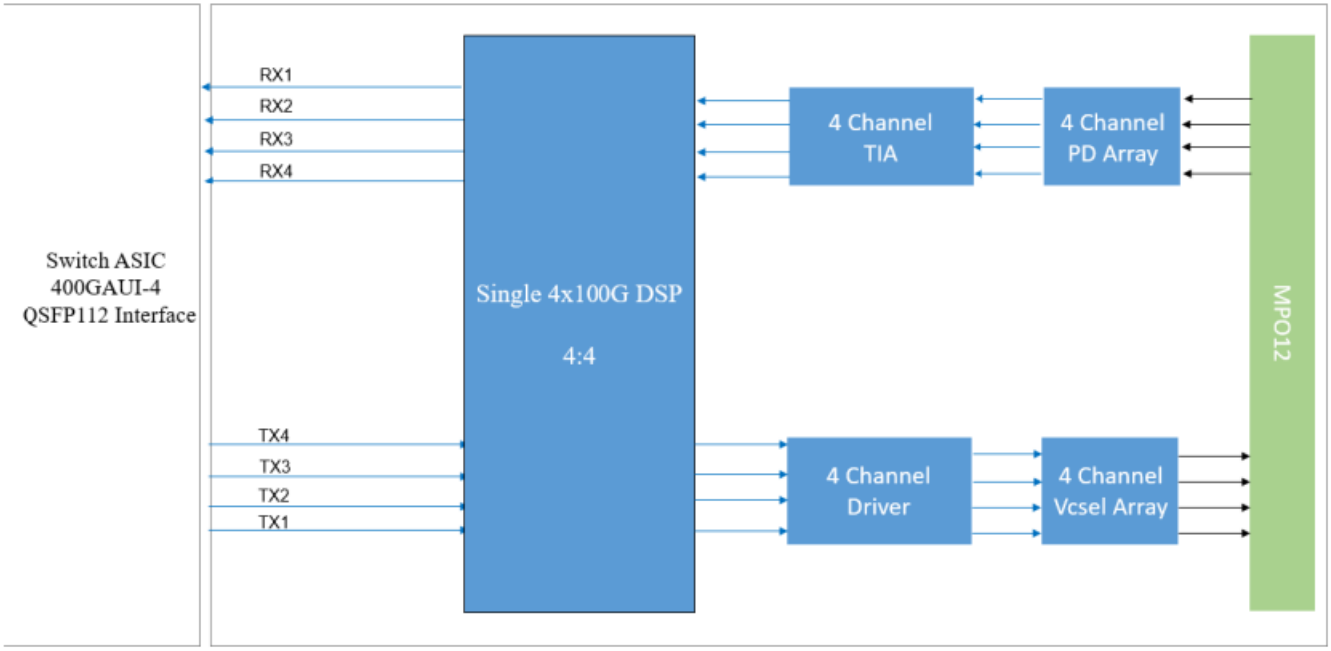
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1 and VccTx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

Electrical Pad Layout



Functional Block Diagram



Mechanical Specifications