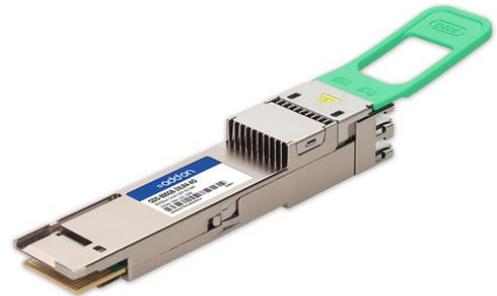


QDD-800GB-2XLR4-AO

MSA and TAA 800GBase-2xLR4 PAM4 QSFP-DD Transceiver (SMF, 1310nm, 10km, 2xLC, DOM, CMIS 5.0)

Features

- Compliant with IEEE 802.3-2022: 2x400GBASE-LR4 Optical Interface
- Dual LC Connector
- Compliant with IEEE 802.3ck-2002 2x400GAUI-4 C2M Electrical Interface
- 800 QSFP-DD MSA Compliant
- Class 1 Laser Safety Certified
- CMIS 5.0 Compliant
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius



Applications

- 2x400GBase Ethernet

Product Description

This MSA compliant QSFP-DD transceiver provides 800GBase-2xLR4 throughput up to 10km over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xLC connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T _{stg}	-40		85	°C	
Operating Case Temperature	T _c	0		70	°C	
Power Supply Voltage	V _{cc}	-0.5		3.6	V	
Relative Humidity (Non-Condensing)	RH	5		95	%	
Data Input Voltage Differential	V _{DIP} -V _{DIN}			1	V	
Control Input Voltage	V _i	-0.3		V _{cc} +0.5	V	
Control Output Current	I _o	-20		20	mA	
Signaling Speed Per Lane	DR		53.125		GBd	
Operating Distance		2		10000	m	MSA
		2		6000		IEEE

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V _{cc}	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	I _{cc_IP}			7600	mA	
Sustained Peak Current at Hot Plug	I _{cc_SP}			6270	mA	
Maximum Power Dissipation	PD			19	W	
Maximum Power Dissipation (Low-Power Mode)	PD _{LP}			2.5	W	
Control Input Voltage - High	V _{IH}	V _{cc} *0.7		V _{cc} +0.3	V	
Control Input Voltage - Low	V _{IL}	-0.3		V _{cc} *0.3	V	
2-Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise (1kHz to 1MHz, Pk-Pk)				66	mVp-p	
Transmitter (Module Input, TP1)						
Differential Pk-Pk Input Voltage Tolerance (TP1a)		750			mV	
Pk-Pk AC Common-Mode Voltage Tolerance	Low-Frequency (V _{CM_{LF}})	32			mV	
	Full-Band (V _{CM_{FB}})	80			mV	
Differential-Mode to Common-Mode Return Loss	RL _{cd}	802.3ck 120G-2			dB	
Effective Return Loss	ERL	8.5			dB	
Differential Termination Mismatch				10	%	
Single-Ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common-Mode Voltage Tolerance		-0.35		2.85	V	
Receiver (Module Output, TP4)						
Pk-Pk AC Common-Mode Voltage	Low-Frequency (V _{CM_{LF}})			32	mV	
	Full-Band (V _{CM_{FB}})			80	mV	
Differential Pk-Pk Output	Short-Mode			600	mV	

Voltage	Long-Mode				845	mV	
Eye Height		EH	15			mV	
Vertical Eye Closure		VEC			12	dB	
Common-Mode to Differential-Mode Return Loss		RLDc	802.3ck 120G-1			dB	
Effective Return Loss		ERL	8.5			dB	
Differential Termination Mismatch					10	%	
Transition Time			8.5			ps	
DC Common-Mode Voltage Tolerance			-0.35		2.85	V	

Electrical Low-Speed Control and Sense Signal Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Module Output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
InitMode, ResetL, and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	Vcc-0.5	Vcc+0.3	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Wavelength	L0, L4	λ C	1264.5	1271	1277.5	nm
	L1, L5		1284.5	1291	1297.5	
	L2, L6		1304.5	1311	1317.5	
	L3, L7		1324.5	1331	1337.5	
Side-Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOP _T			11.1	dBm	
Average Launch Power Per Lane	AOP _L	-2.7		5.1	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}) Per Lane	TDECQ < 1.4dB 1.4dB <= TDECQ <= TDECQ Maximum	OMA _{outer}	0.3		4.4	dBm
			-1.1 + TDECQ			
Difference in Launch Power Between any Two Lanes (OMA _{outer})	AOP _D			4	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane 10km	TDECQ			3.9	dB	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane 6km	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ) Per Lane 10km	TECQ			3.9	dB	

Transmitter Eye Closure for PAM4 (TECQ) Per Lane 6km		TECQ			3.4	dB	
TDECQ - TECQ					2.5	dB	
Over/Under-Shoot 10km					25	%	
Over/Under-Shoot 6km					22	%	
Pk-Pk Power 10km					5.2	dBm	
Transmitter Power Excursion 6m					2.5	dBm	
Average Launch Power of Off Transmitter Per Lane		T _{off}			-16	dBm	
Extinction Ratio		ER	3.5			dB	
Transmitter Transition Time		T _r			17	ps	
RIN _{15.6OMA}		RIN			-136	dB/Hz	
Optical Return Loss Tolerance		ORLT			15.6	dB	
Transmitter Reflectance		TR			-26	dB	2
Receiver							
Wavelength	L0, L4	λ _C	1264.5	1271	1277.5	nm	
	L1, L5		1284.5	1291	1297.5		
	L2, L6		1304.5	1311	1317.5		
	L3, L7		1324.5	1331	1337.5		
Damage Threshold Per Lane		AOP _D	6.1			dBm	
Average Receive Power Per Lane		AOP _R	-9		5.1	dBm	
Receive Power (OMA _{outer}) Per Lane		OMA _R			4.4	dBm	
Difference in Receive Power Between Any Two Lanes (OMA _{outer})		AOP _G			4.3	dB	
Receiver Reflectance		RR			-26	dB	
Receiver Sensitivity (OMA _{outer}) Per Lane	TECQ < 1.4dB	SOMA			-6.8	dBm	
	1.4dB <= TECQ <= 3.4dB				-8.2 + TECQ		
Stressed Receiver Sensitivity (OMA _{outer}) Per Lane 10km		SRS			-4.3	dBm	3
Stressed Receiver Sensitivity (OMA _{outer}) Per Lane 6km		SRS			-4.8	dBm	3
Conditions of Stressed Receiver Sensitivity Test							
Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test 10km		SECQ			3.9	dB	
Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test 6km					3.4	dB	
OMA _{outer} of Each Aggressor Lane					-0.4	dBm	

Notes:

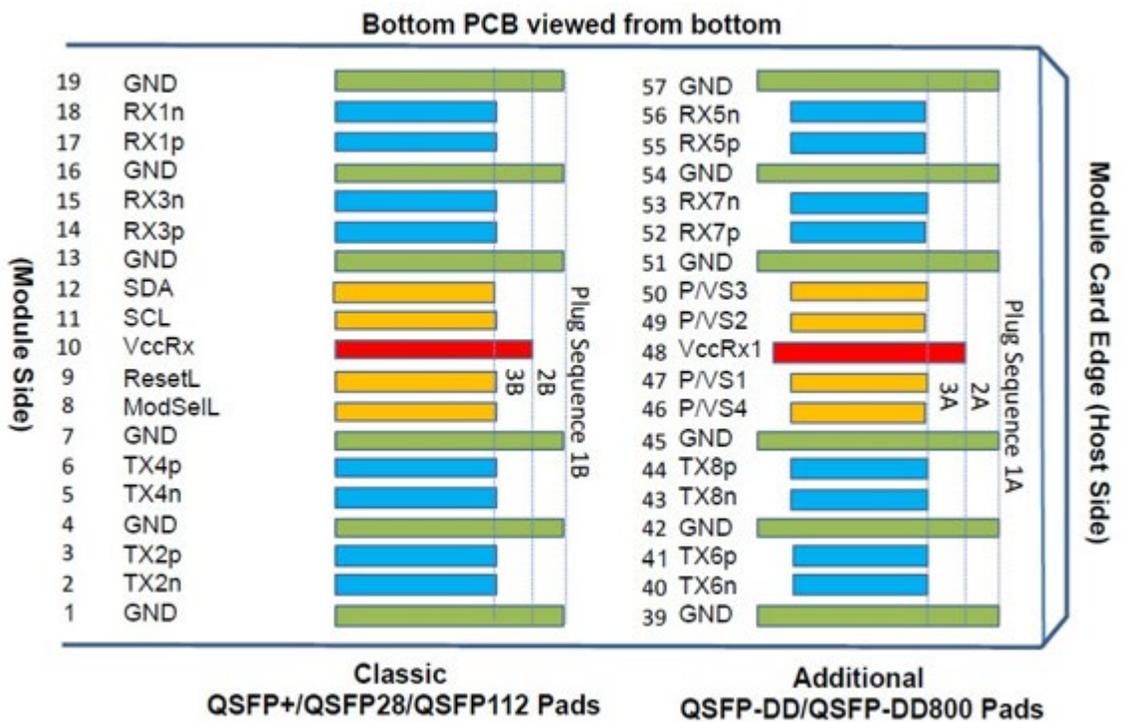
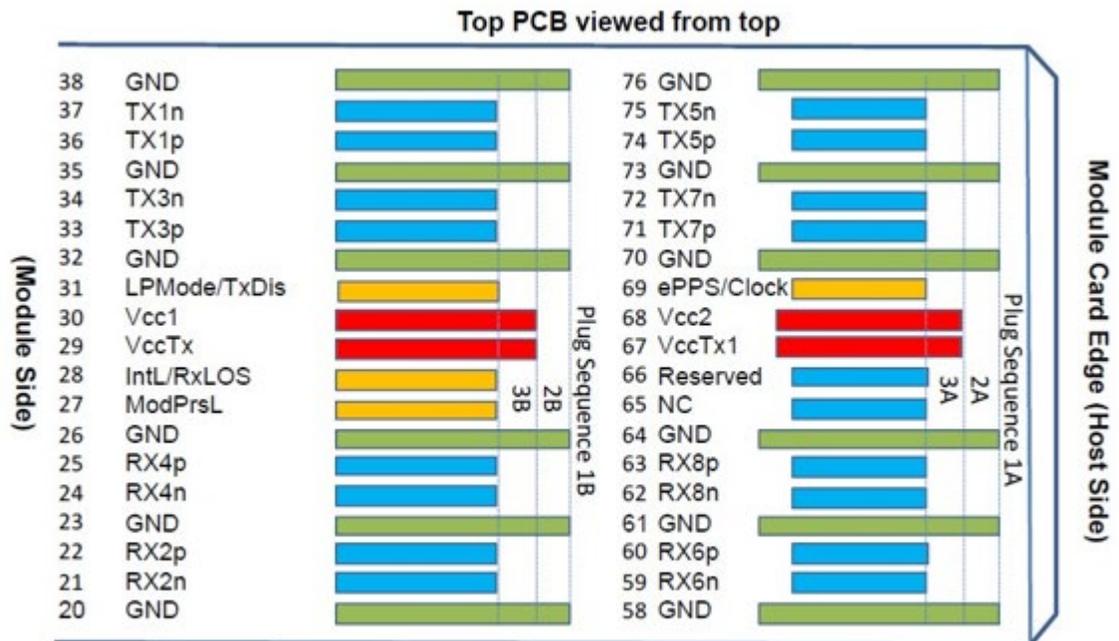
1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Measured with conformance test signal at TP3 for the BER = 2.4x10⁻⁴.

Pin Descriptions

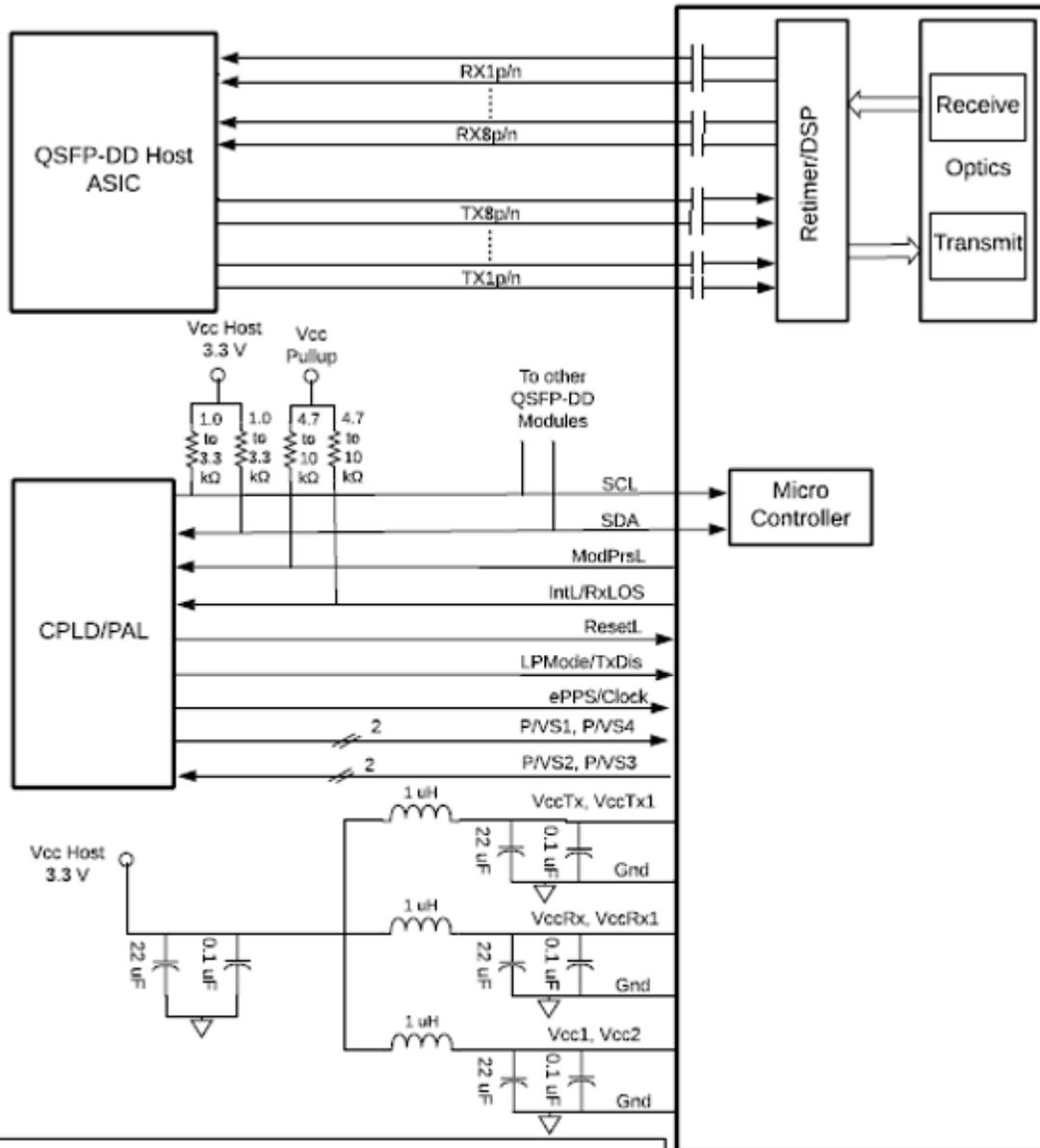
Pin	Symbol	Logic	Name/Description	Notes
1	GND		Module Ground.	
2	Tx2-	CML-I	Transmitter Inverted Data Input.	
3	Tx2+	CML-I	Transmitter Non-Inverted Data Input.	
4	GND		Module Ground.	
5	Tx4-	CML-I	Transmitter Inverted Data Input.	
6	Tx4+	CML-I	Transmitter Non-Inverted Data Input.	
7	GND		Module Ground.	
8	ModSelL	LVTTTL-I	Module Select.	
9	ResetL	LVTTTL-I	Module Reset.	
10	VccRx		+3.3V Receiver Power Supply.	
11	SCL	LVC MOS-I/O	2-Wire Serial Interface Clock.	
12	SDA	LVC MOS-I/O	2-Wire Serial Interface Data.	
13	GND		Module Ground.	
14	Rx3+	CML-O	Receiver Non-Inverted Data Output.	
15	Rx3-	CML-O	Receiver Inverted Data Output.	
16	GND		Module Ground.	
17	Rx1+	CML-O	Receiver Non-Inverted Data Output.	
18	Rx1-	CML-O	Receiver Inverted Data Output.	
19	GND		Module Ground.	
20	GND		Module Ground.	
21	Rx2-	CML-O	Receiver Inverted Data Output.	
22	Rx2+	CML-O	Receiver Non-Inverted Data Output.	
23	GND		Module Ground.	
24	Rx4-	CML-O	Receiver Inverted Data Output.	
25	Rx4+	CML-O	Receiver Non-Inverted Data Output.	
26	GND		Module Ground.	
27	ModPrsL	LVTTTL-O	Module Present.	
28	IntL/RxLOS	LVTTTL-O	Interrupt. Optionally RxLOS.	
29	VccTx		+3.3V Transmitter Power Supply.	
30	Vcc1		+3.3V Power Supply.	
31	LPMoDe/TxDis	LVTTTL-I	Low-Power Mode. Optionally Tx_Disable	
32	GND		Module Ground.	
33	Tx3+	CML-I	Transmitter Non-Inverted Data Input.	
34	Tx3-	CML-I	Transmitter Inverted Data Input.	
35	GND		Module Ground.	
36	Tx1+	CML-I	Transmitter Non-Inverted Data Input.	
37	Tx1-	CML-I	Transmitter Inverted Data Input.	
38	GND		Module Ground.	
39	GND		Module Ground.	
40	Tx6-	CML-I	Transmitter Inverted Data Input.	
41	Tx6+	CML-I	Transmitter Non-Inverted Data Input.	

42	GND		Module Ground.	
43	Tx8-	CML-I	Transmitter Inverted Data Input.	
44	Tx8+	CML-I	Transmitter Non-Inverted Data Input.	
45	GND		Module Ground.	
46	P/VS4	LVC MOS/CML-I	Programmable. Module Vendor-Specific 4.	
47	P/VS1	LVC MOS/CML-I	Programmable. Module Vendor-Specific 1.	
48	VccRx1		+3.3V Receiver Power Supply.	
49	P/VS2	LVC MOS/CML-O	Programmable. Module Vendor-Specific 2.	
50	P/VS3	LVC MOS/CML-O	Programmable. Module Vendor-Specific 3.	
51	GND		Module Ground.	
52	Rx7+	CML-O	Receiver Non-Inverted Data Output.	
53	Rx7-	CML-O	Receiver Inverted Data Output.	
54	GND		Module Ground.	
55	Rx5+	CML-O	Receiver Non-Inverted Data Output.	
56	Rx5-	CML-O	Receiver Inverted Data Output.	
57	GND		Module Ground.	
58	GND		Module Ground.	
59	Rx6-	CML-O	Receiver Inverted Data Output.	
60	Rx6+	CML-O	Receiver Non-Inverted Data Output.	
61	GND		Module Ground.	
62	Rx8-	CML-O	Receiver Inverted Data Output.	
63	Rx8+	CML-O	Receiver Non-Inverted Data Output.	
64	GND		Module Ground.	
65	NC		Not Connected.	
66	Reserved			
67	VccTx1		+3.3V Power Supply.	
68	Vcc2		+3.3V Power Supply.	
69	ePPS/Clock	LVC MOS-I	1PPS PTP Clock or Reference Clock Input.	
70	GND		Module Ground.	
71	Tx7+	CML-I	Transmitter Non-Inverted Data Input.	
72	Tx7-	CML-I	Transmitter Inverted Data Input.	
73	GND		Module Ground.	
74	Tx5+	CML-I	Transmitter Non-Inverted Data Input.	
75	Tx5-	CML-I	Transmitter Inverted Data Input.	
76	GND		Module Ground.	

Electrical Pad Layout



Recommended Host Board Schematic

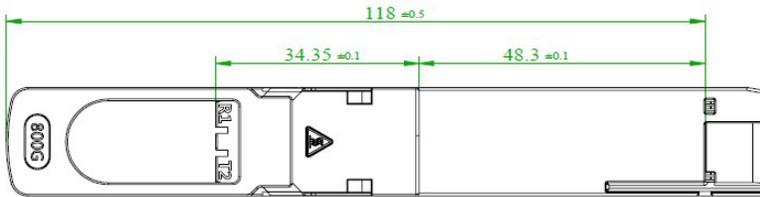
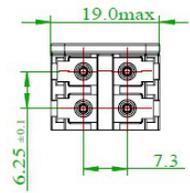
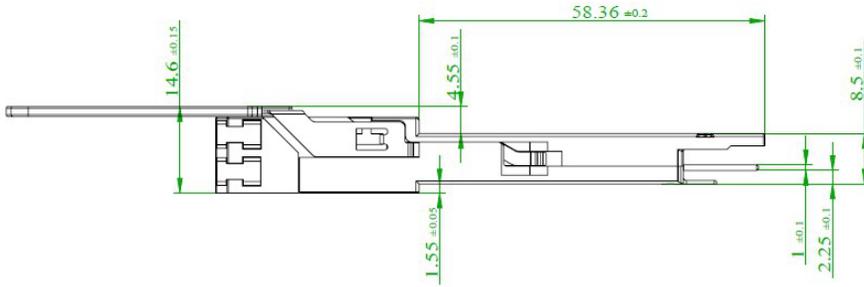
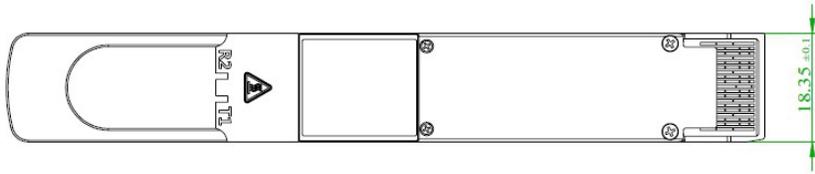


Note: Filter capacitors values are informative and application dependent, 0.1 μF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

**QSFDP-DD/QSFDP-DD800
Optical Module**

Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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