QDD-400G-DCO-ULH-AO

MSA and TAA 400GBase-Open ULH Coherent QSFP-DD Transceiver (SMF, 1528.77nm to 1567.13nm, 2400km, LC, DOM)

Features

- Hot-Pluggable QSFP-DD Footprint (Type 2B)
- Supports 400/200/100Gbps
- Duplex LC Connector
- Tunable C-Band Transmitter
- Single 3.3V Power Supply
- Coherent Receivers
- High Output Power: -10dBm to 1dBm, Adjustable at C-Band
- EDFA and VOA Inside
- RoHS Complaint and Lead-Free
- Operating Temperature: 0 to 70 Celsius

Applications

- 400GBase Ethernet

Product Description

This MSA compliant QSFP-DD transceiver provides 400GBase-Open ULH throughput up to 120km over single-mode fiber (SMF) using a wavelength of 1528.77nm to 1567.13nm via an LC connector. It can operate at temperatures between 0 and 75C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Rev. 040226

Absolute Maximum Ratings

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature		Tstg	-40		85	°C	
Operating Case Temperature		Tc	0		75	°C	
Maximum Power Supply Voltage		Vcc	-0.3	3.3	3.6	V	
Relative Humidity (Non-Condensing)		RH	5		85	%	
Receiver Damage Threshold		PRdmg	13			dBm	Optical Power
ESD Sensitivity (All Pins)					1000	V	HBM Conditions
Client Mode			1 x 400GAUI-8				
			2 x 200GAUI-4				
			4 x 100GAUI-2				
Transmission Distance (DWDM Amplified)	**400G ULH**				2400	km	DWDN System Dependent
Modulation Format			100G 118GB QPSK				OFEC FEC
Baud Rate		GBd	118.2 +/- 20ppm				

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
	Icc			9.0	A	
Maximum Sustained Peak Current (<500ms)				9.9	A	
Maximum Instantaneous Peak Current (<50µs)				12.0	A	
Power Consumption	PC			29.5	W	
Power Supply Noise	Vrip			1	%	DC-1MHz
				2	%	1-10MHz
Low-Speed						
SCL and SDA	VOL	0		0.4	V	IOL(max.)=3mA for fast-mode, 20mA for fast-mode plus.
	VOH	Vcc-0.5		Vcc+0.3	V	
SCL and SDA	VIL	-0.3		Vcc*0.3	V	
	VIH	Vcc*0.7		Vcc+0.5	V	
Capacitance for SCL and SDA I/O Signal	Ci			14	pF	Capacitance of SCL and SDA in this specification are higher than I^2C bus specification to account for connector and trace capacitances.
Total Bus Capacitive Load for SCL and SDA	Cb			400	pF	Maximum bus capacitance for fast-mode (400kHz).
				550	pF	Maximum bus capacitance for fast-mode+ (1MHz).
LPMode/TxDis, ResetL, and ModSelL	VIL	-0.3		0.8	V	
	VIH	2		Vcc+0.3	V	
	|Iin|			360	uA	0V<VIN<Vcc

IntL	VOL	0		0.4	V	IOL=2.0mA
	VOH	Vcc-0.5		Vcc+0.3	V	10kΩ pull-up to Host_Vcc
ModPrsL	VOL	0		0.4	V	IOL=2.0mA
	VOH					ModPrsL can be implemented as a short-circuit to GND on the module.

Time/Power Monitor Requirements

Parameter	Symbol	Min.	Max.	Unit	Notes
Transmitter Disable Time	ms	1	100	ms	Time from setting OutputDisableTx bit until the transmitter optical output falls below the Tx disabled output power. The transmitter remains tuned and ready for fast enable. Rx shall remain locked and thus LO must remain enabled.
Transmitter Turn-Up Time: Warm Start	s		180	s	The maximum time from ModuleLowPwr to DataPathActivated state.
Transmitter Turn-Up Time: Cold Start	s		200	s	The maximum time from de-assertion of ResetS to DataPathActivated state.
Transmitter Wavelength Switching Time	s		60	s	The maximum time to change transmitter wavelength including the turn-up time.
Receiver Acquisition Time	s		10	s	Time to fully acquire signal after Rx_LOS de-assert with Data Path already in the DataPathActivated state. Valid 800ZR optical Rx input signal present.
Receiver Turn-Up Time: Cold Start	s		200	s	Time to fully acquire signal after module reset. Valid 800ZR optical Rx input signal present.
Service Recovery Time	ms		40	s	From Rx_LOS de-assert to valid host-side output signal.
Input Total Power Monitor Accuracy	dB	-2	2	dB	
Input Channel Power Monitor Accuracy	dB	-2	2	dB	

Control and I/O Timing Characteristics

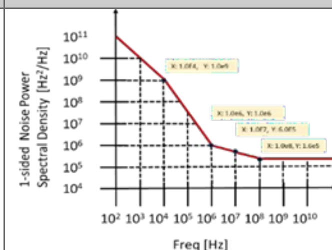
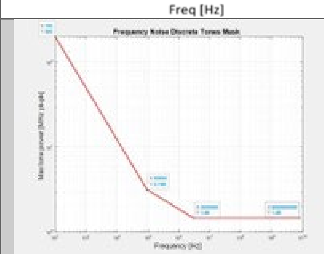
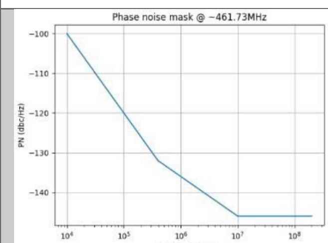
Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInitDuration	Max. MgmtInit Duration		2000	ms	Time from power on, hot plug, or rising edge of reset until the high-to-low SDA transition of the Start condition for the first acknowledged TWI Transaction. Note 1.
ResetL Assert Time	t_reset_init	10		us	Minimum pulse time on the ResetL signal to initiate a module reset.
Int/RxLOS Mode Change	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual- mode signal IntL/RxLOSL.
LPMode/TxDis Mode Change Time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of LPMode/TxDis.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until VOUT:IntL=VOL.
IntL De-Assert Time	toff_IntL		500	us	Time from clear on read operation of associated flag until VOUT:IntL=VOH. This includes de-assert times for RxLOS, TxFault, and other flag bits. Note 2.
RxLOS Assert Time	ton_los		100	ms	Time from RxLOS condition present to RxLOS bit set (value = 1b) and IntL asserted. Note 3.
RxLOS Assert Time (Optional Fast-Mode)	ton_losf		1	ms	Time from RxLOS state to RxLOS bit set (value = 1b) and IntL asserted. Note 3.

RxLOS De-Assert Time	toff_los		100	ms	Time from optical signal above the LOS de-assert threshold to when the module releases the RxLOSL signal to high.
RxLOS Assert Time (Optional Fast-Mode)	toff_f_LOS		3	ms	Optional fast-mode is advertised via the CMIS.
TxDisable Assert Time	ton_txdis		100	ms	Time from the stop condition of the TxDisable write sequence 1 until optical output falls below 10% of nominal.
TxDisable Assert Time (Optional Fast-Mode)	ton_txdisf		3	ms	Optional fast-mode is advertised via CMIS. Time from TxDisable signal "high" to the optical output reaching the disabled level.
TxDisable De-Assert Time	toff_txdis		400	ms	Time from TxDisable bit cleared to 1 until optical output rises above 90% of nominal. Note 4.
TxDisable De-Assert Time (Optional Fast-Mode)	toff_txdisf		10	ms	Time from TxDisable bit cleared to 1 until optical output rises above 90% of nominal.
TxFault Assert Time	ton_Txfault		200	ms	Time from TxFault state to TxFault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) until associated IntL assertion is inhibited. Note 5.
Mask De-Assert Time	toff_mask		100	ms	Time from mask bit set (value=1b) until associated IntL operation resumes. Note 5.
RxSquelch Assert Time	ton_Rxsq		15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
RxOutput Disable Assert Time	ton_rxdis		100	ms	Time from Rx Output Disable bit set (value = 1b) until Rx output falls below 10% of nominal.
RxOutput Disable De-Assert Time	toff_rxdis		100	ms	Time from Rx Output Disable bit cleared (value = 0b) until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis		100	ms	This applies to RxSquelch and is the time from bit set (value = 0b) until squelch functionality is disabled.
Squelch Disable De-Assert Time	toff_sqdis		100	ms	This applies to RxSquelch and is the time from bit cleared (value = 0b) until squelch functionality is enabled.

Notes:

1. "Power on" is defined as the instant when supply voltages reach and remain at or above the minimum level.
2. Measured from low-to-high SDA edge of the "stop" condition of the read transaction.
3. RxLOS condition is defined at the optical input by the relevant standard. LOS, TxFault, and other flag bits.
4. TxSquelch de-assert time is longer than SFF-8679.
5. Measured from low-to-high SDA edge of the "stop" condition of the write transaction.

Optical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Notes
Transmitter					
Transmitter Frequency Range	191.3		196.1	THz	
Flexible DWDM Grid	3.125			GHz	
Frequency Fine Tuning Step	0.1			GHz	
Laser Frequency Accuracy	-1.8		1.8	GHz	
Laser Linewidth			300	kHz	Tx and LO
Laser Frequency Noise			See Mask	Hz2/Hz	
Laser Frequency Noise - Discrete Tone Amplitude			See Mask	MHz	
Laser RIN			-145	dB/Hz	0.2GHz≤f≤10GHz Average
			-140		0.2GHz≤f≤10GHz Peak
Tx Clock Phase Noise (PN): Maximum PN Mask			See Mask	dBc/Hz	
Tx Output Power at ProgOutputPowerMax	0			dBm	Transmit output power over wavelength, temperature, and aging.
Minimum Provisionable Range of Transmit Output Power	-10		1	dBm	
Default Transmit Output Power		+0.5		dBm	
Total Output Power with Tx Disabled			-35	dBm	OutputDisableTx = true.
Total Output Power During Wavelength Switching			-35	dBm	Applicable to modules with tunable optics.
Transmit Output Power Stability	-0.5		0.5	dB	Output short-term power stability when operating at a fixed wavelength and temperature. Measurement condition: 1ms averaging time for 1-minute accumulation.
Optical Power Setting Accuracy	-1		1	dB	Difference between setting and reporting.
Output Power Monitor Accuracy	-1		1	dB	
Transmit Output Power Adjust Step	0.1			dB	
In-Band (IB) OSNR	37			dB/12.5GHz	In-band OSNR is defined as the Tx signal power between the -20dB Tx Spectral Mask frequency points,

					referenced to an optical noise bandwidth of 12.5 GHz (0.1nm @ 193.7THz) at the Tx signal peak frequency.
Out-of-Band (OOB) OSNR	27			dB/12.5GHz	Out-of-Band OSNR is defined as the Tx signal power between the -20dB Tx Spectral Mask frequency points, referenced to the maximum optical noise power within any optical bandwidth of 12.5GHz (0.1nm @ 193.7THz) outside of the -20dB Tx Spectral Mask.
Transmitter Reflectance			-20	dB	Looking into the Tx.
Transmitter Back Reflection Tolerance			-24	dB	Light reflected relative to Tx output power back to transmitter while still meeting Tx optical performance requirements.
Transmitter Polarization-Dependent Power			1.5	dB	
X-Y Skew			5	ps	
DC I-Q Offset (Mean Per Polarization)			-26	dB	$P_{excess} = \frac{\mathrm{I}_{\mathrm{mean}}^2 + \mathrm{Q}_{\mathrm{mean}}^2}{\mathrm{P}_{\mathrm{Signal}}}$ $IQ_{\mathrm{offset}} = 10 \log_{10} (\mathrm{P}_{\mathrm{excess}})$
I-Q Instantaneous Offset			-20	dB	Same formula definition as DC I-Q offset; however, any averaging period shall be <1us to be consistent with the timescales of Rx DSP operations. Specification applies at any point in time. Allows for modulator bias controls/errors.
Mean I-Q Amplitude Imbalance			1	dB	
I-Q Phase Error	-5		5	deg	
I-Q Skew			0.75	ps	
Receiver					
Frequency Offset Between Received Carrier and LO	-3.6		3.6	GHz	Acquisition range.
Input Power Range	-12		0	dBm	Signal power of the channel for the OSNR tolerance defined.
Input Power Damage Threshold	13			dBm	Instantaneous balanced dual polarization signal.
Input Power Range (Single Wavelength Unamplified)	-25		0	dBm	Rx OSNR > 35dB, 193.7THz
OSNR Tolerance			17.8	dB/12.5GHz	The OSNR tolerance is referenced to an optical bandwidth of 12.5GHz (0.1nm @ 193.7THz). Measured back-to-back with short optical channel.
Maximum FEC Pre-BER			0.020		
Optical Return Loss	20			dB	Optical reflectance at Rx connector input.
Chromatic Dispersion (CD) Tolerance	48000			ps/nm	Tolerance to chromatic dispersion.
CD OSNR Tolerance Penalty			0.5	dB	OSNR tolerance penalty over OSNR Tolerance due to chromatic dispersion.
PMD Tolerance (DGD, SOPMD)	30			ps	Tolerance to PMD with ≤0.5dB penalty against OSNR tolerance when change in SOP is ≤1krad/s.

					10ps of average PMD (DGD, SOPMD) corresponds to: 33ps of DGDmax when SOPMD = 0ps2 272 ps2 of SOPMD when DGDmax = 23.3 ps. Due to the statistical nature of PMD the DGDmax to DGDmean ratio is calculated at 3.3 (4.1×10^{-6} probability that instantaneous DGD exceeds DGDmax).
Peak PDL Tolerance	3.5			dB	Tolerance to peak PDL with ≤1.8dB penalty to OSNR tolerance when change in SOP is ≤1krad/s. Test configuration: PDL emulator applied before noise loading.
Tolerance to Change in SOP	50			krad/s	Tolerance to change in SOP with ≤0.5dB additional OSNR penalty over all PMD and PDL values.
Optical Input Power Transient Tolerance	-2		2	dB	Tolerance to change in input power with ≤0.5dB penalty to OSNR tolerance. Received power during transient shall be within the range defined by input power range. OSNR penalty is referenced against the steady state required OSNR tolerance at the minimum power of the input transient. The 20-80% rise/fall times for the input power change shall be no faster than 50 microseconds, equivalent to a ≤24mdB/ms maximum slew rate.
Adjacent Channel Crosstalk OSNR Tolerance Penalty	DWDM system-dependent			dB	OSNR tolerance penalty due to crosstalk interference from neighboring channels. Back-to-back through the reference mux/demux filters specified. Neighboring channels conforming to the worst-case Tx Spectral Mask. Neighboring channels having +3dB higher Tx output power relative to the channel under measurement and at worst-case frequency offsets.
Intra-Channel Filtering Penalty	DWDM system-dependent			dB	Due to filtering effects with the reference 150GHz mux/demux filters specified.

Pin Descriptions

Pin	Symbol	Logic	Name/Description	Plug Sequence	Notes
1	GND		Module Ground.	1B	1
2	Tx2-	CML-I	Transmitter Inverted Data Input.	3B	
3	Tx2+	CML-I	Transmitter Non-Inverted Data Input.	3B	
4	GND		Module Ground.	1B	1
5	Tx4-	CML-I	Transmitter Inverted Data Input.	3B	
6	Tx4+	CML-I	Transmitter Non-Inverted Data Input.	3B	
7	GND		Module Ground.	1B	1
8	ModSelL	LVTTL-I	Module Select.	3B	
9	ResetL	LVTTL-I	Module Reset.	3B	
10	VccRx		+3.3V Receiver Power Supply.	2B	2
11	SCL	LVCMOS-I/O	2-Wire Serial Interface Clock.	3B	
12	SDA	LVCMOS-I/O	2-Wire Serial Interface Data.	3B	
13	GND		Module Ground.	1B	1
14	Rx3+	CML-O	Receiver Non-Inverted Data Output.	3B	
15	Rx3-	CML-O	Receiver Inverted Data Output.	3B	
16	GND		Module Ground.	1B	1
17	Rx1+	CML-O	Receiver Non-Inverted Data Output.	3B	
18	Rx1-	CML-O	Receiver Inverted Data Output.	3B	
19	GND		Module Ground.	1B	1
20	GND		Module Ground.	1B	1
21	Rx2-	CML-O	Receiver Inverted Data Output.	3B	
22	Rx2+	CML-O	Receiver Non-Inverted Data Output.	3B	
23	GND		Module Ground.	1B	1
24	Rx4-	CML-O	Receiver Inverted Data Output.	3B	
25	Rx4+	CML-O	Receiver Non-Inverted Data Output.	3B	
26	GND		Module Ground.	1B	1
27	ModPrsL	LVTTL-O	Module Present.	3B	
28	IntL/RxLOS	LVTTL-O	Interrupt. Optionally RxLOS.	3B	
29	VccTx		+3.3V Transmitter Power Supply.	2B	2
30	Vcc1		+3.3V Power Supply.	2B	2
31	LPMode/TxDis	LVTTL-I	Low-Power Mode. Optionally TxDis.	3B	
32	GND		Module Ground.	1B	1
33	Tx3+	CML-I	Transmitter Non-Inverted Data Input.	3B	
34	Tx3-	CML-I	Transmitter Inverted Data Input.	3B	
35	GND		Module Ground.	1B	1
36	Tx1+	CML-I	Transmitter Non-Inverted Data Input.	3B	
37	Tx1-	CML-I	Transmitter Inverted Data Input.	3B	
38	GND		Module Ground.	1B	1
39	GND		Module Ground.	1A	1
40	Tx6-	CML-I	Transmitter Inverted Data Input.	3A	
41	Tx6+	CML-I	Transmitter Non-Inverted Data Input.	3A	
42	GND		Module Ground.	1A	1
43	Tx8-	CML-I	Transmitter Inverted Data Input.	3A	
44	Tx8+	CML-I	Transmitter Non-Inverted Data Input.	3A	

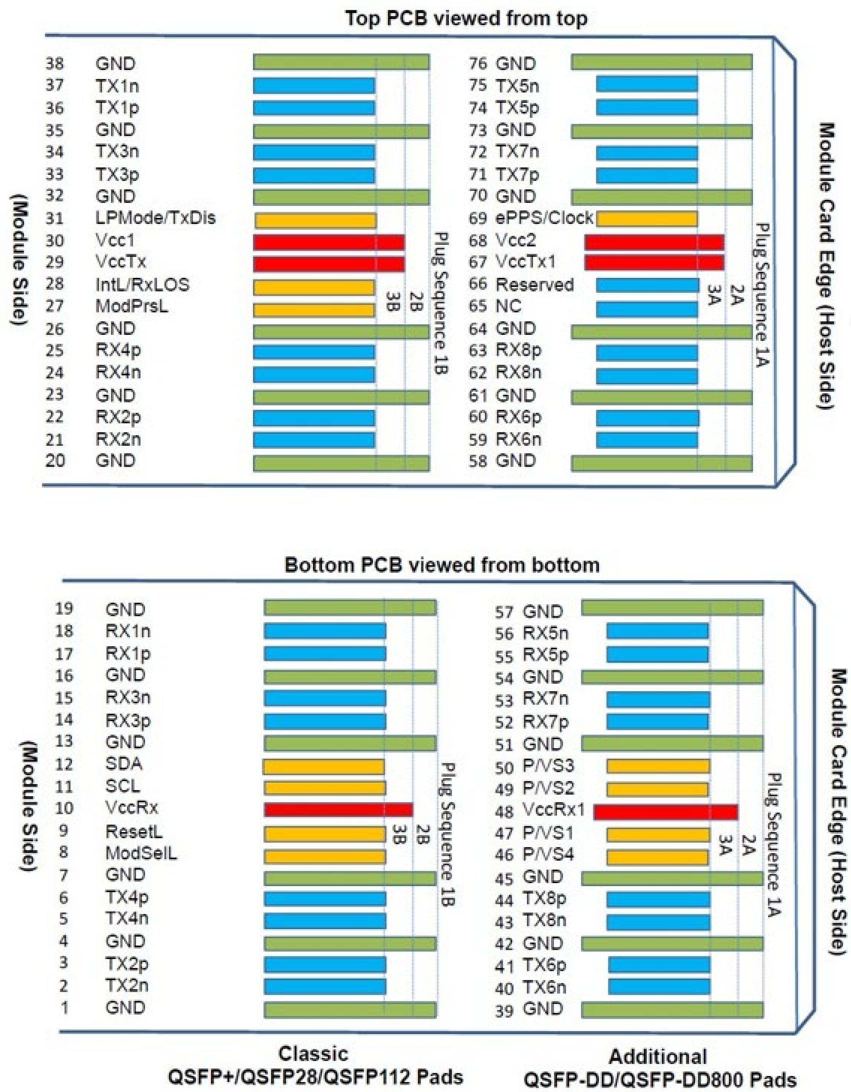
45	GND		Module Ground.	1A	1
46	P/VS4	LVCMOS/CML-I	Programmable. Module Vendor-Specific 4.	3A	5
47	P/VS1	LVCMOS/CML-I	Programmable. Module Vendor-Specific 1.	3A	5
48	VccRx1		+3.3V Receiver Power Supply.	2A	2
49	P/VS2	LVCMOS/CML-O	Programmable. Module Vendor-Specific 2.	3A	5
50	P/VS3	LVCMOS/CML-O	Programmable. Module Vendor-Specific 3.	3A	5
51	GND		Module Ground.	1A	1
52	Rx7+	CML-O	Receiver Non-Inverted Data Output.	3A	
53	Rx7-	CML-O	Receiver Inverted Data Output.	3A	
54	GND		Module Ground.	1A	1
55	Rx5+	CML-O	Receiver Non-Inverted Data Output.	3A	
56	Rx5-	CML-O	Receiver Inverted Data Output.	3A	
57	GND		Module Ground.	1A	1
58	GND		Module Ground.	1A	1
59	Rx6-	CML-O	Receiver Inverted Data Output.	3A	
60	Rx6+	CML-O	Receiver Non-Inverted Data Output.	3A	
61	GND		Module Ground.	1A	1
62	Rx8-	CML-O	Receiver Inverted Data Output.	3A	
63	Rx8+	CML-O	Receiver Non-Inverted Data Output.	3A	
64	GND		Module Ground.	1A	1
65	NC		Not Connected.	3A	3
66	Reserved		For Future Use.	3A	3
67	VccTx1		+3.3V Power Supply.	2A	2
68	Vcc2		+3.3V Power Supply.	2A	2
69	ePPS/Clock	LVCMOS-I	1PPS PTP Clock or Reference Clock Input.	3A	6
70	GND		Module Ground.	1A	1
71	Tx7+	CML-I	Transmitter Non-Inverted Data Input.	3A	
72	Tx7-	CML-I	Transmitter Inverted Data Input.	3A	
73	GND		Module Ground.	1A	1
74	Tx5+	CML-I	Transmitter Non-Inverted Data Input.	3A	
75	Tx5-	CML-I	Transmitter Inverted Data Input.	3A	
76	GND		Module Ground.	1A	1

Notes:

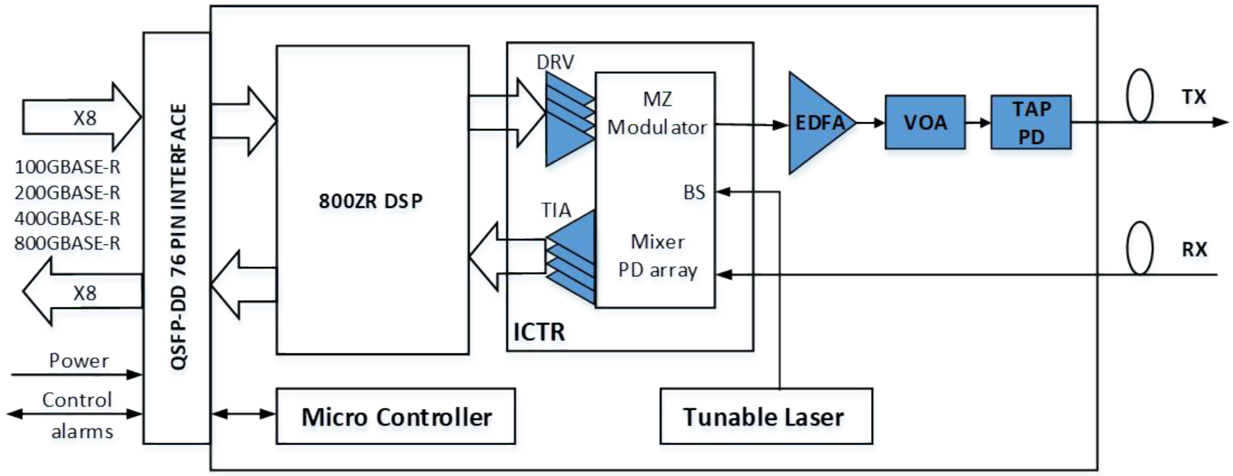
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane. Each connector GND contact is rated for a steady state current of 500mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500mA.
3. Reserved pad recommended to be terminated with 10kΩ to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module, optionally pad 65 may get terminated with 10kΩ to ground on the host.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break, contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
5. Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor-specific inputs P/VS1 and P/VS4 signals, it is recommended that each be terminated in the module with 10kΩ. For host designs using programmable/vendor-specific outputs P/VS2 and P/VS3 signals, it is recommended each to be terminated on the host with 10kΩ.
6. For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

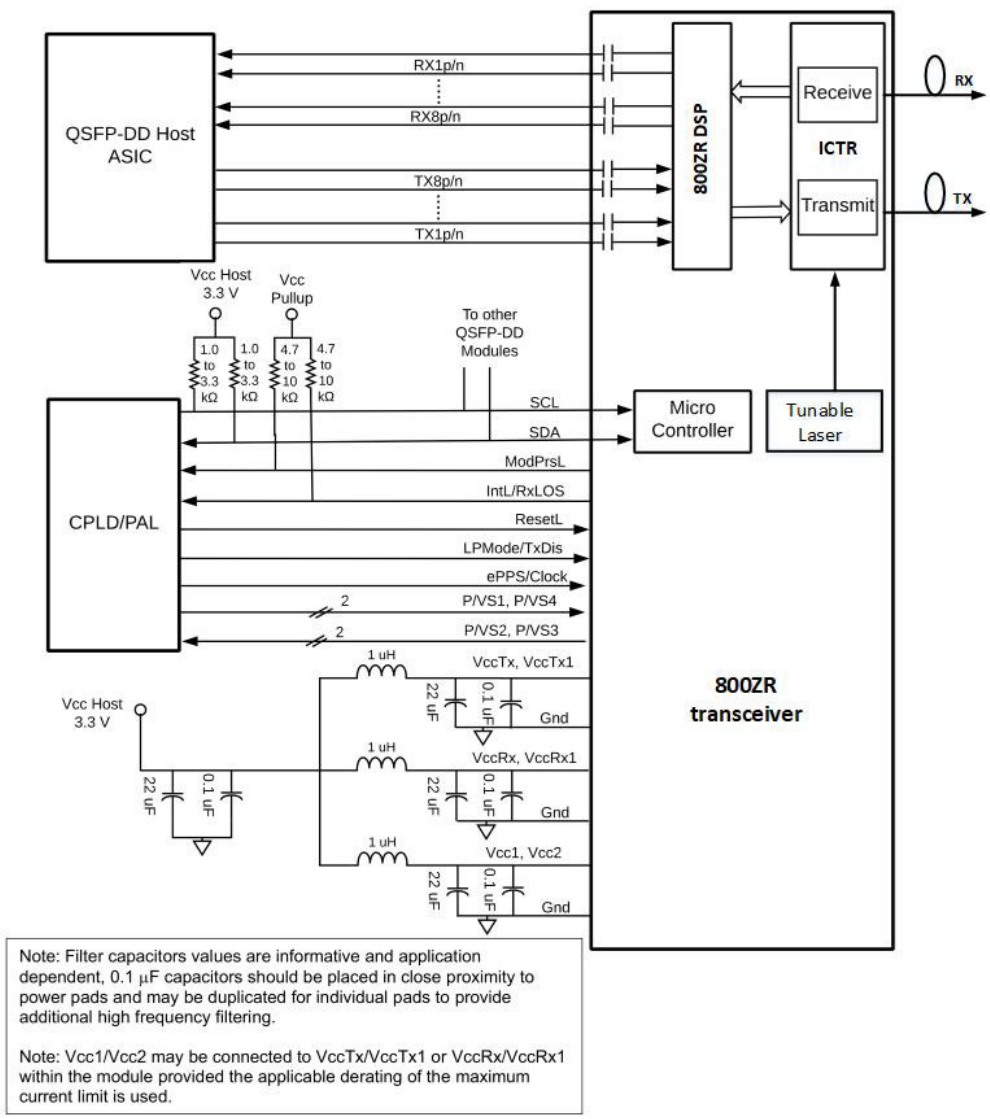
Electrical Pad Layout



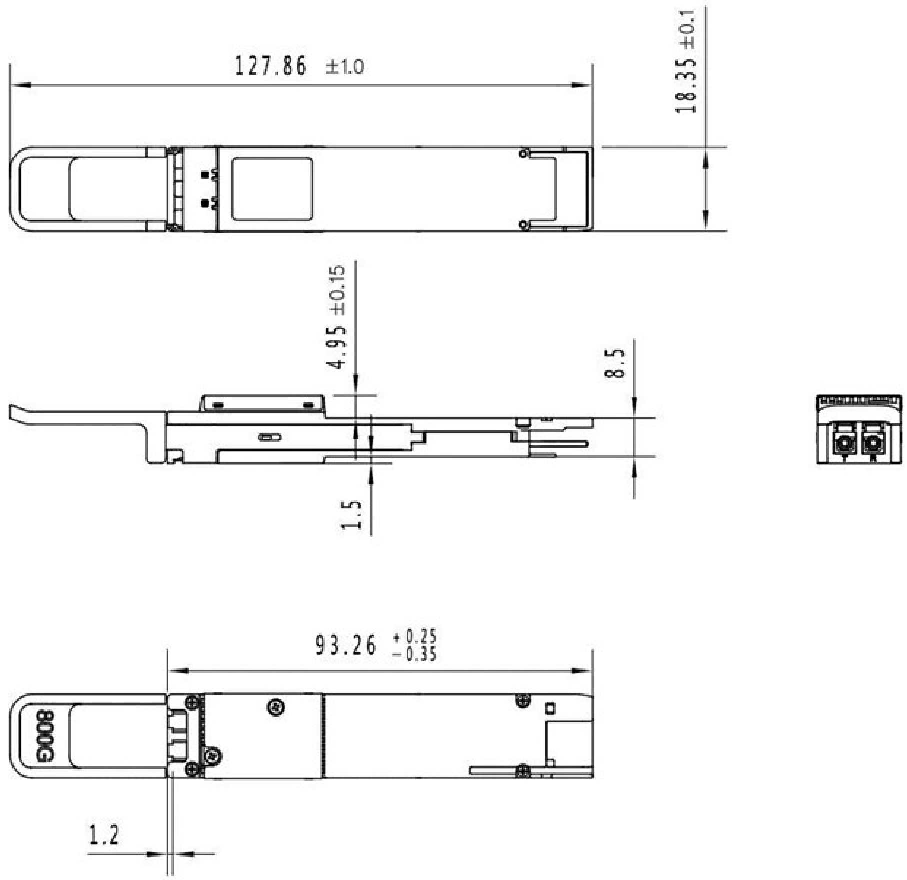
Block Diagram of the Transceiver



Recommended Interface Circuit



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.

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