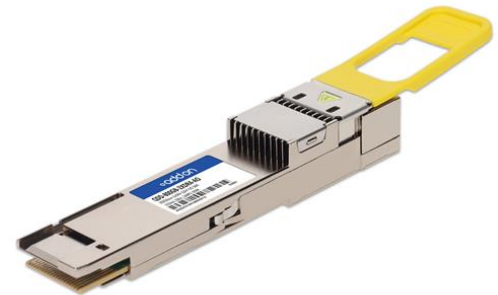


QDD-800GB-2XDR4-AO

MSA and TAA 800GBase-2xDR4 QSFP-DD Transceiver (SMF, 1310nm, 500m, 2xMPO-12, DOM, CMIS 5.0)

Features

- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR Optical Interface
- QSFP-DD MSA Compliant
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M Electrical Interface
- Compliant with CMIS 5.0
- Operating Temperature: 0 to 70 Celsius
- Dual MPO Connector
- RoHS Compliant and Lead-Free
- Class 1 Laser



Applications

- 800GBase-Ethernet

Product Description

This MSA compliant QSFP-DD transceiver provides 800GBase-2xDR4 throughput up to 500m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Power Supply Voltage	Vcc	-0.5		3.6	V	
Relative Humidity (Non-Condensing)	RH	5		95	%	
Data Input Voltage Differential	V _{DIP-V_{DIN}}			1	V	
Control Input Voltage	V _i	-0.3		Vcc+0.5	V	
Control Output Current	I _o	-20		20	mA	
Signaling Speed Per Lane	DRL		53.125		GBd	
Operating Distance		2		500	m	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	I _{CC_IP}			6600	mA	
Sustained Peak Current at Hot Plug	I _{CC_SP}			5446	mA	
Maximum Power Dissipation	PD			16.5	W	
Maximum Power Dissipation (Low-Power Mode)	PD _{LP}			2	W	
Control Input Voltage - High	V _{IH}	Vcc*0.7		Vcc+0.3	V	
Control Input Voltage - Low	V _{IL}	-0.3		Vcc*0.3	V	
2-Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise (1kHz to 1MHz, Pk-Pk)				66	mVp-p	
Transmitter (Module Input, TP1)						
Differential Pk-Pk Input Voltage Tolerance (TP1a)		750			mV	
Pk-Pk AC Common-Mode Voltage Tolerance	Low-Frequency (VCM _{LF})	32			mV	
	Full-Band (VCM _{FB})	80			mV	
Differential-Mode to Common-Mode Return Loss	RL _{cd}	802.3ck 120G-2			dB	
Effective Return Loss	ERL	8.5			dB	
Differential Termination Mismatch				10	%	
Single-Ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common-Mode Voltage Tolerance		-0.35		2.85	V	
Receiver (Module Output, TP4)						
Pk-Pk AC Common-Mode Voltage	Low-Frequency (VCM _{LF})			32	mV	
	Full-Band (VCM _{FB})			80	mV	
Differential Pk-Pk Output Voltage	Short-Mode			600	mV	
	Long-Mode			845	mV	

Eye Height	EH	15			mV	
Vertical Eye Closure	VEC			12	dB	
Common-Mode to Differential-Mode Return Loss	RLDc	802.3ck 120G-1			dB	
Effective Return Loss	ERL	8.5			dB	
Differential Termination Mismatch				10	%	
Transition Time		8.5			ps	
DC Common-Mode Voltage Tolerance		-0.35		2.85	V	

Electrical Low-Speed Control and Sense Signal Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Module Output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
InitMode, ResetL, and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	Vcc-0.5	Vcc+0.3	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	AOP_L	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}) Per Lane	OMA _{outer}	-0.8		4.2	dBm	
Launch Power in OMA _{outer} minus TDECQ per Lane	Extinction Ratio ≥ 5 dB	$T_{OMA-TDECQ}$	-2.2		dBm	
	Extinction Ratio < 5 dB		-1.9		dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane	TDECQ			3.4	dB	
TDECQ – $10\log_{10}(C_{eq})$ Per Lane	C_{eq}			3.4	dB	
Average Launch Power of Off Transmitter Per Lane	T_{off}			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	T_r			17	ps	
$RIN_{15.5OMA}$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORLT			15.5	dB	
Transmitter Reflectance	TR			-26	dB	2
Receiver						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold Per Lane	AOP_D	5			dBm	
Average Receive Power Per Lane	AOP_R	-5.9		4	dBm	
Receive Power (OMA _{outer}) Per Lane	OMA _R			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA _{outer}) Per Lane	SOMA			Max. (-3.9 SECQ-5.3)	dBm	3
Stressed Receiver Sensitivity (OMA _{outer}) Per Lane	SRS			-1.9	dBm	4
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ) Per Lane Under Test	SECQ		3.4		dB	
SECQ- $10\log_{10}(C_{eq})$ Per Lane Under Test	C_{eq}			3.4	dB	
OMA _{outer} of Each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMA_{outer}) per lane (maximum) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4} .

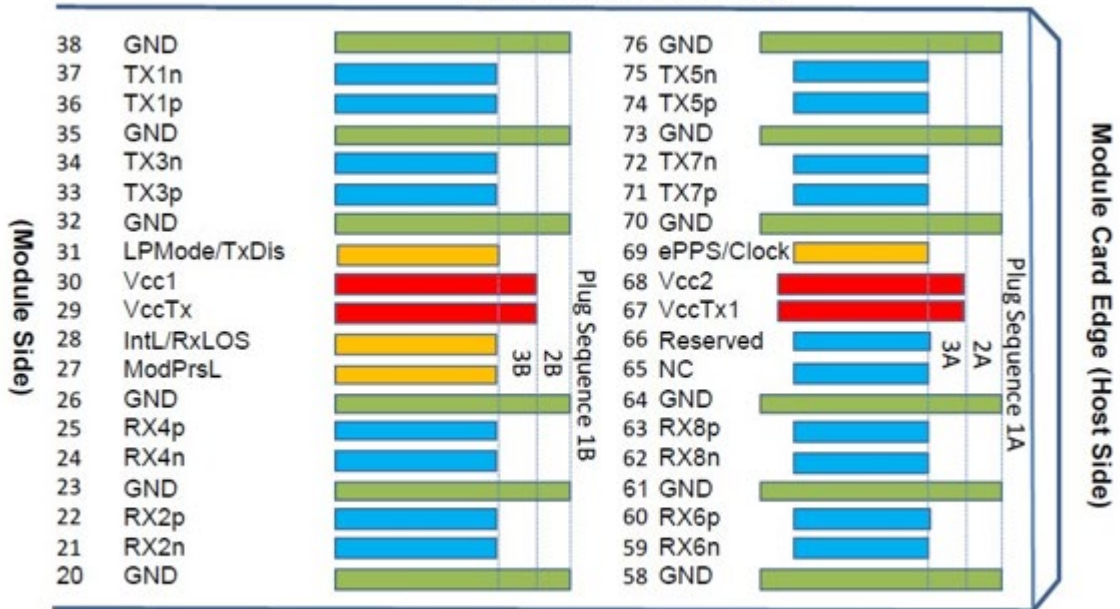
Pin Descriptions

Pin	Symbol	Logic	Name/Description	Notes
1	GND		Module Ground.	
2	Tx2-	CML-I	Transmitter Inverted Data Input.	
3	Tx2+	CML-I	Transmitter Non-Inverted Data Input.	
4	GND		Module Ground.	
5	Tx4-	CML-I	Transmitter Inverted Data Input.	
6	Tx4+	CML-I	Transmitter Non-Inverted Data Input.	
7	GND		Module Ground.	
8	ModSelL	LVTTTL-I	Module Select.	
9	ResetL	LVTTTL-I	Module Reset.	
10	VccRx		+3.3V Receiver Power Supply.	
11	SCL	LVC MOS-I/O	2-Wire Serial Interface Clock.	
12	SDA	LVC MOS-I/O	2-Wire Serial Interface Data.	
13	GND		Module Ground.	
14	Rx3+	CML-O	Receiver Non-Inverted Data Output.	
15	Rx3-	CML-O	Receiver Inverted Data Output.	
16	GND		Module Ground.	
17	Rx1+	CML-O	Receiver Non-Inverted Data Output.	
18	Rx1-	CML-O	Receiver Inverted Data Output.	
19	GND		Module Ground.	
20	GND		Module Ground.	
21	Rx2-	CML-O	Receiver Inverted Data Output.	
22	Rx2+	CML-O	Receiver Non-Inverted Data Output.	
23	GND		Module Ground.	
24	Rx4-	CML-O	Receiver Inverted Data Output.	
25	Rx4+	CML-O	Receiver Non-Inverted Data Output.	
26	GND		Module Ground.	
27	ModPrsL	LVTTTL-O	Module Present.	
28	IntL/RxLOS	LVTTTL-O	Interrupt. Optionally RxLOS.	
29	VccTx		+3.3V Transmitter Power Supply.	
30	Vcc1		+3.3V Power Supply.	
31	LPMMode/TxDis	LVTTTL-I	Low-Power Mode. Optionally Tx_Disable.	
32	GND		Module Ground.	
33	Tx3+	CML-I	Transmitter Non-Inverted Data Input.	
34	Tx3-	CML-I	Transmitter Inverted Data Input.	
35	GND		Module Ground.	
36	Tx1+	CML-I	Transmitter Non-Inverted Data Input.	
37	Tx1-	CML-I	Transmitter Inverted Data Input.	
38	GND		Module Ground.	
39	GND		Module Ground.	
40	Tx6-	CML-I	Transmitter Inverted Data Input.	
41	Tx6+	CML-I	Transmitter Non-Inverted Data Input.	

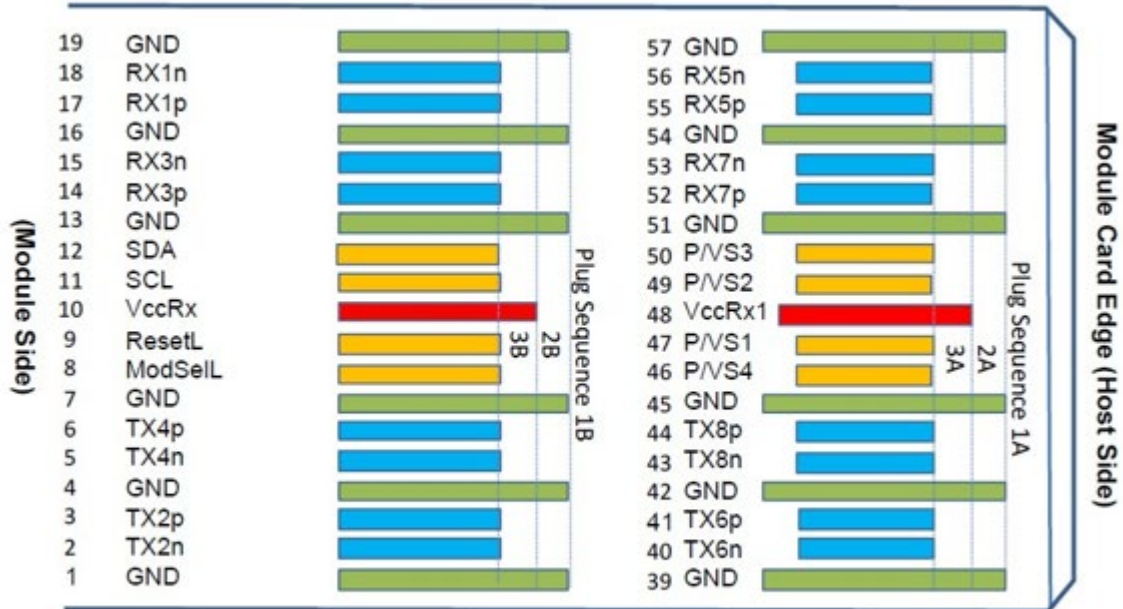
42	GND		Module Ground.	
43	Tx8-	CML-I	Transmitter Inverted Data Input.	
44	Tx8+	CML-I	Transmitter Non-Inverted Data Input.	
45	GND		Module Ground.	
46	P/VS4	LVC MOS/CML-I	Programmable. Module Vendor-Specific 4.	
47	P/VS1	LVC MOS/CML-I	Programmable. Module Vendor-Specific 1.	
48	VccRx1		+3.3V Receiver Power Supply.	
49	P/VS2	LVC MOS/CML-O	Programmable. Module Vendor-Specific 2.	
50	P/VS3	LVC MOS/CML-O	Programmable. Module Vendor-Specific 3.	
51	GND		Module Ground.	
52	Rx7+	CML-O	Receiver Non-Inverted Data Output.	
53	Rx7-	CML-O	Receiver Inverted Data Output.	
54	GND		Module Ground.	
55	Rx5+	CML-O	Receiver Non-Inverted Data Output.	
56	Rx5-	CML-O	Receiver Inverted Data Output.	
57	GND		Module Ground.	
58	GND		Module Ground.	
59	Rx6-	CML-O	Receiver Inverted Data Output.	
60	Rx6+	CML-O	Receiver Non-Inverted Data Output.	
61	GND		Module Ground.	
62	Rx8-	CML-O	Receiver Inverted Data Output.	
63	Rx8+	CML-O	Receiver Non-Inverted Data Output.	
64	GND		Module Ground.	
65	NC		Not Connected.	
66	Reserved			
67	VccTx1		+3.3V Power Supply.	
68	Vcc2		+3.3V Power Supply.	
69	ePPS/Clock	LVC MOS-I	1PPS PTP Clock or Reference Clock Input.	
70	GND		Module Ground.	
71	Tx7+	CML-I	Transmitter Non-Inverted Data Input.	
72	Tx7-	CML-I	Transmitter Inverted Data Input.	
73	GND		Module Ground.	
74	Tx5+	CML-I	Transmitter Non-Inverted Data Input.	
75	Tx5-	CML-I	Transmitter Inverted Data Input.	
76	GND		Module Ground.	

Electrical Pad Layout

Top PCB viewed from top



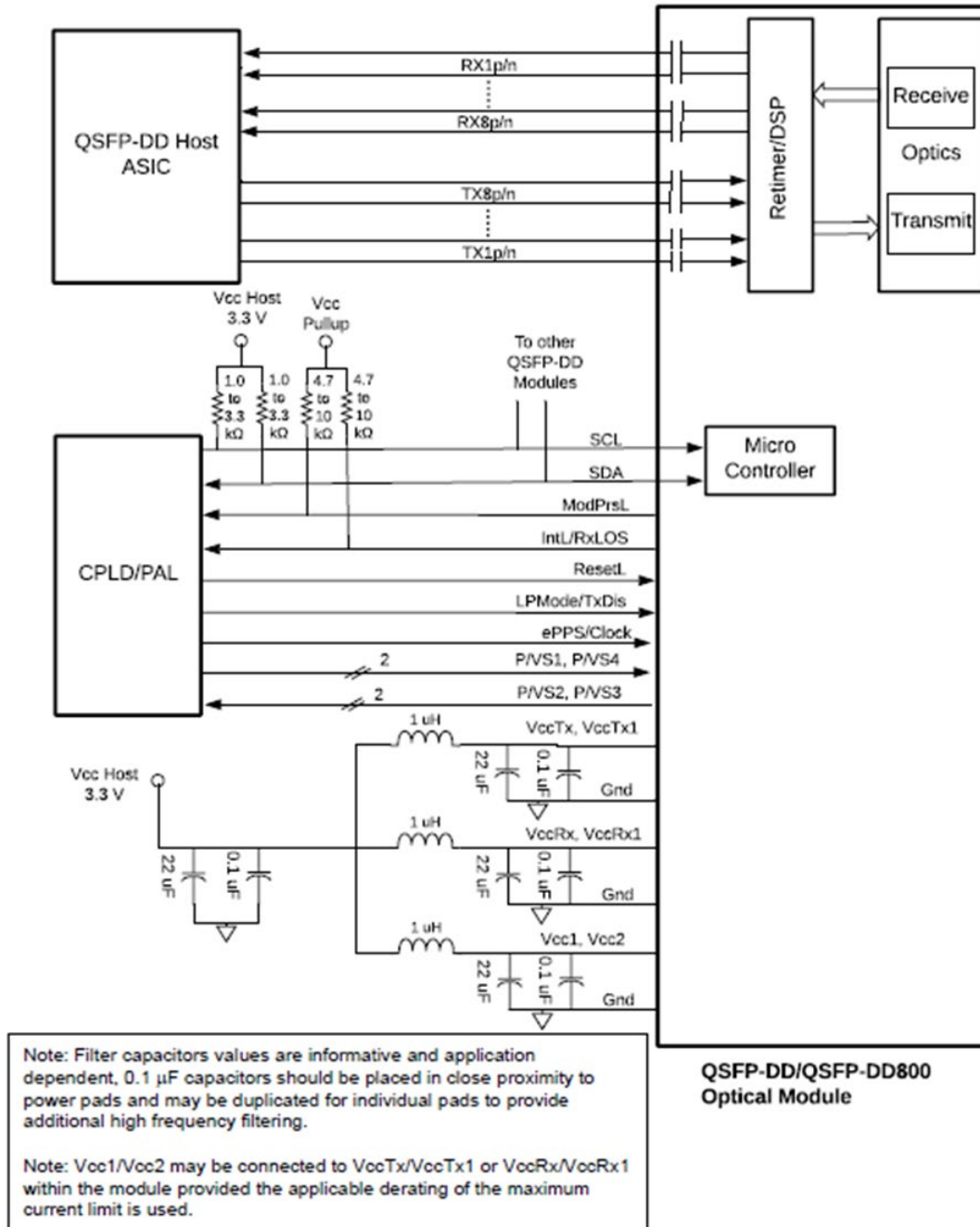
Bottom PCB viewed from bottom



Classic
QSFP+/QSFP28/QSFP112 Pads

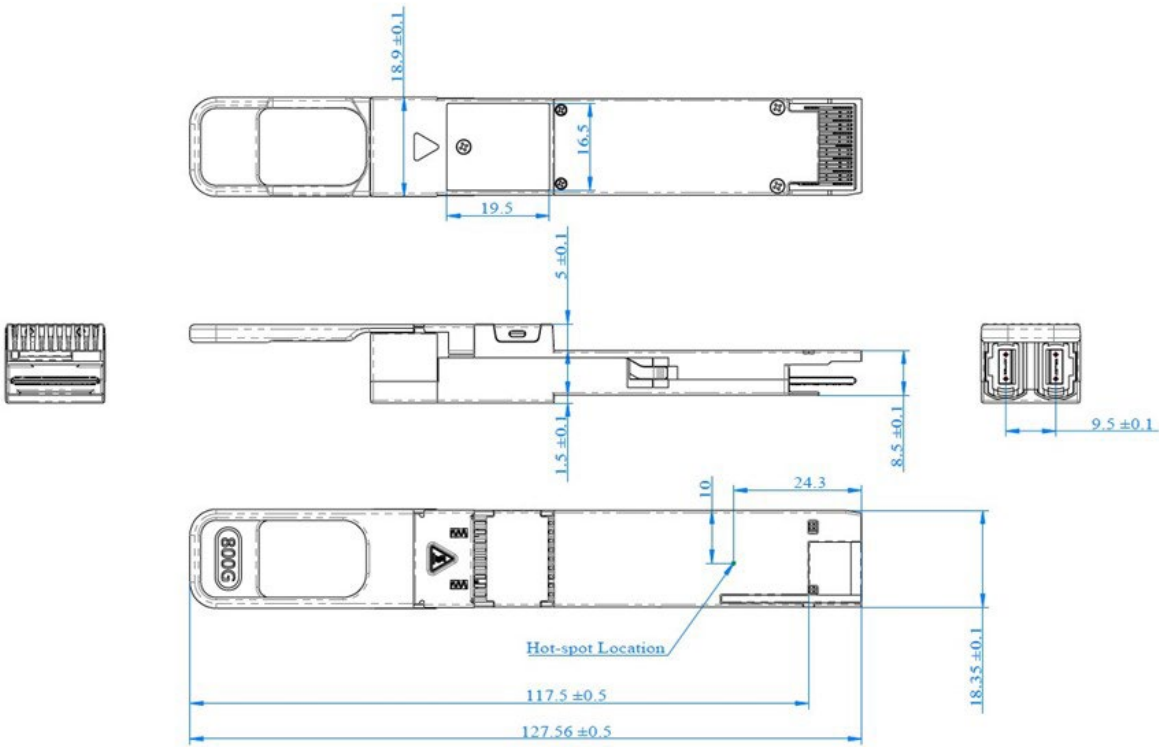
Additional
QSFP-DD/QSFP-DD800 Pads

Recommended Host Board Schematic



**QSFP-DD/QSFP-DD800
Optical Module**

Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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