Preliminary Datasheet

OSFP224-1600GB-2XFR4-LRO-AO

MSA 1.6T 2xFR4 PAM4 OSFP224 Transceiver (SMF, 1310nm, 2km, 2xLC, DOM, CMIS 5.3) LRO

Features:

- OSFP MSA Compliant
- Duplex LC Optical Receptacle Connector
- Hot-Pluggable
- CMIS 5.3
- Up to 2km Transmission on Single-Mode Fiber
- Single 3.3V Power Supply
- Power Consumption: 19W Maximum
- Operating Temperature: 0 to 70 Celsius
- RoHS Compliant and Lead-Free

Applications:

- 16x100GBase Ethernet
- 2x800GBase Ethernet
- InfiniBand

Product Description:

This MSA compliant OSFP224 transceiver provides 1600GBase-2xFR4 throughput up to 2km over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0	25	70	°C	
Relative Humidity – Storage (Non-Condensing)	RHstg	0		95	%	2
Relative Humidity – Operating (Non-Condensing)	RHc	0		85	%	2
Supply Voltage	Vcc	-0.5		3.6	V	
PAM4 Signaling Rate Per Lane	S		106.25		GBaud	3

Notes:

1. Exceeding the "Absolute Maximum Ratings" may cause irreversible damage to the device. The device is not intended to be operated under the condition of simultaneous "Absolute Maximum Ratings," a condition which may cause irreversible damage to the device.
2. Non-Condensing.
3. Range: ±100ppm.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption	PC			19	W	
Transmitter						
Tx_Data Differential Input Voltage	VIN			880	mV	
Tx_Data Differential Input Impedance	ZIN		93		Ω	
Signaling Rate Per Lane	S		106.25		GBaud	1
Receiver						
Rx_Data Differential Output Voltage	VOUT			800	mV	
Rx_Data Differential Output Impedance	ZOUT		93		Ω	2
Signaling Rate Per Lane	S		106.25		GBaud	1

Notes:

1. ±8%
2. Range: ±50ppm.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Rate Per Lane		106.25 ± 50ppm			GBd	
Laser Type		DFB+SiPho PIC				
Lane Wavelength	λ	1264.5	1271	1277.5	nm	
		1284.5	1291	1297.5	nm	
		1304.5	1311	1317.5	nm	
		1324.5	1331	1337.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	Pout	-2.2		4.9	dBm	
Outer Optical Modulation Amplitude	OMAouter	-0.8		4.8	dBm	1
		-1+TDECQ		4.8	dBm	2
Transmitter and Dispersion Penalty Eye Closure for PAM4	TDECQ			3.4	dB	3
Optical Output with Tx Off Per Lane	Poff			-16	dBm	
Extinction Ratio	ER	3.5			dB	3
Transmitter Reflectance	RFL			-26	dB	
Receiver						
Signaling Rate Per Lane	Sr	106.25 ± 50ppm			GBd	
Lane Wavelength	λ	1264.5	1271	1277.5	nm	
		1284.5	1291	1297.5	nm	
		1304.5	1311	1317.5	nm	
		1324.5	1331	1337.5	nm	
Receiver Sensitivity (OMAouter) Per Lane	SEN	-3.7		4.8	dBm	4, 6
		-4.6+TECQ		4.8	dBm	5, 6
Average Receiver Power Per Lane	P_{IN}	-6.2		4.9	dBm	6
Damage Threshold Per Lane		5.9			dBm	
Receiver Reflectance	RFL			-26	dB	

Notes:

1. For TDECQ<0.9dB
2. For 0.9dB≤TDECQ≤3.4dB.
3. Test with SSPRQ pattern, the reference equalizer is 15-tap FFE.
4. For TECQ<0.9dB
5. For 0.9dB≤TECQ≤3.4dB.
6. PAM4 Signaling rate per lane 106.25GBaud, $6.4E^{-5}$ and PRBS 2^{31}-1.

Pin Descriptions

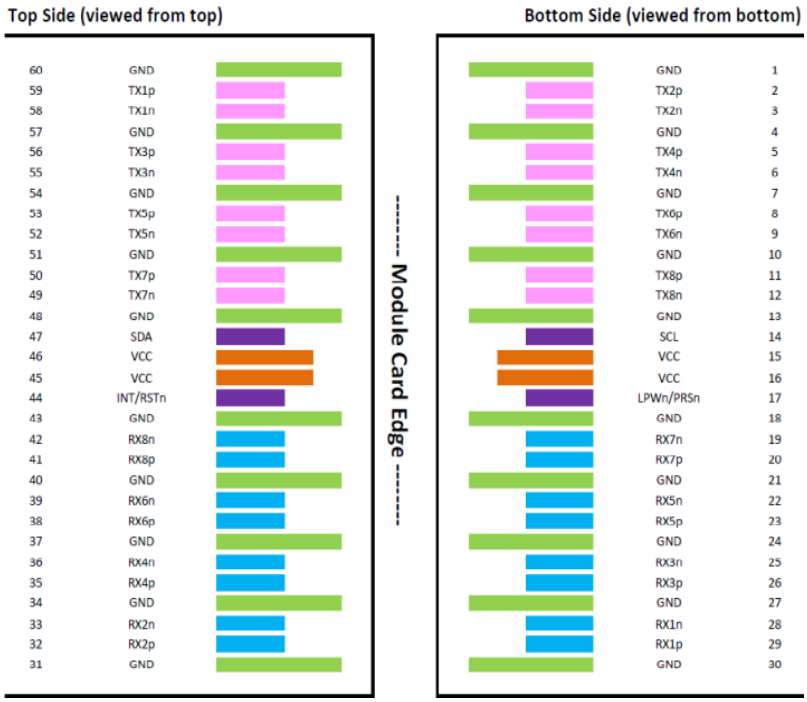
Pin	Logic	Symbol	Name/Description	Direction	Plug Sequence	Notes
1		GND	Module Ground.		1	
2	CML-I	Tx2+	CH2 Transmitter Date Non-Inverted.	Input from Host	3	
3	CML-I	Tx2-	CH2 Transmitter Date Inverted.	Input from Host	3	
4		GND	Module Ground.		1	
5	CML-I	Tx4+	CH4 Transmitter Date Non-Inverted.	Input from Host	3	
6	CML-I	Tx4-	CH4 Transmitter Date Inverted.	Input from Host	3	
7		GND	Module Ground.		1	
8	CML-I	Tx6+	CH6 Transmitter Date Non-Inverted.	Input from Host	3	
9	CML-I	Tx6-	CH6 Transmitter Date Inverted.	Input from Host	3	
10		GND	Module Ground.		1	
11	CML-I	Tx8+	CH8 Transmitter Date Non-Inverted.	Input from Host	3	
12	CML-I	Tx8-	CH8 Transmitter Date Inverted.	Input from Host	3	
13		GND	Module Ground.		1	
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	Bi-Directional	3	1
15		Vcc	+3.3V Power Supply.	Power from Host	2	
16		Vcc	+3.3V Power Supply.	Power from Host	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	Bi-Directional	3	2
18		GND	Module Ground.		1	
19	CML-O	Rx7-	CH7 Receiver Date Inverted.	Output to Host	3	
20	CML-O	Rx7+	CH7 Receiver Date No-Inverted.	Output to Host	3	
21		GND	Module Ground.		1	
22	CML-O	Rx5-	CH5 Receiver Date Inverted.	Output to Host	3	
23	CML-O	Rx5+	CH5 Receiver Date Non-Inverted.	Output to Host	3	
24		GND	Module Ground.		1	
25	CML-O	Rx3-	CH3 Receiver Date Inverted.	Output to Host	3	
26	CML-O	Rx3+	CH3 Receiver Date Non-Inverted.	Output to Host	3	
27		GND	Module Ground.		1	
28	CML-O	Rx1-	CH1 Receiver Date Inverted.	Output to Host	3	
29	CML-O	Rx1+	CH1 Receiver Date Non-Inverted.	Output to Host	3	
30		GND	Module Ground.		1	
31		GND	Module Ground.		1	
32	CML-O	Rx2+	CH2 Receiver Date Non-Inverted.	Output to Host	3	
33	CML-O	Rx2-	CH2 Receiver Date Inverted.	Output to Host	3	
34		GND	Module Ground.		1	
35	CML-O	Rx4+	CH4 Receiver Date Non-Inverted.	Output to Host	3	
36	CML-O	Rx4-	CH4 Receiver Date Inverted.	Output to Host	3	

37		GND	Module Ground.		1	
38	CML-O	Rx6+	CH6 Receiver Date Non-Inverted.	Output to Host	3	
39	CML-O	Rx6-	CH6 Receiver Date Inverted.	Output to Host	3	
40		GND	Module Ground.		1	
41	CML-O	Rx8+	CH8 Receiver Date Non-Inverted.	Output to Host	3	
42	CML-O	Rx8-	CH8 Receiver Date Inverted.	Output to Host	3	
43		GND	Module Ground.		1	
44	Multi-Level	INT/RSTn	Module Interrupt/Module Reset.	Bi-Directional	3	3
45		Vcc	+3.3V Power Supply.	Power from Host	2	
46		Vcc	+3.3V Power Supply.	Power from Host	2	
47	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	Bi-Directional	3	4
48		GND	Module Ground.		1	
49	CML-I	Tx7-	CH7 Transmitter Date Inverted.	Input from Host	3	
50	CML-I	Tx7+	CH7 Transmitter Date Non-Inverted.	Input from Host	3	
51		GND	Module Ground.		1	
52	CML-I	Tx5-	CH5 Transmitter Date Inverted.	Input from Host	3	
53	CML-I	Tx5+	CH5 Transmitter Date Non-Inverted.	Input from Host	3	
54		GND	Module Ground.		1	
55	CML-I	Tx3-	CH3 Transmitter Date Inverted.	Input from Host	3	
56	CML-I	Tx3+	CH3 Transmitter Date Non-Inverted.	Input from Host	3	
57		GND	Module Ground.		1	
58	CML-I	Tx1-	CH1 Transmitter Date Inverted.	Input from Host	3	
59	CML-I	Tx1+	CH1 Transmitter Date Non-Inverted.	Input from Host	3	
60		GND	Module Ground.		1	

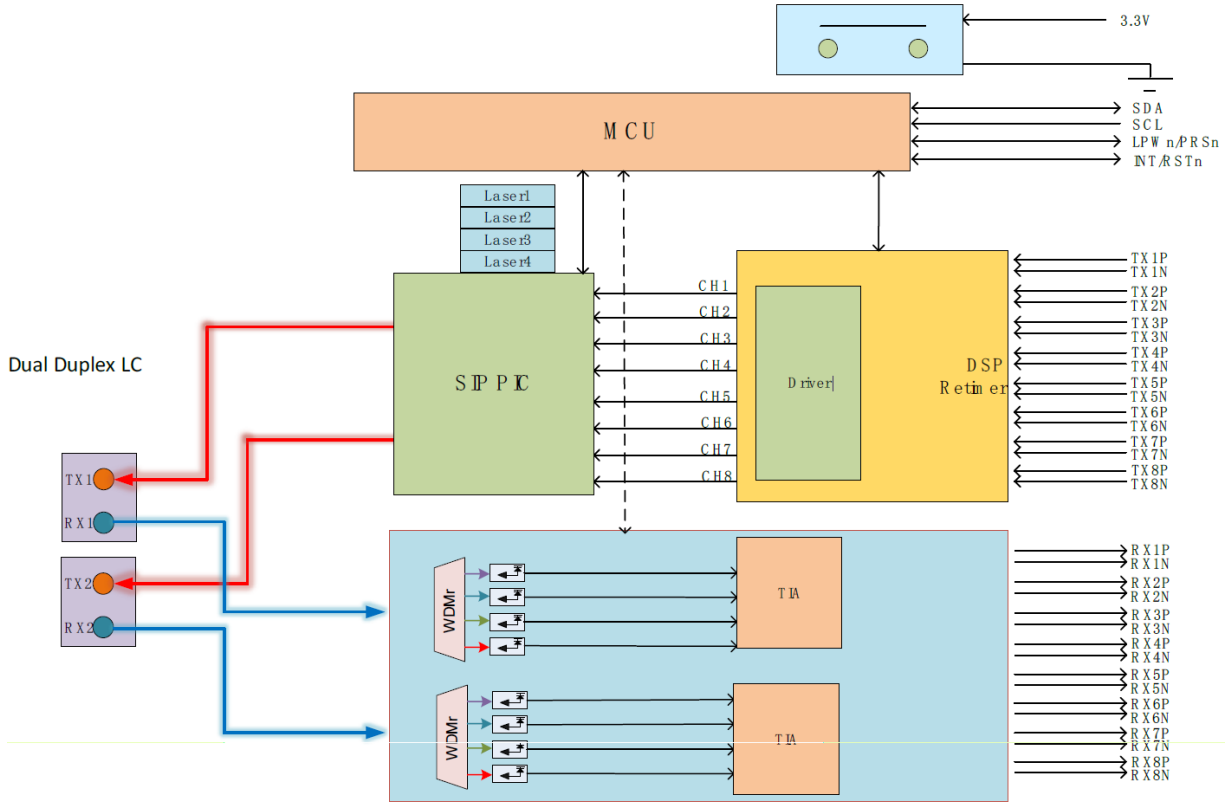
Notes:

1. Open-drain with Pull-up resistor on host.
2. LPWn/PRSn is a dual function signal that allows the host to signal low-power mode and for the module to indicate that the module is present.
3. INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.

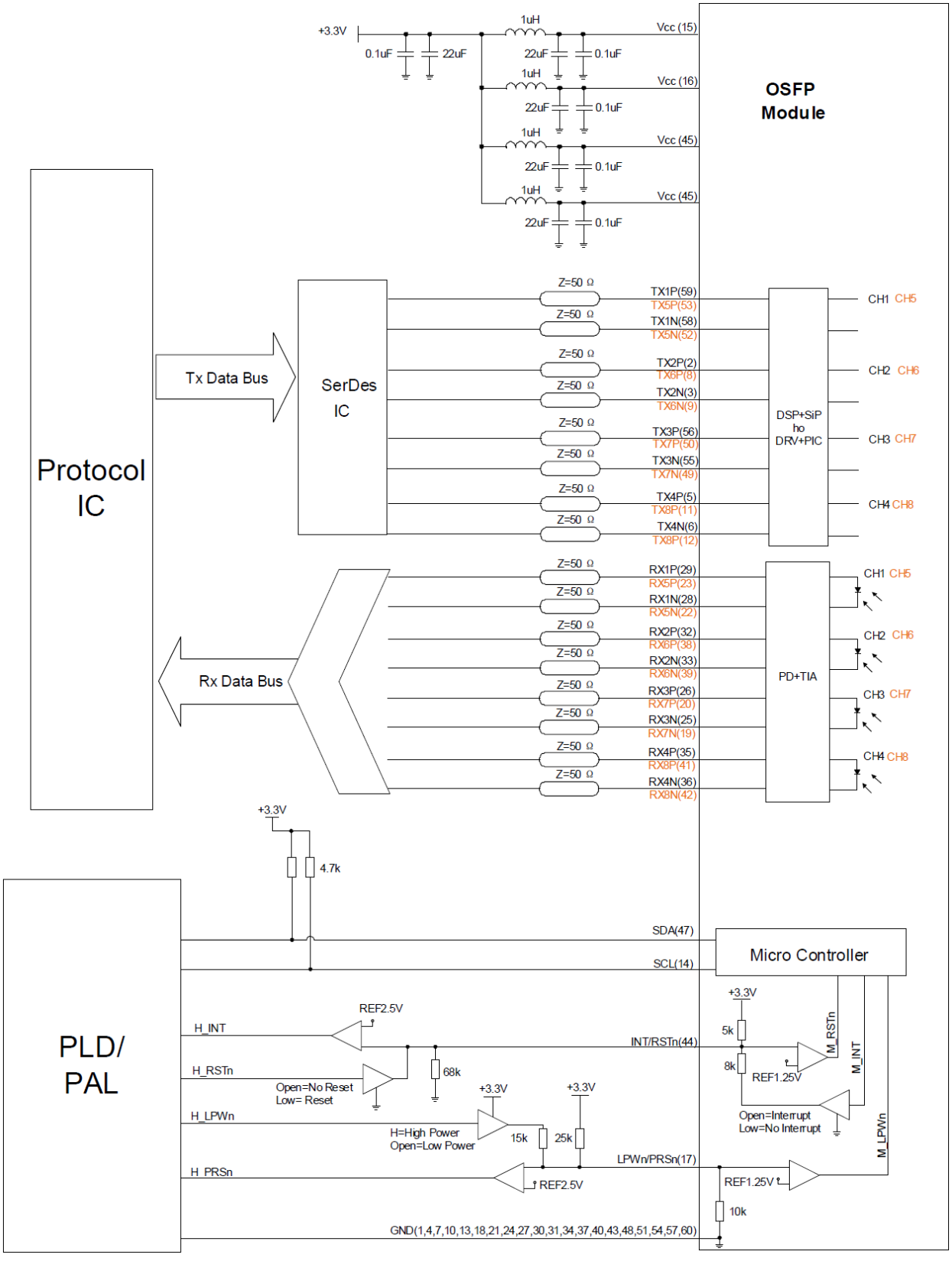
Electrical Pad Layout



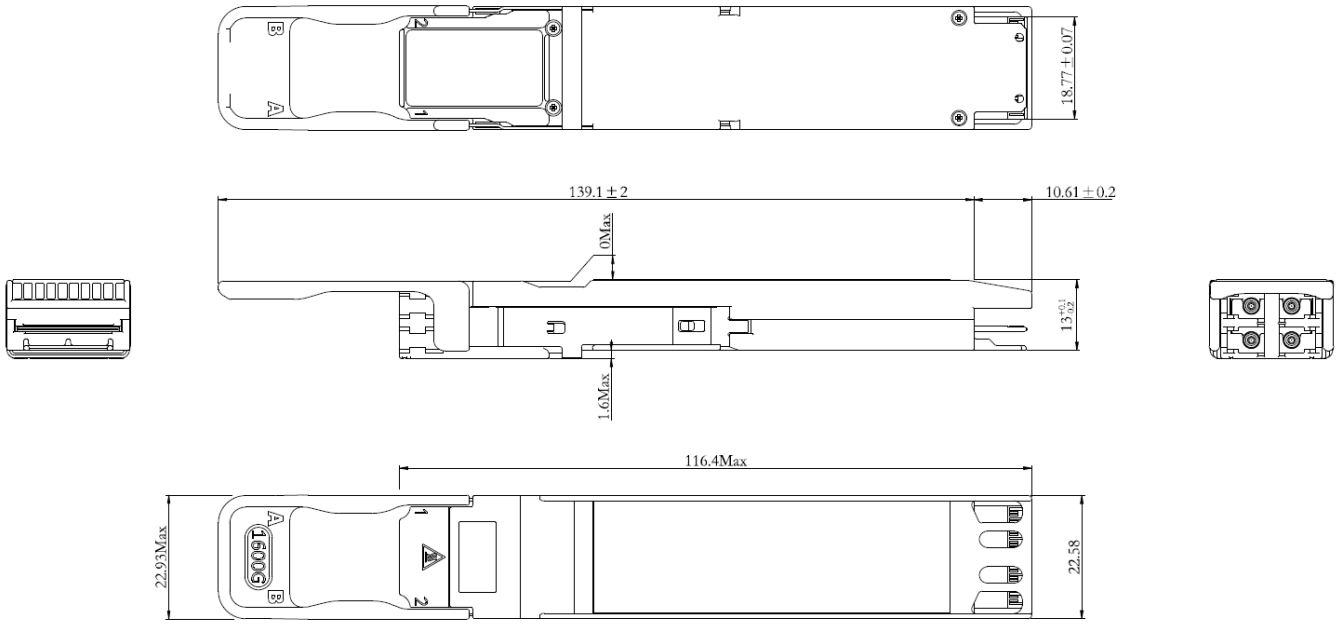
Block Diagram



Host Board


OSFP Module
Protocol IC
Tx Data Bus
SerDes IC
Rx Data Bus
DSP+SiPho DRV+PIC
PD+TIA
PLD/ PAL
Micro Controller
+3.3V
1uH
0.1uF
22uF
Vcc (15)
Vcc (16)
Vcc (45)
Vcc (45)
Z=50 Ω
TX1P(59)
TX5P(53)
TX1N(58)
TX5N(52)
TX2P(2)
TX6P(8)
TX2N(3)
TX6N(9)
TX3P(56)
TX7P(50)
TX3N(55)
TX7N(49)
TX4P(5)
TX8P(11)
TX4N(6)
TX8P(12)
CH1 CH5
CH2 CH6
CH3 CH7
CH4 CH8
RX1P(29)
RX5P(23)
RX1N(28)
RX5N(22)
RX2P(32)
RX6P(38)
RX2N(33)
RX6N(39)
RX3P(26)
RX7P(20)
RX3N(25)
RX7N(19)
RX4P(35)
RX8P(41)
RX4N(36)
RX8N(42)
4.7k
SDA(47)
SCL(14)
REF2.5V
H_INT
H_RSTn
Open=No Reset
Low= Reset
68k
H_LPWn
H=High Power
Open=Low Power
15k
25k
H_PRSn
INT/RSTn(44)
LPWn/PRSn(17)
5k
8k
REF1.25V
M_RSTn
M_INT
M_LPWn
Open=Interrupt
Low=No Interrupt
10k
GND(1,4,7,10,13,18,21,24,27,30,31,34,37,40,43,48,51,54,57,60)

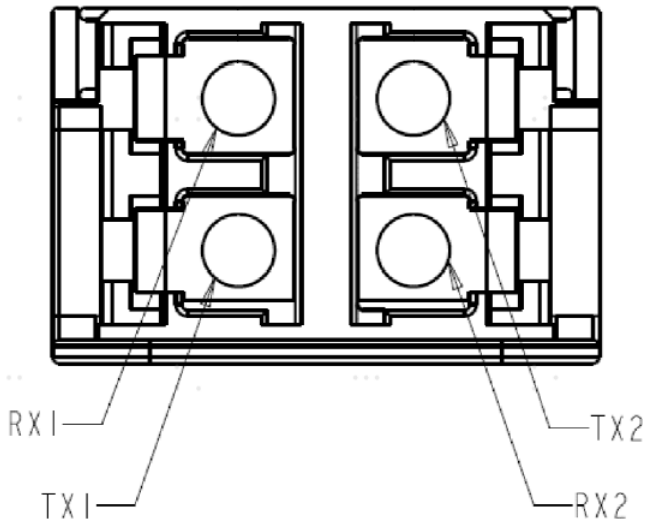
Mechanical Specification



Notes:

1. Tolerance: ±0.1mm.
2. Others according with OSFP MSA.
3. Optical port according with Fiber Connector Specifications.

Optical Lane Assignment



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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