QDD-800GB-LB-0DB-AO

MSA and TAA 800GBase QSFP-DD Loopback Transceiver with 0dB Attenuation

Features

- Compliant with SFF-8024
- Built-In Surge Current Mitigation Technology
- Supports 8x10G/25G/56G PAM4/112G PAM4 Data Rates
- Multi-Color LED Indicator for High/Low-Power Modes
- +3.3V Power Supply
- Built-In High-Precision Temperature Monitoring w/ Calibration Algorithm
- Operating Temperature: 0 to 70 Celsius
- Hot-Pluggable
- RoHS Compliant and Lead-Free

Applications

- Ethernet IEEE 802.3 (Gigabit, 10 Gigabit and 25 Gigabit Ethernet)
- QSFP-DD port/system testing
- SONET, SDH, GBE, Fiber Channel Support

Product Description

This MSA compliant QSFP-DD loopback provides a simple solution to loopback testing on individual ports with the use of a cable assembly. It has 0dB of attenuation and is compatible with existing 800G QSFP-DD ports. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Rev. 060226

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Tstg	-40	+85	°C
Ambient Operating Temperature	Ta	0	+70	°C
Storage Relative Humidity	RHs	0	95	%
Operating Relative Humidity	RHo	0	85	%
Power Supply Voltage	Vcc	2.97	+3.63	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	Ta	0		+70	°C
Power Supply Voltage	Vcc	2.97	3.3	3.63	V
Data Rate	DR	0.1		800	Gbps
Durability Cycles			2000	2250	Times

High-Speed Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input/Output Impedance	Zd	90	95	105	Ω	1
Return Loss	SDD11/22	<-10 0.01GHz ≤ f < 10GHz <-5 10GHz ≤ f < 40GHz			dB	
Insertion Loss	SDD21			7 (Include Trace&Via&Mating& Connectors, Without MCB Insertion Loss)	dB	2
				11.5 (Include MCB Insertion Loss&Trace&Via& Mating&Connectors)	dB	2
Intra Pair Skew	IPS			100	ps	

Notes:

1. Differential impedance.
2. The insertion loss for Tx to Rx, including the AC caps, as measured with MCB. The MCB insertion loss complies with IEEE 802.3ck CL 162B.1.2.1.

Pin Descriptions

Pin	Symbol	Logic	Name/Description	Plug Sequence	Notes
1	GND		Module Ground.	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input.	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input.	3B	
4	GND		Module Ground.	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input.	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input.	3B	
7	GND		Module Ground.	1B	1
8	ModSelL	LVTTL-I	Module Select.	3B	
9	ResetL	LVTTL-I	Module Reset.	3B	
10	VccRx		+3.3V Receiver Power Supply.	2B	2
11	SCL	LVCMOS-I/O	2-Wire Serial Interface Clock.	3B	
12	SDA	LVCMOS-I/O	2-Wire Serial Interface Data.	3B	
13	GND		Module Ground.	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output.	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output.	3B	
16	GND		Module Ground.	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output.	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output.	3B	
19	GND		Module Ground.	1B	1
20	GND		Module Ground.	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output.	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output.	3B	
23	GND		Module Ground.	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output.	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output.	3B	
26	GND		Module Ground.	1B	1
27	ModPrsL	LVTTL-O	Module Present.	3B	
28	IntL/RxLOS	LVTTL-O	Interrupt. Optionally RxLOS.	3B	
29	VccTx		+3.3V Transmitter Power Supply.	2B	2
30	Vcc1		+3.3V Power Supply.	2B	2
31	LPMode/TxDis	LVTTL-I	Low-Power Mode. Optionally TxDis.	3B	
32	GND		Module Ground.	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input.	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input.	3B	
35	GND		Module Ground.	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input.	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input.	3B	
38	GND		Module Ground.	1B	1
39	GND		Module Ground.	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input.	3A	

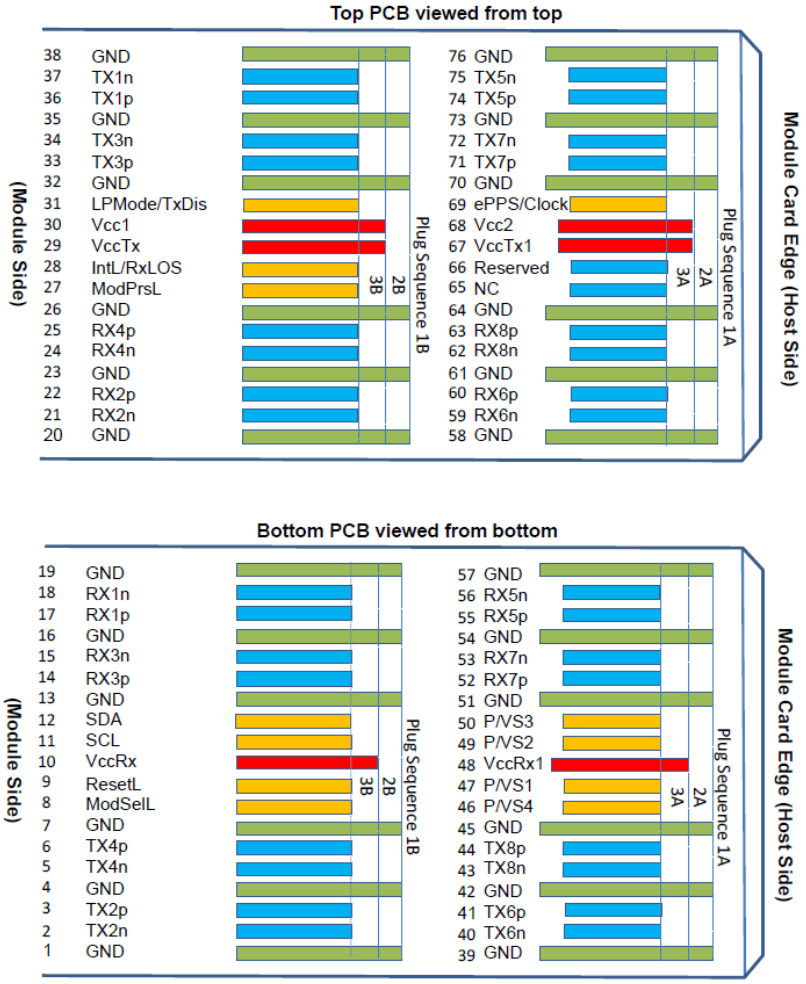
41	Tx6p	CML-I	Transmitter Non-Inverted Data Input.	3A	
42	GND		Module Ground.	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input.	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Input.	3A	
45	GND		Module Ground.	1A	1
46	P/VS4	LVCMOS/CML-I	Programmable. Module Vendor-Specific 4.	3A	5
47	P/VS1	LVCMOS/CML-I	Programmable. Module Vendor-Specific 1.	3A	5
48	VccRx1		+3.3V Receiver Power Supply.	2A	2
49	P/VS2	LVCMOS/CML-O	Programmable. Module Vendor-Specific 2.	3A	5
50	P/VS3	LVCMOS/CML-O	Programmable. Module Vendor-Specific 3.	3A	5
51	GND		Module Ground.	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output.	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output.	3A	
54	GND		Module Ground.	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output.	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output.	3A	
57	GND		Module Ground.	1A	1
58	GND		Module Ground.	1A	1
59	Rx6n	CML-O	Receiver Inverted Data Output.	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output.	3A	
61	GND		Module Ground.	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output.	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output.	3A	
64	GND		Module Ground.	1A	1
65	NC		Not Connected.	3A	3
66	Reserved		For Future Use.	3A	3
67	VccTx1		+3.3V Power Supply.	2A	2
68	Vcc2		+3.3V Power Supply.	2A	2
69	ePPS/Clock	LVCMOS-I	1PPS PTP Clock or Reference Clock Input.	3A	6
70	GND		Module Ground.	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Input.	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Input.	3A	
73	GND		Module Ground.	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Input.	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Input.	3A	
76	GND		Module Ground.	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane. Each connector GND contact is rated for a steady state current of 500mA.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector. For power classes 4 and above, the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500mA.
3. Reserved pad recommended to be terminated with 10kΩ to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module, optionally pad 65 may get terminated with 10kΩ to ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
5. Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor-specific inputs P/VS1 and P/VS4 signals, it is recommended for each to be terminated in the module with 10kΩ. For host designs using programmable/vendor-specific outputs P/VS2 and P/VS3 signals, it is recommended each to be terminated on the host with 10kΩ.
6. For a host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination inside the module.

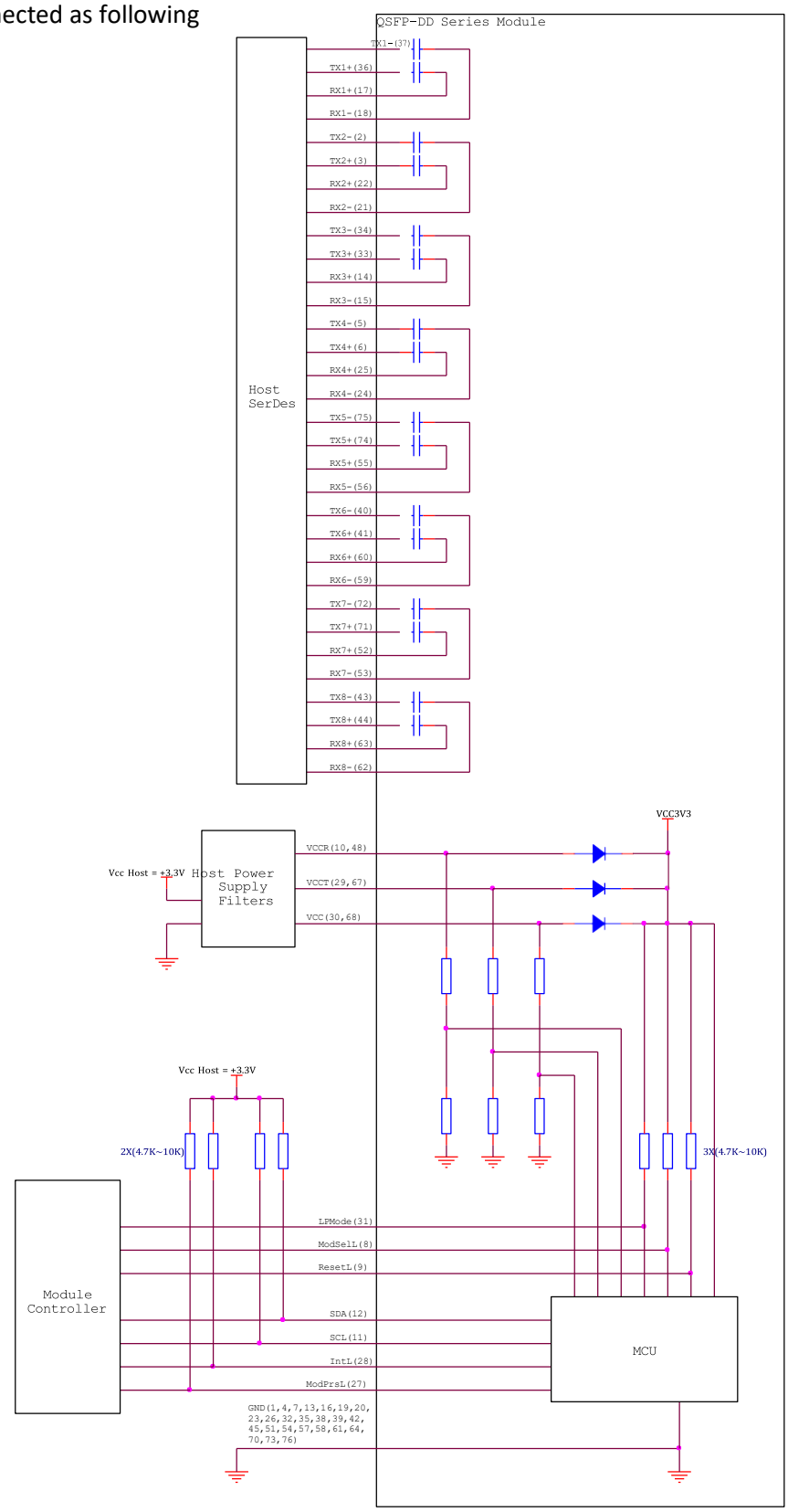
Electrical Pad Layout



Typical Application Circuit

The 16 lanes are connected as following with match polarity:

- TX1 and RX1
- TX2 and RX2
- TX3 and RX3
- TX4 and RX4
- TX5 and RX5
- TX6 and RX6
- TX7 and RX7
- TX8 and RX8



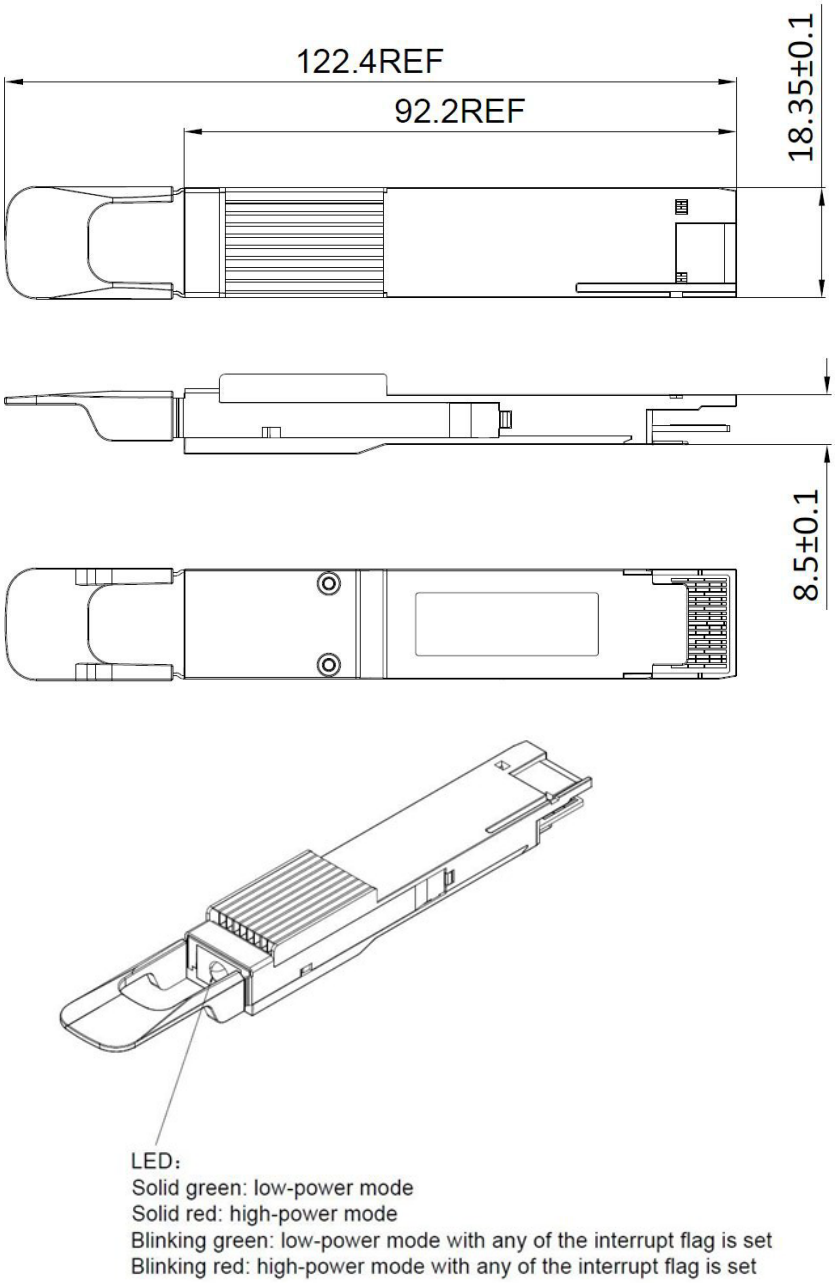
Status LED

A multi-color LED must be viewed from the front of the module in order to signify high/low-power modes, as well as interrupts.

- Solid green: low-power mode
- Solid red: high-power mode
- Blinking green: low-power mode with any of the interrupt flag is set
- Blinking red: high-power mode with any of the interrupt flag is set

Mechanical Specifications

Dimensions are in millimeters. Unit: mm.



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.

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