

#### QSFPDD-400G-AOC10M-AO

MSA and TAA Compliant 400GBase-AOC QSFP-DD to QSFP-DD Active Optical Cable (850nm, MMF, 10m)

#### **Features**

- Multi-rate capabilities: Up to 400Gbps
- QSFP-DD Form Factor
- Hot-Pluggable Active Cable
- 10m Length
- 8x50Gbps PAM4 Modulation
- Jacket Cable LSZH
- CMIS 3.1 Compliant I<sup>2</sup>C Interface
- Power: 10W Typical per Cable End
- ROHS-6 Compliant



### **Applications**

50/200/400G Ethernet

### **Product Description**

This is an MSA compliant 400GBase-AOC QSFP-DD to QSFP-DD active optical cable that operates over active fiber with a maximum reach of 10m. At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's QSFP-DD active optical cables are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



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# **Regulatory Compliance**

| Certification    | Standard  |
|------------------|---|
| Laser Eye Safety | IEC: 60825-1, 3 <sup>rd</sup> Edition<br>FDA: CFR-21 Sections 1040.10 and 1040.11 |
| Product Safety   | TUV: EN62368-1<br>UL/CSA 60950-1  |
| EMC/EMI          | FCC: Part 15 sb.B<br>EN: 55032/55024  |

## **Absolute Maximum Ratings**

| Parameter                           | Symbol                                  | Min  | Тур. | Max. | Unit |
|-------------------------------------|---|------|------|------|------|
| Supply Voltage                      | Vcc, Vcc2, VccTx, VccTx1, VccRx, VccRx1 | -0.5 |      | 3.6  | V    |
| Storage Temperature                 | Ts                                      | -10  |      | 85   | °C   |
| Storage Humidity (non-Condensation) | RHU                                     | 5    |      | 85   | %    |
| Differential Max. Input Voltage     | Vin-diff-maxd                           |      |      | 1600 | mV   |

# **Recommended Operating Conditions**

| Parameter                  | Symbol                                  | Min | Тур.   | Max. | Unit |
|----------------------------|---|-----|--------|------|------|
| Supply Voltage             | Vcc, Vcc2, VccTx, VccTx1, VccRx, VccRx1 |     | 3.3    |      | V    |
| Case Operating Temperature | Тор                                     | 0   |        | 70   | °C   |
| Module Total Power         | PTOT                                    |     | 10     |      | W    |
| Operating Humidity         | RH                                      | 5   |        | 85   | %    |
| Signaling Rate Per Lane    | FD                                      |     | 53.125 |      | Gb/s |

## **General Characteristics**

| Parameter                        | Symbol   | Unit | Notes                            |
|----------------------------------|--|------|----------------------------------|
| Module Form Factor               | QSFP-DD Type 1                                 |      | QSFP-DD MSA<br>Hardware Rev. 4.0 |
| Number of Lanes                  | 8 Tx, 8 Rx                                     |      |                                  |
| Maximum Aggregate Data Rate      | 425  | Gb/s |                                  |
| Maximum Data Rate per Lane       | 53.125   | Gb/s |                                  |
| Protocols Supported              | 50GbE, 200GbE, 400GbE                          |      |                                  |
| Electrical Interface and Pin-Out | 8x50G PAM4, 8x25G NRZ<br>76-pin Edge Connector |      |                                  |
| Management Interface             | Serial, I <sup>2</sup> C based, 400KHz Max     |      | CMIS Rev. 3.1 compliant          |

# **Electrical and Timing Characteristics**

| Parameter                                      | Symbol  | Min.      | Тур.               | Max.              | Unit. | Notes |
|--|---------|-----------|--------------------|-------------------|-------|-------|
| Supply voltage                                 | Vcc     | 3.135     | 3.3                | 3.465             | V     |       |
| Supply Current, per cable end                  | Icc     |           |                    |                   | mA    |       |
| Power Dissipation, per cable end               | Р       |           | 10                 |                   | W     |       |
| Latency  | TL      |           | TBD                |                   | ms    |       |
| Bit Error Rate (Pre-FEC)                       | BER     |           | < 1E <sup>-8</sup> | 5E <sup>-05</sup> |       |       |
| Transmit High Speed Electrical Specifications  |         |           |                    |                   |       |       |
| High Speed Differential Termination Resistance | ZTERMio |           | 100                |                   | Ω     |       |
| Differential Voltage                           | Vin_pp  |           |                    | 1600              | mVpp  |       |
| Input Differential Return loss                 | SDD11   | Compliant | to IEEE 802.       | 3bs               | dB    |       |
| Receive High Speed Electrical Specifications   |         |           |                    |                   |       |       |
| Signaling rate per lane                        |         |           | 53.125             |                   | Gb/s  |       |
| High Speed Differential Termination Resistance | ZTERMio |           | 100                |                   | Ω     |       |
| Differential output swing                      | Vout_pp |           |                    | 900               | mVpp  |       |
| Output rise/fall time (20-80%)                 |         |           |                    | TBD               | ps    |       |
| Low Speed Electrical Specifications            |         |           |                    |                   |       |       |
| Output Logic High (SCL, SDA)                   | VOH     | Vcc-0.5   |                    | Vcc+0.3           | V     |       |
| Output Logic Low (SCL, SDA)                    | VOL     | 0         |                    | 0.4               | V     |       |
| Input Logic High (SCL, SDA)                    | VIH     | Vcc*0.7   |                    | Vcc+0.5           | V     |       |
| Input Logic Low (SCL, SDA)                     | VIL     | -0.3      |                    | Vcc*0.3           | V     |       |
| Output Logic High (IntL)                       | VOH     | Vcc-0.5   |                    | Vcc+0.3           | V     |       |
| Output Logic Low (ModPrsL, IntL)               | VOL     | 0         |                    | 0.4               | V     |       |
| Input Logic High (InitMode, Reset, ModSelL)    | VIH     | 2         |                    | vcc+0.3           | V     |       |
| Input Logic Low (InitMode, Reset, ModSelL)     | VIL     | -0.3      |                    | 0.8               | V     |       |

**Pin Descriptions** 

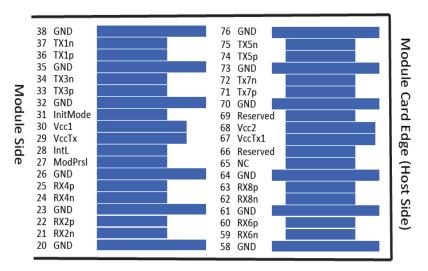
| PIN DE | escriptions |          |                                     |       |
|--------|-------------|----------|-------------------------------------|-------|
| PIN    | Logic       | Symbol   | Description                         | Notes |
| 1      |             | GND      | Ground                              | 1     |
| 2      | CML-I       | Tx2n     | Transmitter Inverted Data Input     |       |
| 3      | CML-I       | Tx2p     | Transmitter Non-Inverted Data Input |       |
| 4      |             | GND      | Ground                              | 1     |
| 5      | CML-I       | Tx4n     | Transmitter Inverted Data Input     |       |
| 6      | CML-I       | Тх4р     | Transmitter Non-Inverted Data Input |       |
| 7      |             | GND      | Ground                              | 1     |
| 8      | LVTTL-I     | ModSelL  | Module Select                       |       |
| 9      | LVTTL-I     | ResetL   | Module Reset                        |       |
| 10     |             | VccRx    | +3.3V Power Supply Receiver         | 2     |
| 11     | LVCMOS-I/O  | SCL      | 2-wire Serial Interface Clock       |       |
| 12     | LVCMOS-I/O  | SDA      | 2-wire Serial Interface Data        |       |
| 13     |             | GND      | Ground                              | 1     |
| 14     | CML-O       | Rx3p     | Receiver Non-Inverted Data Output   |       |
| 15     | CML-O       | Rx3n     | Receiver Inverted Data Output       |       |
| 16     |             | GND      | Ground                              | 1     |
| 17     | CML-O       | Rx1p     | Receiver Non-Inverted Data Output   |       |
| 18     | CML-O       | Rx1n     | Receiver Inverted Data Output       |       |
| 19     |             | GND      | Ground                              | 1     |
| 20     |             | GND      | Ground                              | 1     |
| 21     | CML-O       | Rx2n     | Receiver Inverted Data Output       |       |
| 22     | CML-O       | Rx2p     | Receiver Non-Inverted Data Output   |       |
| 23     |             | GND      | Ground                              | 1     |
| 24     | CML-O       | Rx4n     | Receiver Inverted Data Output       |       |
| 25     | CML-O       | Rx4p     | Receiver Non-Inverted Data Output   |       |
| 26     |             | GND      | Ground                              | 1     |
| 27     | LVTTL-O     | ModPrsL  | Module Present                      |       |
| 28     | LVTTL-O     | IntL     | Interrupt                           |       |
| 29     |             | VccTx    | +3.3V Power Supply Transmitter      | 2     |
| 30     |             | Vcc1     | +3.3V Power Supply                  | 2     |
| 31     | LVTTL-I     | InitMode | Initialization mode                 |       |
| 32     |             | GND      | Ground                              |       |
| 33     | CML-I       | Тх3р     | Transmitter Non-Inverted Data Input |       |
| 34     | CML-I       | Tx3n     | Transmitter Inverted Data Input     |       |
| 35     |             | GND      | Ground                              | 1     |
| 36     | CML-I       | Tx1p     | Transmitter Non-Inverted Data Input |       |
| 37     | CML-I       | Tx1n     | Transmitter Inverted Data Input     |       |
| 38     |             | GND      | Ground                              | 1     |

| PIN |       | Symbol   | Description                         | Notes |
|-----|-------|----------|-------------------------------------|-------|
| 39  |       | GND      | Ground                              | 1     |
| 40  | CML-I | Tx6n     | Transmitter Inverted Data Input     |       |
| 41  | CML-I | Тх6р     | Transmitter Non-Inverted Data Input |       |
| 42  |       | GND      | Ground                              | 1     |
| 43  | CML-I | Tx8n     | Transmitter Inverted Data Input     |       |
| 44  | CML-I | Tx8p     | Transmitter Non-Inverted Data Input |       |
| 45  |       | Reserved |                                     |       |
| 46  |       | VS1      | Module Vendor Specific 1            | 3     |
| 47  |       | VccRx1   | 3.3V Power Supply                   | 2     |
| 48  |       | VS2      | Module Vendor Specific 2            | 3     |
| 49  |       | VS3      | Module Vendor Specific 3            | 3     |
| 50  |       | GND      | Ground                              | 1     |
| 51  | CML-O | Rx7p     | Receiver Non-Inverted Data Output   |       |
| 52  | CML-O | Rx7n     | Receiver Inverted Data Output       |       |
| 53  |       | GND      | Ground                              | 1     |
| 54  | CML-O | Rx5p     | Receiver Non-Inverted Data Output   |       |
| 55  | CML-O | Rx5n     | Receiver Inverted Data Output       |       |
| 56  |       | GND      | Ground                              | 1     |
| 57  |       | GND      | Ground                              | 1     |
| 58  | CML-O | Rx6n     | Receiver Inverted Data Output       |       |
| 59  | CML-O | Rx6p     | Receiver Non-Inverted Data Output   |       |
| 60  |       | GND      | Ground                              | 1     |
| 61  | CML-O | Rx8n     | Receiver Inverted Data Output       |       |
| 62  | CML-O | Rx8p     | Receiver Non-Inverted Data Output   |       |
| 63  |       | GND      | Ground                              | 1     |
| 64  |       | NC       | No Connect                          | 1     |
| 65  |       | Reserved |                                     | 3     |
| 66  |       | VccTx1   | 3.3V Power Supply                   | 2     |
| 67  |       | Vcc2     | 3.3V Power Supply                   | 2     |
| 68  |       | Reserved |                                     | 3     |
| 69  |       | GND      | Ground                              | 1     |
| 70  | CML-I | Тх7р     | Transmitter Non-Inverted Data Input |       |
| 71  | CML-I | Tx7n     | Transmitter Inverted Data Input     |       |
| 72  |       | GND      | Ground                              | 1     |
| 73  | CML-I | Тх5р     | Transmitter Non-Inverted Data Input |       |
| 74  | CML-I | Tx5n     | Transmitter Inverted Data Input     |       |
| 75  |       | GND      | Ground                              | 1     |
| 76  |       | Reserved |                                     |       |

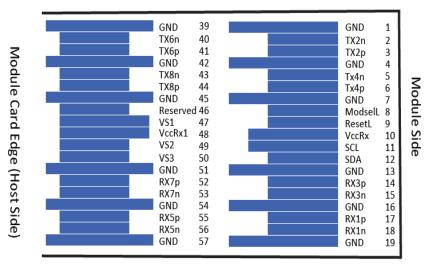
#### Notes:

- 1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- 2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently.
- 3. All vendor specific, Reserved and No Connect pins may be terminated with  $50\Omega$  to ground on the host. Pad 65 (NC) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 K $\Omega$  and less than 100pF

### **Electrical Pin-out Details**

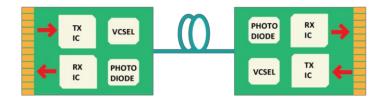


Top side viewed from top



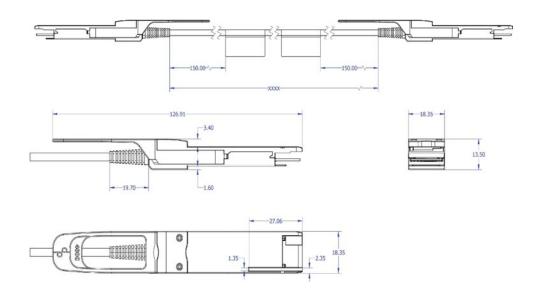
Bottom side viewed from bottom

## **Block Diagram**



## **Mechanical Specifications**

The 400G QSFP-DD AOC mechanical specifications are compliant with the QSFP-DD transceiver module specifications (as defined in QSFP-DD MSA), substituting the MPO receptacle with a fiber optics cable connecting both ends.



### **About AddOn Networks**

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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