QSFPDD-400G-AOC3M-C
MSA and TAA Compliant 400GBase-AOC QSFP-DD to QSFP-DD Active Optical Cable (850nm, MMF, 3m)

Features

- Hot Pluggable QSFP-DD Cable End
- Supports 425Gb/s aggregate bit rate
- Low Power Dissipation, Typ. 7.0W Each End
- 8x50G PAM4 VCSEL/PIN photo detector
- Operating Case Temperature: 0℃~70
- Compliant to QSFP-DD Rev 3.0
- SFF-8636 Management Interface
- SFF-8679: General Electrical
- IEEE 802.3bs: Physical Layer Specifications and Management Parameters
- ROHS-6: Environment Safety

Applications

- 400GBASE-AOC Ethernet

Product Description
This is an MSA compliant 400GBase-AOC QSFP-DD to QSFP-DD active optical cable that operates over active fiber with a maximum reach of 3m. At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' QSFP-DD active optical cables are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

General Characteristics

Parameter	Symbol	Unit	Notes
Module Form Factor	QSFP-DD	As defined by QSFF-DD Rev 3.0	Module Form Factor
Number of Lanes	8 Tx, 8 Rx		
Maximum Aggregate Data Rate	425	Gb/s	
Maximum Power Consumption per End	7	Watts	Varies with output voltage swing and pre-emphasis settings
Standard Cable Lengths	1, 2, 3, 5, 7, 10, 15, 20	Meters	Other lengths may be available upon request
Protocols Supported	Ethernet		
Electrical Interface and Pin-Out	76-pin Edge Connector		Pin-out as defined by QSFF-DD Rev 3.0
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by SFF-8636

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
Maximum Supply Voltage	Vcc	-0.5		3.6	V
Storage Temperature	Tsto	-40		85	°C
Relative Humidity (non-condensing)	RH	0		85	%
Case Operating Temperature	Top	0		70	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit	Notes
Supply Voltage	Vcc	3.14		3.46	V	
Power Consumption	PCon		7		W	
Bit Rate	BR		26.5625		GBd	1
Bit Error Ratio	BER			10^{-12}		2
Center wavelength	λ_C	840		860	nm	3
Number of Lanes		16				
Management Interface		Serial, I2C-based, maximum frequency 400 kHz			°C	4
Logic Input Voltage High	Vih	2		Vcc+0.3	V	
Logic Input Voltage Low	Vil	-0.3		0.8	V	

Notes:

1. Single lane
2. PRBS13Q test pattern is used.

3. As defined by IEEE Std. 802.3bs ™/D3.5
4. As defined by SFF-8636

Force Specification

Parameter	Min	Max	Unit	Notes
QSFP-DD Module Insertion		90	Newton	
QSFP-DD Module Extraction		50	Newton	
QSFP-DD Module Retention	90		Newton	
Insertion and Removal Cycles	50		Cycle	
Cable Outer Diameter	2.9	3.0	mm	
Cable Jacket Material	LSZH			

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes
Transceiver Power Supply Current	I_{CC}		2100		mA	
Transceiver Power On Initialization Time	T_{init}			2000	ms	
Transmitter at TP1a						
AC common-mode output voltage (RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitter disabled)				35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)				880	mV	
Eye symmetry mask width	ESMW		0.22		UI	
Eye height, differential	EH	32			mV	
Differential output return loss		See Eq. 1				1
Common to differential mode conversion return loss		See Eq. 2				2
Differential termination mismatch		10			%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
Receiver at TP4						
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		See Eq. 1				1
Common to differential mode conversion return loss		See Eq. 2				2
Differential termination mismatch		10			%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
DC common mode voltage		-350		2850	mV	

Notes:

1. Eq. 1

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}(f/14) & 8 \leq f < 19 \end{cases} \text{ (dB)}$$

Where f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

2. Eq. 2

$$RLdc(f) \geq \begin{cases} 22 - 20(f/25.78) & 0.01 \leq f < 12.89 \\ 15 - 6(f/25.78) & 12.89 \leq f < 19 \end{cases} \text{ (dB)}$$

Where f is the frequency in GHz, RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

Pin Descriptions

PIN	Symbol	Description	Notes
1	GND	Ground	1
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc RX	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1

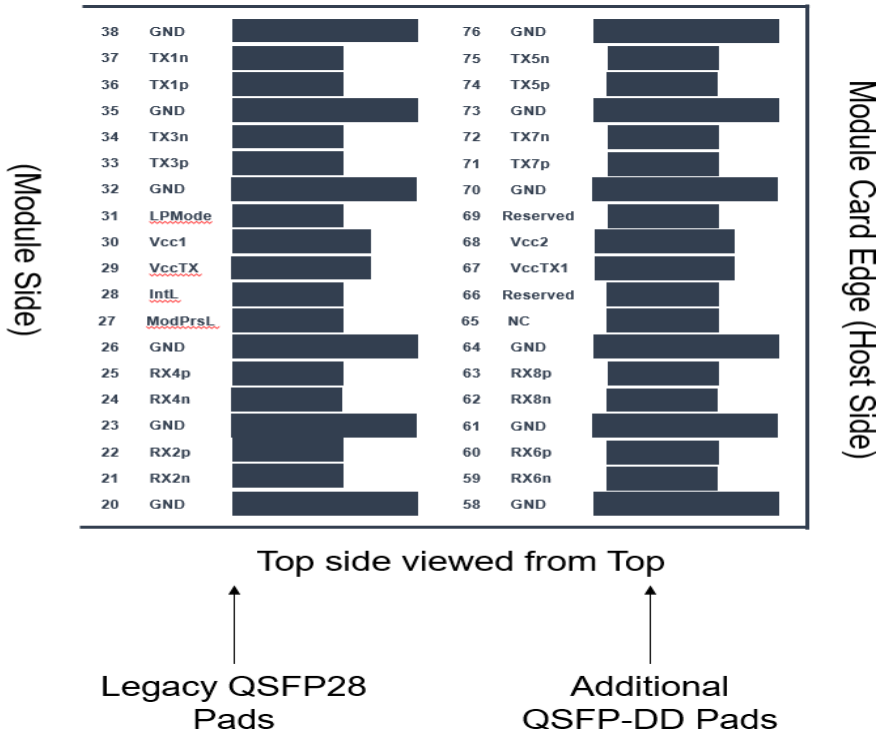
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc TX	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32	GND	Ground	1
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	Reserved	For future use	3
47	VS1	Module Vendor Specific 1	3
48	3.3V Power Supply	2A	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For future use	3

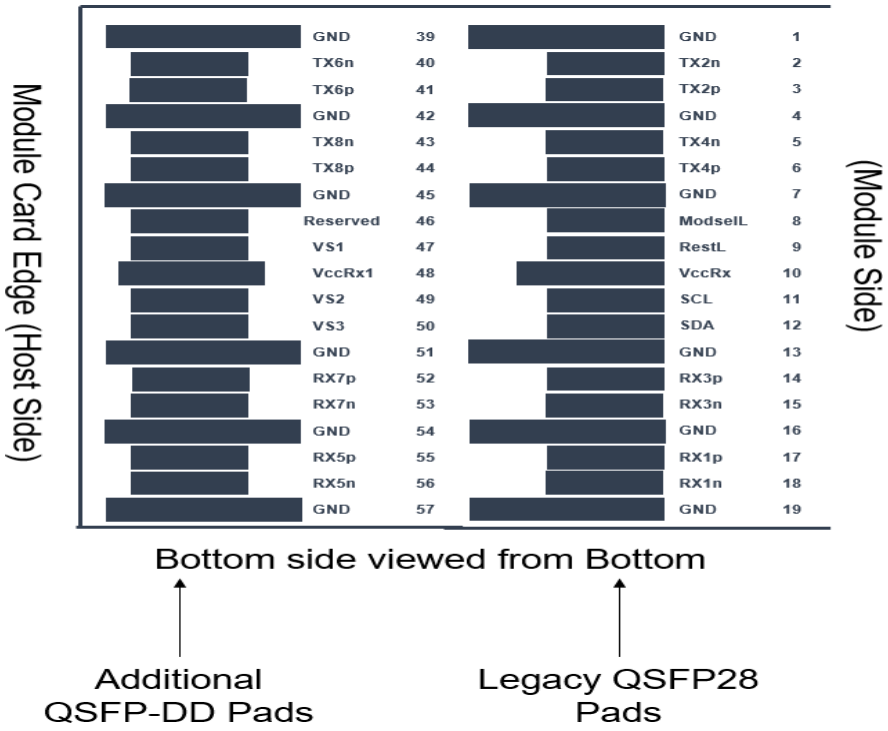
67	VccTx1	3.3V Power Supply	2
68	Vcc2	3.3V Power Supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

Notes:

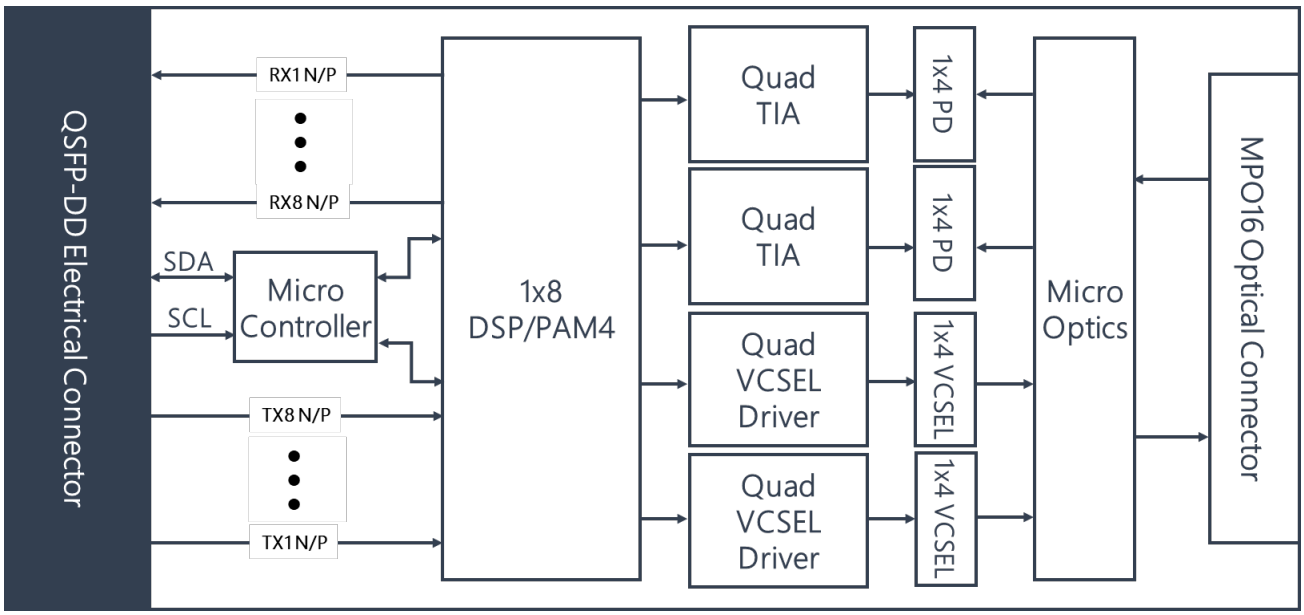
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination.
   The connector Vcc ping are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to grounds on the host. Pad 65 (No connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, the break contact with additional QSFP- DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Electrical Pin-out Details

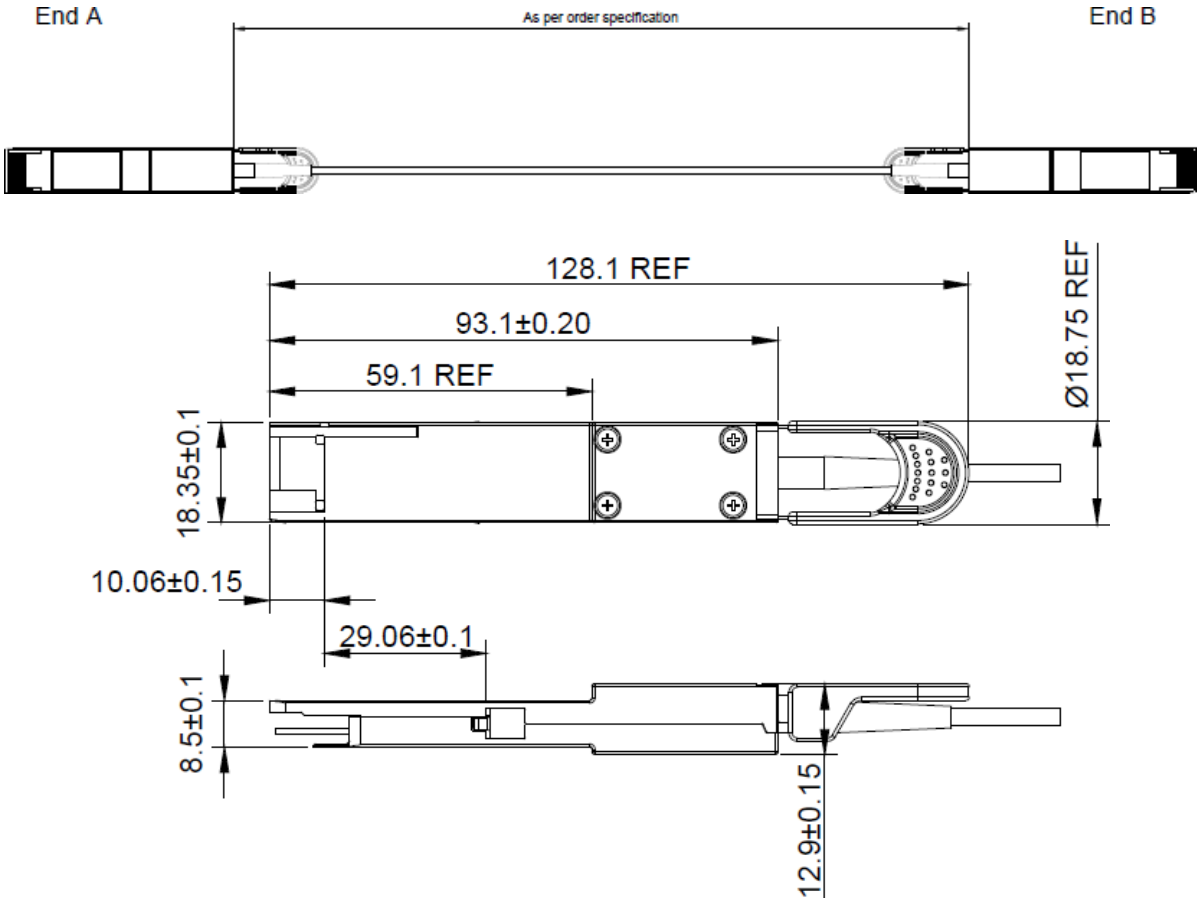




Recommended Host Board Schematic



Mechanical Specifications



Memory Map (compliant QSFP-DD Rev. 3.0)