

SFP-10GB-DW21-H-80-OPC

MSA and TAA 10GBase-DWDM SFP+ Transceiver C-Band 100GHz (SMF, 1560.61nm, 80km, LC, DOM, -40 to 92C)

Features

- SFF-8431 and SFF-8432 Compliance
- Cooled DWDM EML transmitter with TEC
- Supports 9.95Gb/s to 11.3Gb/s bit rates
- APD Receiver
- LC/UPC Duplex optical connector interface
- Power Consumption < 2.8W, depending on temperature
- Single 3.3V power supply
- Hot-pluggable SFP+ footprint
- Operating Temperature: -40C to +92C
- RoHS-6 Complaint



Applications:

- 10x Gigabit Ethernet over DWDM
- 8x/10x Fibre Channel
- Access, Metro and Enterprise

Product Description

This MSA compliant SFP+ transceiver provides 10GBase-DWDM throughput up to 80km over single-mode fiber (SMF) using a wavelength of 1560.61nm via an LC connector. It can operate at temperatures between -40 and 92C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.4
- ESD to the LC Receptacle: compatible with IEC 61000-4-3
- EMI/EMC compatible with FCC Part 15 Subpart B Rules, EN55022:2010
- Laser Eye Safety compatible with FDA 21CFR, EN60950-1& EN (IEC) 60825-1,2
- RoHS compliant with EU RoHS 2.0 directive 2015/863/EU

ITU-T Grid Channel (100GHz Spacing)

Channel	THz	nm	Channel	THz	nm
17*	191.7	1563.86	40	194	1545.32
18	191.8	1563.05	41	194.1	1544.53
19	191.9	1562.23	42	194.2	1543.73
20	192.0	1561.42	43	194.3	1542.94
21	192.1	1560.61	44	194.4	1542.14
22	192.2	1559.79	45	194.5	1541.35
23	192.3	1558.98	46	194.6	1540.56
24	192.4	1558.17	47	194.7	1539.77
25	192.5	1557.36	48	194.8	1538.98
26	192.6	1556.55	49	194.9	1538.19
27	192.7	1555.75	50	195.0	1537.40
28	192.8	1554.94	51	195.1	1536.61
29	192.9	1554.13	52	195.2	1535.82
30	193.0	1553.33	53	195.3	1535.04
31	193.1	1552.52	54	195.4	1534.25
32	193.2	1551.72	55	195.5	1533.47
33	193.3	1550.92	56	195.6	1532.68
34	193.4	1550.12	57	195.7	1531.90
35	193.5	1549.32	58	195.8	1531.12
36	193.6	1548.51	59	195.9	1530.33
37	193.7	1547.72	60	196.0	1529.55
38	193.8	1546.92	61*	196.1	1528.77
39	193.9	1546.12			

*This channel is supported with limited availability.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	VccT, VccR	-0.5		4.0	V	
Storage Temperature	TS	-40		95	°C	
Operating Case Temperature	Tc	-40		92	°C	1
Relative Humidity (non-condensation)	RH	0		85	%	
Data Rate			10.3125		Gbps	
Maximum Range				80	km	

Notes:

1. With Airflows

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Supply Voltage	VccT, VccR	+3.135	3.3	+3.465	V	
Total Power Consumption	PC			2.8	W	With Airflows
Power Supply Noise Tolerance	PSNT			66	mVp-p	10 Hz to 10 MHz
Transmitter differential input voltage	Vp		2.5		V	
Low Speed Signal Electrical Characteristics						
Tx_Fault, Rx_LOS	VOL	-0.3		0.4	V	At 0.7mA
	IOH	-50		37.5	μA	1
Tx_Disable, RS0, RS1	VIL	-0.3		0.8	V	2
	VIH	2.0		VccT + 0.3	V	2

Notes:

1. Measured with a 4.7kΩ load pull up to Vcc_Host
2. Tx Disable has an internal 4.7kΩ to 10kΩ pull up to VccT

High Speed Signal Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Transmitter Input Electrical Specifications at B'						
Tx Input Differential Voltage	VI	190		700	mV	1
Differential Input Resistance	RI	95	100	105	ohm	
Differential Input S-parameter (Note 2)	SDD11			Note 3	dB	0.01to 4.1 GHz
				Note 4	dB	4.1 to 11.1 GHz
Reflected Differential to Common Mode Conversion	SCD11			-10	dB	0.01 to 11.1GHz
Module Receiver Output Electrical Specifications at C'						
Rx Output Differential Voltage	Vo	300		850	mV	1
Termination Mismatch at 1 MHz	ΔZM			5	%	
Single Ended Output Voltage Tolerance		-0.3		4.0	V	
Output AC Common Mode Voltage				7.5	mV	RMS, 5
Differential Output S-parameter	SDD22			Note 6	dB	0.01 to 4.1 GHz
				Note 7	dB	4.1 to 11.1 GHz
Common Mode Output Reflection Coefficient	SCC22			Note 8	dB	0.01 to 2.5 GHz
				-3	dB	2.5 to 11.1 GHz
Rx Output Rise and Fall Time	tr, tf	28			ps	20% to 80%
Rx Output Total Jitter	TJ			0.70	Ulp-p	
Rx Output Deterministic Jitter	DJ			0.42	Ulp-p	

Notes:

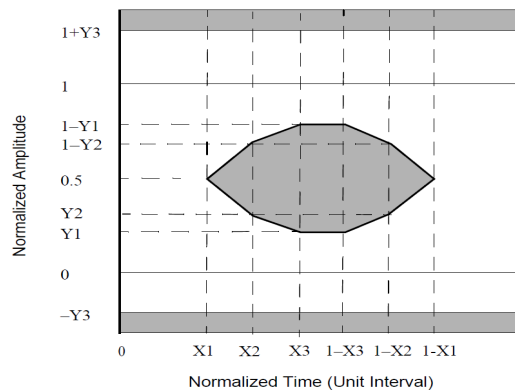
1. Voltage swing for 1G operation is equivalent to voltage swing in 10G operation (SFF-8431 Rev 3.0).
2. Measured at B'' with Host Compliance Board and Module Compliance Board pair.
3. Reflection Coefficient given by equation $SDD11 (dB) < -12 + 2 \times \sqrt{f}$, with f in GHz.
4. Reflection Coefficient given by equation $SDD11 (dB) < -6.3 + 13 \times \log_{10}(f/5.5)$, with f in GHz.
5. The RMS value is measured by calculating the standard deviation of the histogram for one UI of the common mode signal.
6. Reflection Coefficient given by equation $SDD22 (dB) < -12 + 2 \times \sqrt{f}$, with f in GHz.
7. Reflection Coefficient given by equation $SDD22 (dB) < -6.3 + 13 \times \log_{10}(f/5.5)$, with f in GHz.
8. Reflection Coefficient given by equation $SCC22 (dB) < -7 + 1.6 \times f$, with f in GHz.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Peak Wavelength	λ_p	ITU-T 694.1 Grid Wavelength			nm	
Center wavelength spacing		100			GHz	
Spectral Width@-20dB	$\Delta\lambda$ -20dB			0.30	nm	At -20dB
Side Mode Suppression Ratio	SMSR	30.0			dB	
Average Optical Power	Pave	0		+5.0	dBm	
Extinction Ratio	ER	9			dB	@10.3Gb/s, PRBS 2 ³¹ -1
Transmitter and dispersion penalty	DP			3	dB	
Laser Off Power	Poff			-30.0	dBm	
Relative intensity noise	RIN12OMA			-128.0	dB/Hz	
Wavelength Stability after Startup		λ_p - 100		λ_p + 100	pm	
Transmitter Output Eye Mask	IEEE 802.3-2012 Clause 52.9.7					3
Receiver						
Operating Wavelength	λ_o	1260		1600	nm	
Receiver sensitivity (Average)	S			-23.0	dBm	1
Receiver Power (Pave) Overload	OL	-8			dBm	1
Sensitivity (OMA)	SOMA			-21.9	dBm	1
Receiver Reflectance	RR			-27.0	dB	@ λ_o
Loss of signal-Asserted	LOSA	-37.0			dBm	2
Loss of signal-De-asserted	LOSD			-24.0	dBm	2
Loss of signal Hysteresis	LOSD-A	0.5	2.5	5.0	dB	

Notes:

1. Measured with at 10.3125Gb/s, Source ER>8.2dB, PRBS 231-1, BER<1x10⁻¹²
2. Loss of Signal (LOS) detection responds only to OMA and the indicator will respond unpredictably with the application of un-modulated optical.
3. Transmitter Optical Eye Mask Definition



a) SFP+ module compliance points are defined as the following, SFF8431/Chapter3.3.2/Figure14:

- B': SFP+ module transmitter input at the input of the Module Compliance Board.
- C': SFP+ module receiver output at the output of the Module Compliance Board.

Low Speed Signals Timing Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Tx Disable assert time	t_off		100	μs	1
Tx Disable negate time	t_on		2	ms	2
Time to initialize. Cold and warm start time	t_start_up		90	s	3, Cooled type
Rx LOS assert delay	t_los_on		100	μs	4
Rx LOS negate delay	t_los_off		100	μs	5
Tx Fault Assert	Tx_fault_on		1	ms	6
Tx Fault Reset	t_reset	10		μs	7

Notes:

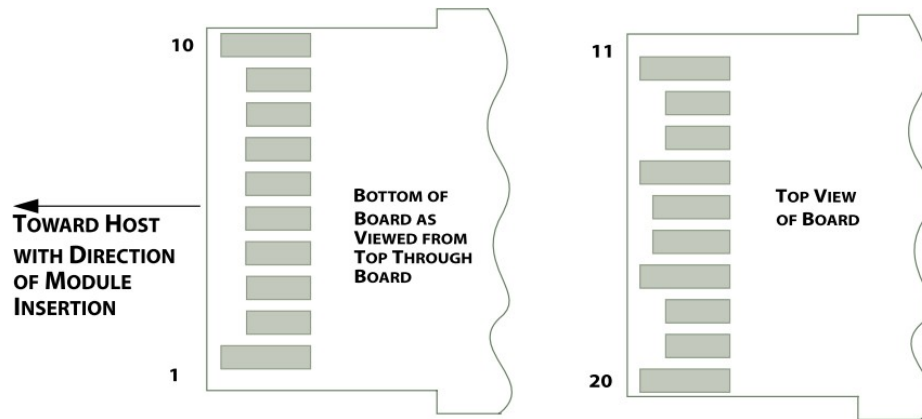
1. Rising edge of Tx_Disable to fall of output signal below 10% of nominal
2. Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery
3. Time from power on or falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal and the Two-Wire interface is available
4. From occurrence of loss of signal to assertion of Rx_LOS
5. From occurrence of presence of signal to negation of Rx_LOS
6. From occurrence of fault to assertion of Tx_Fault
7. Time Tx_Disable must be held high to reset Tx_Fault

Pin Descriptions

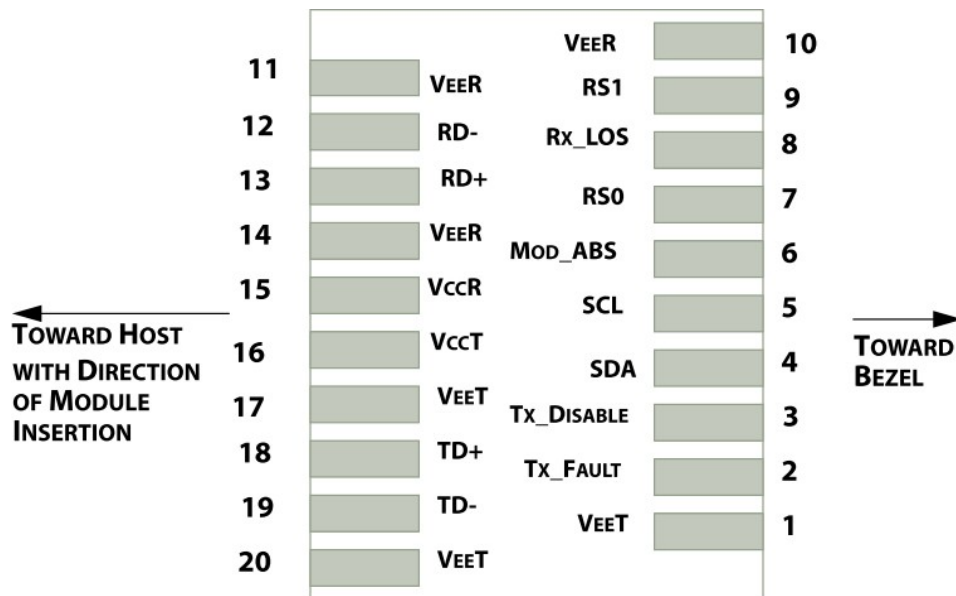
Pin	Symbol	Descriptions	Sequence	Notes
1	VeeT	Transmitter Signal Ground	1 st	
2	Tx_Fault	Transmitter Fault (LVTTTL-O) – High indicates a fault condition	3 rd	1
3	Tx_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3 rd	2
4	SDA	Two Wire Serial Interface Data Line (LVCMOS – I/O) (same as MOD-DEF2 in INF-8074)	3 rd	3
5	SCL	Two Wire Serial Interface Clock Line (LVCMOS – I/O) (same as MOD-DEF1 in INF-8074)	3 rd	3
6	MOD-ABS	Module Absent, (controlled by module)	3 rd	4
7	RS0	Receiver Rate Select 0 - not used (Internally pull-down, 51kohm)	3 rd	
8	RX_LOS	Receiver Loss of Signal Indication (LVTTTL-O)	3 rd	1
9	RS1	Transmitter Rate Select 1 - not used (Internally pull-down, 51kohm)	3 rd	
10	VeeR	Receiver Signal Ground	1 st	
11	VeeR	Receiver Signal Ground	1 st	
12	RD-	Receiver Data Output, Inverted (CML-O)	3 rd	
13	RD+	Receiver Data Output, Non-Inverted (CML-O)	3 rd	
14	VeeR	Receiver Signal Ground	1 st	
15	VccR	Receiver Power + 3.3 V	2 nd	
16	VccT	Transmitter Power + 3.3 V	2 nd	
17	VeeT	Transmitter Signal Ground	1 st	
18	TD+	Transmitter Data Input, Non-Inverted Data (CML-I)	3 rd	
19	TD-	Transmitter Data Input, Inverted (CML-I)	3 rd	
20	VeeT	Transmitter Signal Ground	1 st	

Notes:

1. This is an open drain output that on the host board requires a 4.7k Ω to 10k Ω pull-up resistor to Vcc_Host.
2. This input is internally biased high with a 4.7k Ω to 10k Ω pull-up resistor to VccT.
3. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
4. They must be pulled up with a 4.7k Ω to 10 k Ω resistor on the host board. MOD-ABS is grounded by the module to indicate the module is present.

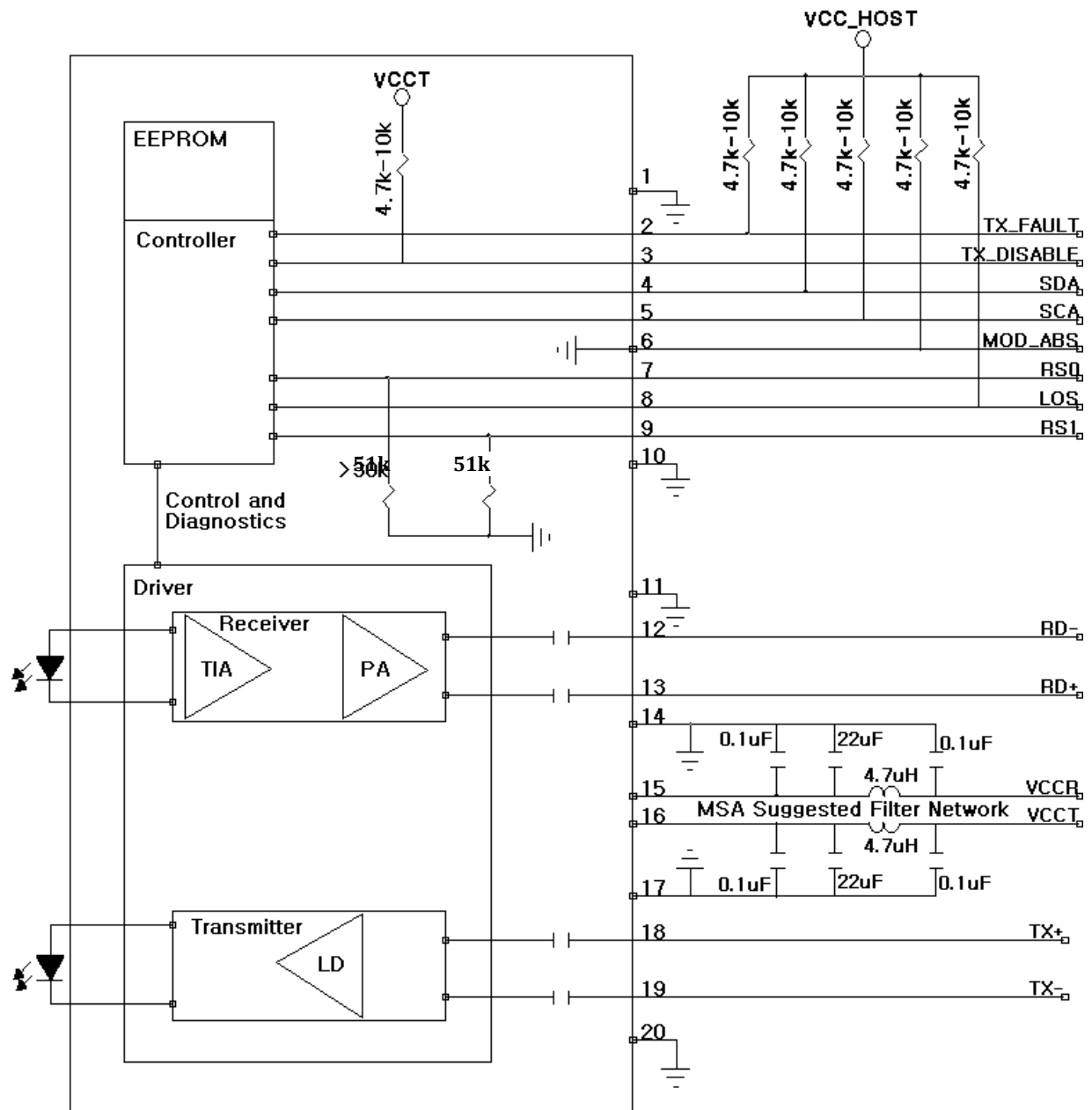


SFP+ Transceiver Electrical Pad Layout



20-pin Host PCB SFP+ pad assignment top view

Recommended Application Schematic



Notes:

1. Tx_Disable: Transmitter Disable, logic high, open drain compatible, 4.7k to 10kohm pull up to Vcc on module.
2. Tx_Fault: Transmitter Fault, logic high, open drain compatible, 4.7k to 10kohm pull up to Vcc on Host.
3. Rx_LOS: Receiver Loss of Signal, logic high, open drain compatible, 4.7k to 10kohm pull up to Vcc on Host.

2-Wire Interface Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Host 2-Wire Vcc	Vcch	3.14	3.46	V	1
SCL and SDA	VOL	0.0	0.8	V	Rp pulled to VccT/R, 2
	VOH	Vcch-0.5	Vcch+0.3	V	
SCL and SDA	VIL	-0.3	VccT*0.3	V	3
	VIH	VccT*0.7	VccT+0.5	V	
Input Current on the SCL and SDA Contacts	II	-10	10	μA	
Capacitance on SCL and SDA contacts	Ci		14	pF	4
Total bus capacitance for SCL and SDA	Cb[5]		100	pF	At 400kHz, 3.0kΩ Rp, max At 100kHz, 8.0kΩ Rp, max
			290	pF	At 400kHz, 1.1kΩ Rp, max At 100kHz, 2.75kΩ Rp, max

Notes:

1. The Host 2-wire Vcc is the voltage used for resistive pull ups for the 2 wire interface
2. Rp is the pull up resistor. Active bus termination may be used by the host in place of a pull up resistor. Pull ups can be connected to any one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R + 0.5 V nor requires the module to sink more than 3.0mA current.
3. These voltages are measured on the other side of the connector to the device under test.
4. Ci is the capacitance looking into the module SCL and SDA contacts.
5. Cb is the total bus capacitance on the SCL or SDA bus.

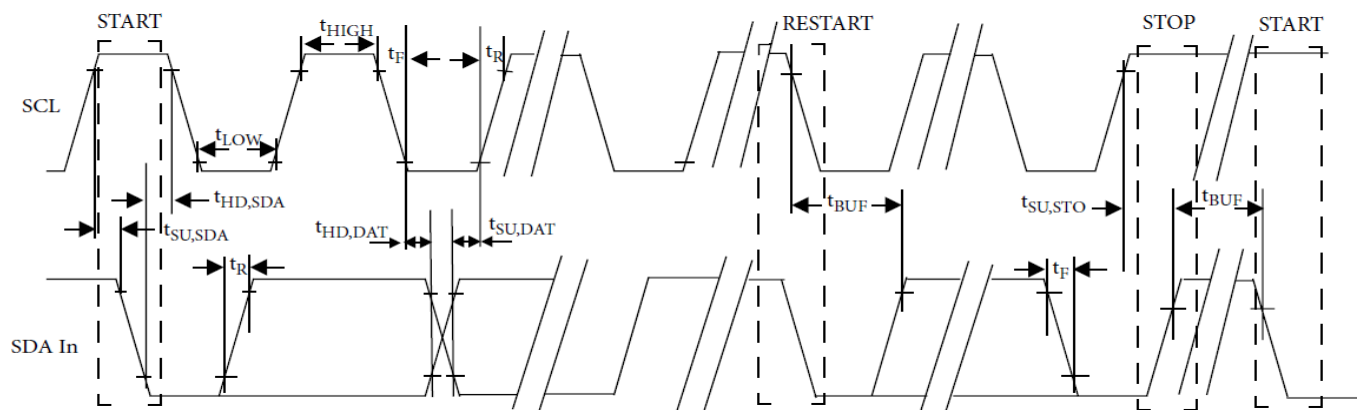
2-Wire Timing Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Clock Frequency	f _{SCL}	0	400	kHz	1
Clock Pulse Width Low	t _{LOW}	1.3		μs	
Clock Pulse Width High	t _{HIGH}	0.6		μs	
Stop to Start Time	t _{BUF}	20		μs	2
Start Hold Time	t _{HD,STA}	0.6		μs	
Start Set-up Time	t _{SU,STA}	0.6		μs	
Data In Hold Time	t _{HD,DAT}	0		μs	
Data In Set-up Time	t _{SU,DAT}	0.1		μs	
Input Rise Time (100kHz)	t _{R,100}		1000	ns	3
Input Rise Time (400kHz)	t _{R,400}		300	ns	3
Input Fall Time (100kHz)	t _{F,100}		300	ns	4
Input Fall Time (400kHz)	t _{F,400}		300	ns	4
Stop Set-up Time	t _{SU,STO}	0.6		μs	
Serial Interface Clock Holdoff "Clock Stretching"	t _{clock_hold}		500	μs	5

Notes:

1. Module shall operate with f_{SCL} up to 100 kHz without requiring clock stretching. The module may clock stretch with f_{SCL} greater than 100 kHz and up to 400 kHz.
2. Between STOP and START and between ACK and Re-START.
3. From (V_{IL},MAX - 0.15) to (V_{IH},MIN + 0.15)
4. From (V_{IH},MIN + 0.15) to (V_{IL},MAX - 0.15)
5. Maximum time the module may hold the SCL line low before continuing with a read or write operation.

2-Wire Bus Timing Diagram



Mechanical Specifications

