

QDD-100GB-DCO-ZRP-OPC

MSA and TAA 100GBase-ZR+ Coherent QSFP-DD Transceiver (SMF, 1528.77nm to 1567.13nm, Open ZR+, LC, DOM)

Features

- QSFP-DD MSA compliant
- Hot pluggable QSFP-DD footprint (Type 2A)
- Supports 100Gbps Payload (Open ZR+)
- Duplex LC Connector
- Tunable C-band Transmitter and Coherent Receivers
- O-FEC (15%) with 11.6dB Net Coding Gain
- 100GAUI-2 (2x 26.5625GBd PAM4) Serial Electrical Interface, RS-FEC (544/514)
- CAUI-4 (4x 25.78125Gbps NRZ) Serial Electrical Interface, RS-FEC (544/528)/No FEC
- Operating Temperature 0 to 70 Celsius
- RoHS Compliant and Lead-free



Applications:

- 100GBase Ethernet
- Access and Enterprise

Product Description

This MSA compliant QSFP-DD transceiver provides 100GBase-ZR+ Open ZR+ throughput over single-mode fiber (SMF) using a wavelength of 1528.77nm to 1567.13nm via an LC connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.218	3.3	3.465	V	
Storage Temperature	Tstg	-40		85	°C	
Case Operating Temperature	Tc	0		70	°C	
Relative Humidity (Non-Condensing)	RH			85	%	
Optical Receiver Overload				4	dBm	1
Supported Host Signal Types			103.125		Gbps	2
Line Baud Rate			30.07		GBd	3

Notes:

1. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used.
2. As per IEEE 802.3-2012.
3. 100G DP-QPSK, O-FEC.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.218	3.3	3.465	V	
Power Supply Current	Icc			6	A	
Power Consumption	PD			16.5	W	
Power Consumption	PD			1.5	W	1

Notes:

1. Low-power mode.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Average Output Power	P _o	-6	-4.5	-2	dBm	1, 2
Laser Linewidth				300	kHz	
Transmitter VOA Dynamic Range		10			dB	3
Output Power Stability		-1		1	dB	
In-Band OSNR		35			dB/0.1nm	
Out-of-Band OSNR		35			dB/0.1nm	
Frequency Range		191.275		196.125	THz	4
Centre Frequency		$\nu_T - 1.5$	ν_T	$\nu_T + 1.5$	GHz	5
Channel Spacing		6.25			GHz	
Centre Wavelength Range	$T\lambda$	1528.58		1567.34	nm	
Centre Wavelength	$T\lambda$	$\lambda_T - 15$	λ_T	$\lambda_T + 15$	pm	
Receiver						
Receiver Operating Wavelength	$R\lambda$	1528.58		1567.34	nm	
Receiver Sensitivity	S			-32	dBm	6
Receiver Overload	P _{OL}	4			dBm	7
Receiver Input Power Range		-20		4	dBm	8
Extended Receiver Input Power Range		-25		4	dBm	9
Acquisition Range		-3.6		3.6	GHz	10
Upstream Tx Linewidth				1000	kHz	
OSNR Tolerance			14	15.5	dB	11
Crosstalk Tolerance				17	dB	12
Chromatic Dispersion Tolerance				5000	ps/nm	13

Notes:

1. Output power coupled into a 9/125μm single-mode fiber.
2. The output power is adjustable in steps of 0.1dB within the specified wavelength range.
3. With Tx VOA attenuation is set to minimum.
4. Per ITU-T G.694.1 DWDM grid definition.
5. Applies also to LO.
6. Minimum input power needed to achieve post-FEC BER≤10⁻¹⁵, 100G DP-QPSK, and OSNR>35dB.
7. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used.
8. An input power in this range guarantees optimum OSNR performance.
9. With ≤1dB OSNR tolerance degradation.
10. Frequency offset between received carrier and LO.
11. At optimum input power range.

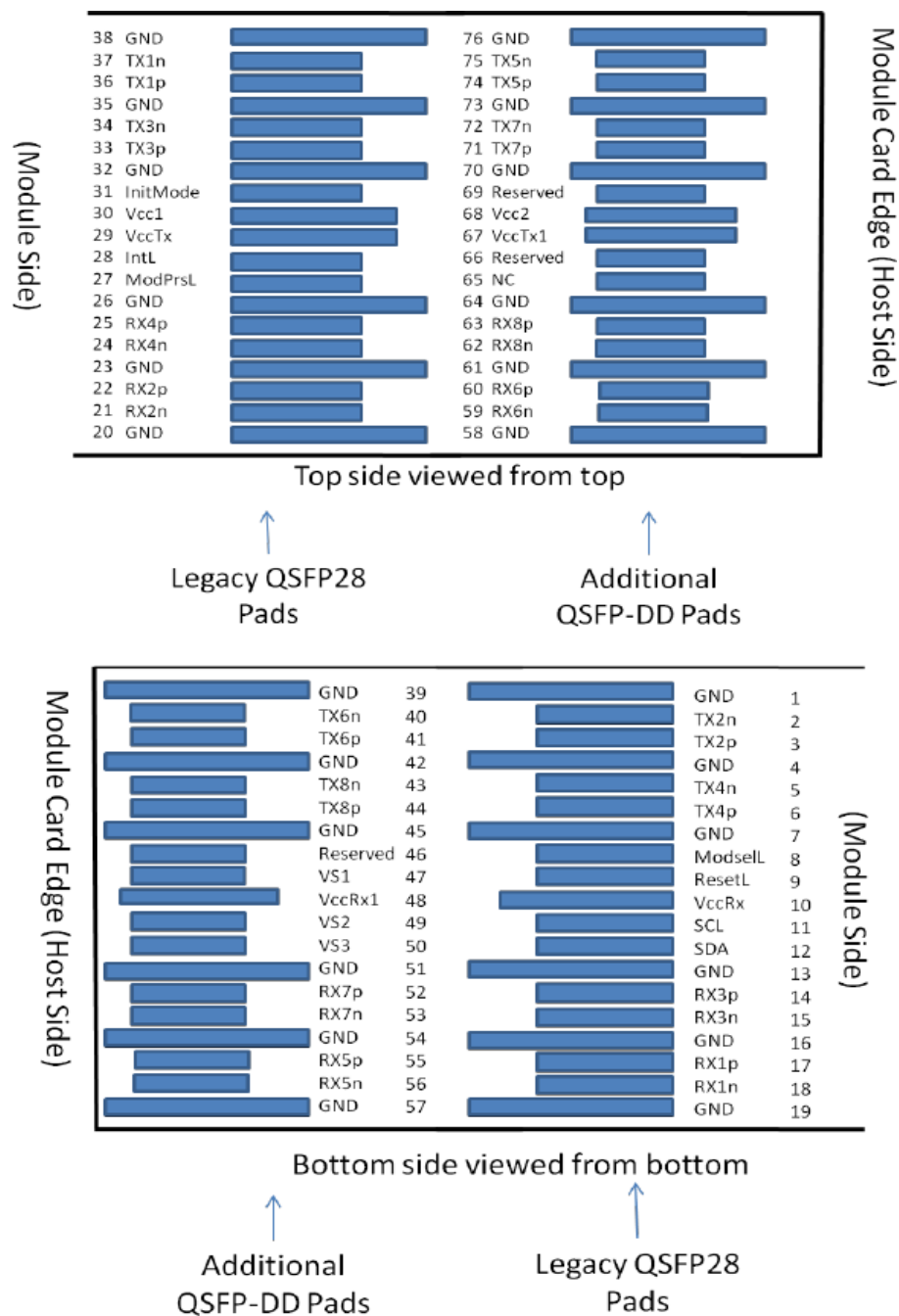
12. Ratio of accumulated crosstalk channels to signal power.
13. Less than 0.5dB receiver sensitivity penalty compared to OSNR>35dB.

Pin Descriptions

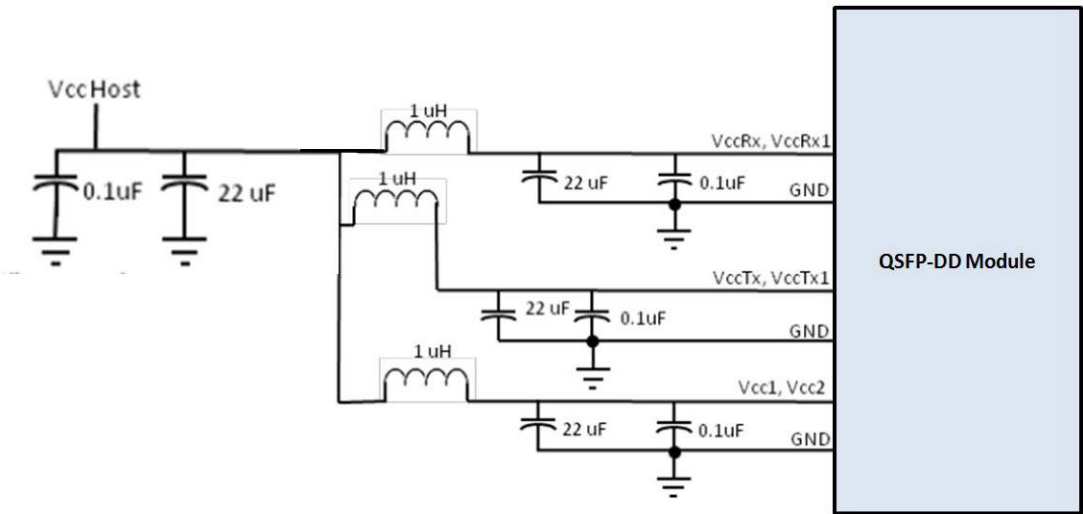
Pin	Logic	Symbol	Name/Description	Plug Sequence
1		GND	Module Ground.	1B
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3B
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3B
4		GND	Module Ground.	1B
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3B
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3B
7		GND	Module Ground.	1B
8	LVTTL-I	ModSelL	Module Select.	3B
9	LVTTL-I	ResetL	Module Reset.	3B
10		VccRx	+3.3V Receiver Power Supply.	2B
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3B
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3B
13		GND	Module Ground.	1B
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3B
15	CML-O	Rx3-	Receiver Inverted Data Output.	3B
16		GND	Module Ground.	1B
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3B
18	CML-O	Rx1-	Receiver Inverted Data Output.	3B
19		GND	Module Ground.	1B
20		GND	Module Ground.	1B
21	CML-O	Rx2-	Receiver Inverted Data Output.	3B
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3B
23		GND	Module Ground.	1B
24	CML-O	Rx4-	Receiver Inverted Data Output.	3B
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3B
26		GND	Module Ground.	1B
27	LVTTL-O	ModPrsL	Module Present.	3B
28	LVTTL-O	IntL	Interrupt.	3B
29		VccTx	+3.3V Transmitter Power Supply.	2B
30		Vcc1	+3.3V Power Supply.	2B
31	LVTTL-I	InitMode	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	3B
32		GND	Module Ground.	1B
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3B
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3B
35		GND	Module Ground.	1B
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3B

37	CML-I	Tx1-	Transmitter Inverted Data Input.	3B
38		GND	Module Ground.	1B
39		GND	Module Ground.	1A
40	CML-I	Tx6-	Transmitter Inverted Data Input.	3A
41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	3A
42		GND	Module Ground.	1A
43	CML-I	Tx8-	Transmitter Inverted Data Input.	3A
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	3A
45		GND	Module Ground.	1A
46		Reserved	For Future Use.	3A
47		VS1	Module Vendor-Specific 1.	3A
48		VccRx1	+3.3V Receiver Power Supply.	2A
49		VS2	Module Vendor-Specific 2.	3A
50		VS3	Module Vendor-Specific 3.	3A
51		GND	Module Ground.	1A
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	3A
53	CML-O	Rx7-	Receiver Inverted Data Output.	3A
54		GND	Module Ground.	1A
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	3A
56	CML-O	Rx5-	Receiver Inverted Data Output.	3A
57		GND	Module Ground.	1A
58		GND	Module Ground.	1A
59	CML-O	Rx6-	Receiver Inverted Data Output.	3A
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	3A
61		GND	Module Ground.	1A
62	CML-O	Rx8-	Receiver Inverted Data Output.	3A
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	3A
67		GND	Module Ground.	1A
68		NC	Not Connected.	3A
69		Reserved	For Future Use.	3A
70		VccTx1	+3.3V Transmitter Power Supply.	2A
71		Vcc2	+3.3V Power Supply.	2A
72		Reserved	For Future Use.	3A
73		GND	Module Ground.	1A
74	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	3A
75	CML-I	Tx7-	Transmitter Inverted Data Input.	3A
76		GND	Module Ground.	1A

Electrical Pad Layout



Recommended Power Supply Filter



Mechanical Specifications

