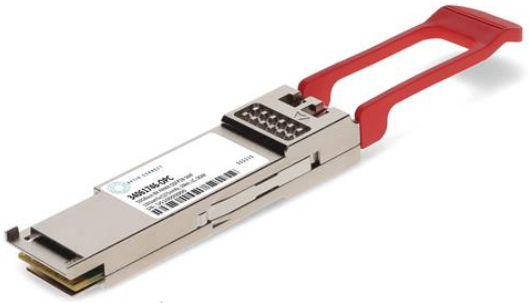
34061746-OPC

Huawei® 34061746 Compatible TAA 50GBase-BX PAM4 QSFP28 Transceiver (SMF, 1331nmTx/1271nmRx, 10km, LC, DOM, 0 to 70C)

Features

- Compliant with QSFP+ MSA
- 2-wire management interface
- Single LC connector for BIDI
- Single 3.3V Supply Voltage
- Power dissipation < 3.5W
- Maximum link length of 10km on Single Mode Fiber (SMF)
- IEEE STD 803.3cp Compliant
- 50GAUI-2 Serial Electrical Interface support
- Optical 26.56GBaud PAM4
- Hot-pluggable
- Operating Temperature: 0C to 70C
- RoHS-6 Compliant



Applications:

- 50GBase Ethernet
- Access and Enterprise

Product Description

This Huawei® 34061746 compatible QSFP28 transceiver provides 50GBase-BX throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1331nmTx/1271nmRx via an LC connector. It is guaranteed to be 100% compatible with the equivalent Huawei® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open internaltional trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

Rev. 081125

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Maximum Supply Voltage	Vcc	-0.5		4	V
Storage Temperature	TS	-40		85	°C
Operating Case Temperature	TC	0		70	°C
Relative Humidity (non-condensing)	RH	5		85	%
Receiver Damage Threshold	PT	5.2			dBm
ESD Sensitivity				±500 for High-speed lines ±2kV for others	V
Data Rate (Electrical)	DRe		26.5625		Gbps
Data Rate (Optical)	DRo		53.125		Gbps
Transmission Distance		2		10000	m

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Dissipation	PD			3.5	W	
Transmitter						
Input Differential Impedance			100		Ω	
Differential Data Input Swing				900	mV	
Receiver						
Differential Data Output Swing				900	mV	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Rate (range)		26.5625 ± 100 ppm			GBd	
Wavelength (range)	λc	1324.5	1331	1337.5	nm	
Module Format		PAM4				
Average Launch Power	PAVG	-4.5		4.2	dBm	1
Optical modulation amplitude (OMA)	POMA	-1.5		4	dBm	2
Side-Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5			dB	
Launch power in OMA minus TDECQ (min)		-2.9			dB	
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	TDECQ			3.2	dB	
Average launch power of OFF transmitter (max)				-30	dBm	
RIN OMA (max)				-132	dB/Hz	
Optical return loss tolerance (max)	ORL			15.6	dB	
Transmitter Reflectance (max)				-26	dB	3
Receiver						
Signaling rate (range)		26.5625 ± 100 ppm			GBd	
Modulation format		PAM4				
Wavelength (range)	λc	1264.5	1271	1277.5	nm	
Damage threshold		5.2			dBm	4
Average receive power		-10.8		4.2	dBm	5
Receiver Sensitivity (OMA)	RS			-8.9	dBm	6
Stressed Receiver Sensitivity (OMA)	RSS			-6.6	dBm	7
Receiver Reflectance				-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-Assert	LOSD			-11	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Condition of Stressed Sensitivity Test						
Stressed Eye Closure	SECQ		3.2		dB	8

Notes:

1. Min average power is informative and not the principal indicator of signal strength. Power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ <1.4dB, the OMAouter (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.

4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
5. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMAouter) (max) is informative and is defined for a transmitter with a value of SECQ up to 3.2 dB for 50GBASE-LR. The BER is below 2.4E-5 before FEC at the begin of life and below 2.4E-4 before FEC at the end of life.
7. Measured with conformance test signal at TP3 (see 139.7.10) for the BER specified in 139.1.1 (IEEE802.3cd).
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver

Control and Status I/O Timing Requirement

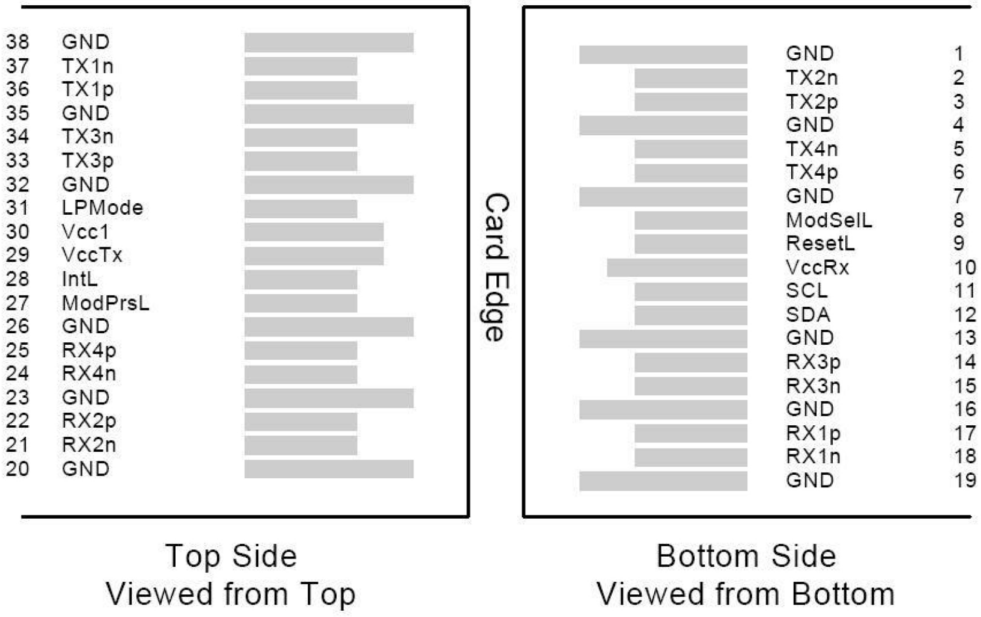
Item	Symbol	Min.	Typ.	Max.	Unit	Notes
Initialization time	t_init			2000	ms	1
Reset Init Assert Time	t_reset_init	10			us	2
Serial Bus Hardware Ready Time	t_serial			2000	ms	3
Reset Assert Time	t_reset			2000	ms	4
LPMode Assert Time	ton_LPMode			100	ms	5
LPMode Deassert Time	Toff_LPMode			300	ms	6
IntL Assert Time	ton_IntL			200	ms	7
IntL Deassert Time	toff_IntL			500	us	8
Rx LOS Assert Time	ton_los			100	ms	9
Tx Fault Assert Time	ton_Txfault			200	ms	10
Flag Assert Time	ton_flag			200	ms	11
Mask Assert Time	ton_mask			100	ms	12
Mask Deassert Time	toff_mask			100	ms	13
Power_override or Power_set Assert Time	ton_Pdown			100	ms	14
Power_override or Power_set Deassert Time	toff_Pdown			300	ms	15

Notes:

1. Time from power on, hot plug or rising edge of reset until the module is fully functional. This time does not apply to non-Power level 0 modules in Low Power State.
2. A Reset is generated by a low level longer than t_reset_init present on the ResetL input.
3. Time from power on until the module responds to data transmission over the two wire serial bus.
4. Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption reaches Power Level 1.

5. Time from deassertion of LPMode (Vin:LPMode = Vil) until module is fully functional.
6. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
7. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes De-Assert times for Rx LOS, Tx Fault and other flag bits.
8. Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
9. Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted.
10. Time from condition triggering flag to associated flag bit set (value = 1b) and IntL asserted.
11. Time from mask bit set (value = 1b) until associated IntL assertion is inhibited.
12. Time from mask bit cleared (value = 0b) until associated IntL operation resumes.
13. Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification.
14. Time from P_Down bit set (value = 1b) until module power consumption reaches Power Level 1.
15. Time from P_Down bit cleared (value = 0b) until module is fully functional.

Electrical Pin-out Details



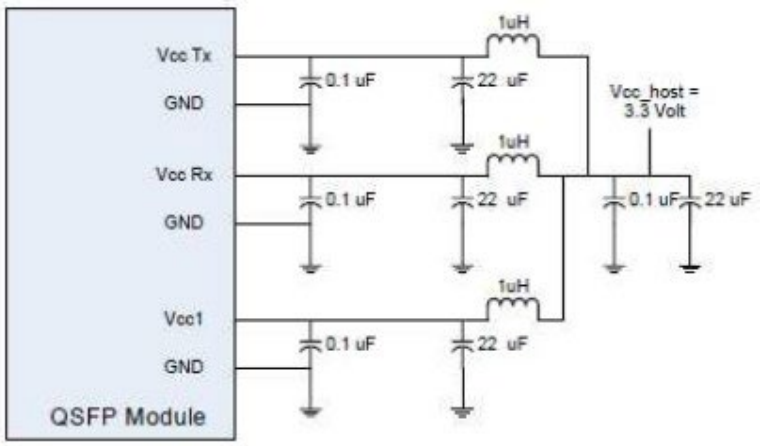
Pin Descriptions

Pin	Logic	Symbol	Descriptions	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	3
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3	3
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	3
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/Rx LOS	Interrupt/Rx LOS	3	4
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power Mode/Tx disable	3	4
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	3
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

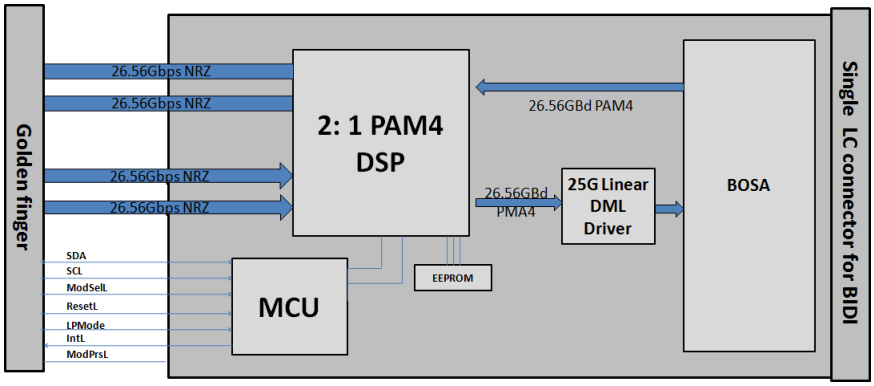
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.
3. Not used.
4. Dual function pin as specified into SFF-8679.

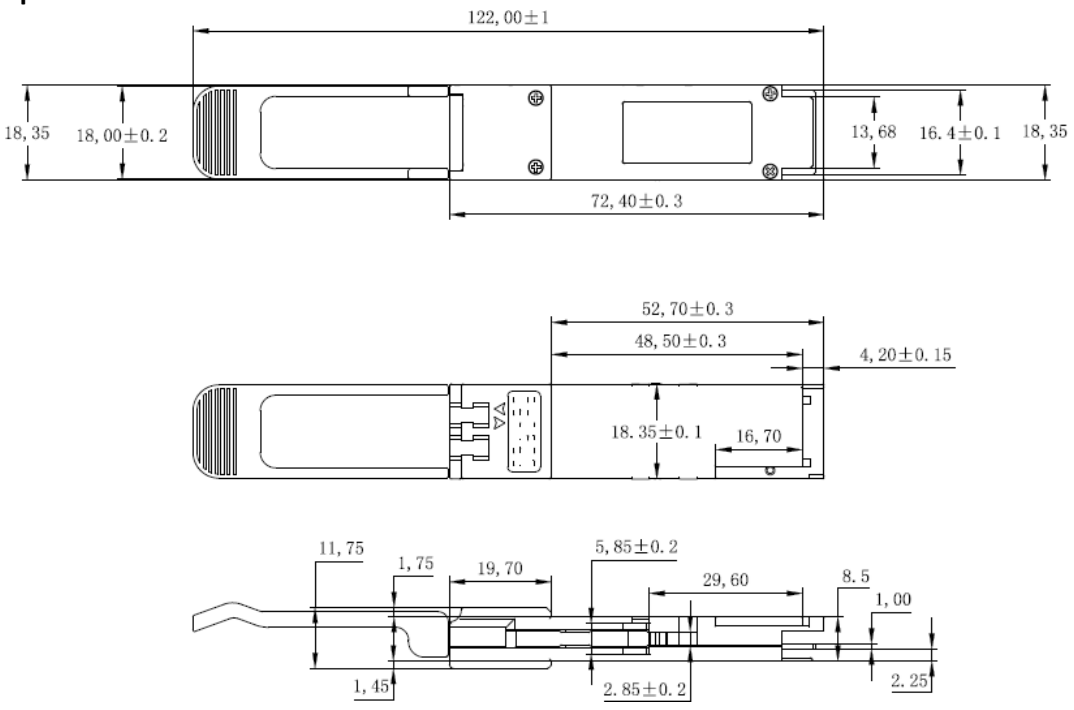
Recommended Interface Circuit



Transceiver Block Diagram



Mechanical Specifications



Digital Diagnostics

Parameter	Symbol	Min	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	℃	
Supply voltage monitor absolute error	DMI _VCC	-5	5	%	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3	3	dB	
Channel Bias current monitor	DMI_Ibias	-10	10	%	
Channel TX power monitor absolute error	DMI_TX	-3	3	dB	

OptioConnect
Innovation for the Future of High-Speed Networking

Who We Are
OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do
At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design
Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team
Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

Our Mission
To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect
Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.
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