QDD-200G-2LR4-OPC

Arista Networks® QDD-200G-2LR4 Compatible TAA 2x100GBase-LR4 QSFP28-DD Transceiver (SMF, 1295nm to 1309nm, 10km, 2xCS, DOM)

Features

- Supports 206Gbps
- Dual CS Connector
- 8x25G electrical interface
- Single-mode Fiber
- 8x25Gbps DFB-based LAN-WDM transmitter
- PIN and TIA array on the receiver side
- Commercial Temperature 0 to 70 Celsius
- I2C interface with integrated Digital Diagnostic Monitoring
- RoHS-6 compliant and Lead Free
- Single +3.3V power supply and power dissipation

Applications:

- 200GBase Ethernet

Product Description

This Arista Networks® QDD-200G-2LR4 compatible QSFP28-DD transceiver provides 2x100GBase-LR4 throughput up to 10km over single-mode fiber (SMF) using a wavelength of 1295nm to 1309nm via a 2xCS connector. It can operate at temperatures between 0 and 70C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Arista Networks®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Maximum Supply Voltage	Vcc	-0.5		3.6	V
Storage Temperature	TS	-40		85	°C
Operating Case Temperature	Tc	0	25	70	°C
Relative Humidity (non-condensing)	RH	5		85	%
Receiver Damage Threshold, per lane	Rxdmg	5.5			dBm

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Dissipation	Pd			8	W	
Instantaneous peak current	Icc_ip			3200	mA	
Sustained peak current	Icc_sp			2640	mA	
Steady state current	Icc			2308	mA	
Transmitter						
Differential data input swing per lane				900	mV_{p-p}	
Input Impedance (Differential)	Zin			10	%	
Stressed Input Parameters						
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13				
Eye height		95			mV	
DC common mode voltage		-350		2850	mV	
Receiver						
Differential output amplitude		200		900	mV_{p-p}	
Output Impedance (Differential)	Zout			10	%	
Output Rise/Fall Time	t_r/t_f	12			ps	20%~80%
Eye width		0.57			UI	
Eye height differential		228			mV	
Vertical eye closure				5.5	dB	

Optical Characteristics

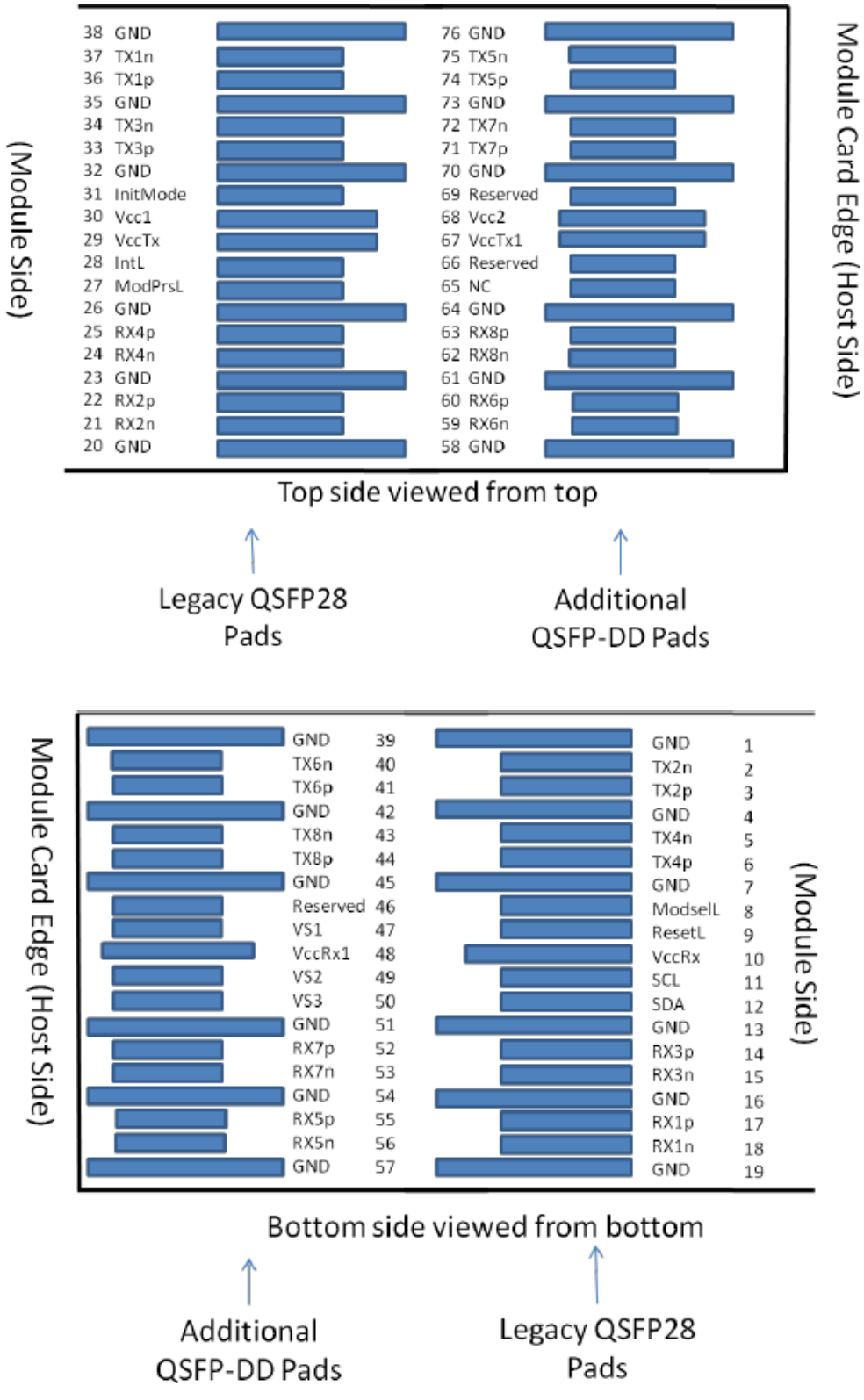
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Signaling Speed per Lane	BRAVE		25.78		Gbps	
Data Rate Variation		-100		+100	ppm	
Lane_1/5 Center Wavelength	λ_{C1}	1294.53	1295.56	1296.59	nm	
Lane_2/6 Center Wavelength	λ_{C2}	1299.02	1300.05	1301.09	nm	
Lane_3/7 Center Wavelength	λ_{C3}	1303.54	1304.58	1305.63	nm	
Lane_4/8 Center Wavelength	λ_{C4}	1308.09	1309.14	1310.19	nm	
Total Average Output Power each optical interface	Po			10.5	dBm	
Average Launch Power each Lane	Peach	-4.3		4.5	dBm	1
Transmit OMA each Lane	TxOMA	-1.3		4.5	dBm	2
Launch power in OMA minus TDP, each lane	OMA-TDP	-2.3			dBm	
Transmitter and Dispersion Penalty per Lane	TDP			2.2	dB	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	3
Extinction Ratio	ER	4			dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				4
Receiver						
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps	
Data Rate Variation		-100		+100	ppm	
Damage threshold	Rxdmg	5.5			dBm	
Lane_1/5 Center Wavelength	λ_{C1}	1294.53	1295.56	1296.59	nm	
Lane_2/6 Center Wavelength	λ_{C2}	1299.02	1300.05	1301.09	nm	
Lane_3/7 Center Wavelength	λ_{C3}	1303.54	1304.58	1305.63	nm	
Lane_4/8 Center Wavelength	λ_{C4}	1308.09	1309.14	1310.19	nm	
Average receive power	Rxpow	-10.6		4.5	dBm	5
Receive Power (OMA) per Lane	RxOMA			4.5	dBm	
Unstressed Receiver Sensitivity (OMA) per Lane	Rxsens			-8.6	dBm	6
Stressed Receiver Sensitivity (OMA) per Lane	RX_{SRS}			-6.8	dBm	7
Optical Return Loss	ORL			-26	dB	
Conditions of Stress Receiver Sensitivity Test						
Vertical Eye Closure Penalty	VECP	1.8			dB	8
Stressed J2 Jitter	J2	0.3			UI	8

Stressed J9 Jitter	J9	0.47			UI	8
LOS Assert	LOSA	-25			dBm	
LOS De-Assert	LOSD			-12	dBm	
LOS Hysteresis		0.5			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDP < 1.0dB, the OMA (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Hit ratio of $5x10^{-5}$
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMA), each lane (max) is informative.
7. Measured with conformance test signal at TP3 for BER =$10^{-12.}$
8. Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

QSFP-DD Transceiver Electrical Pad Layout



Pin Descriptions

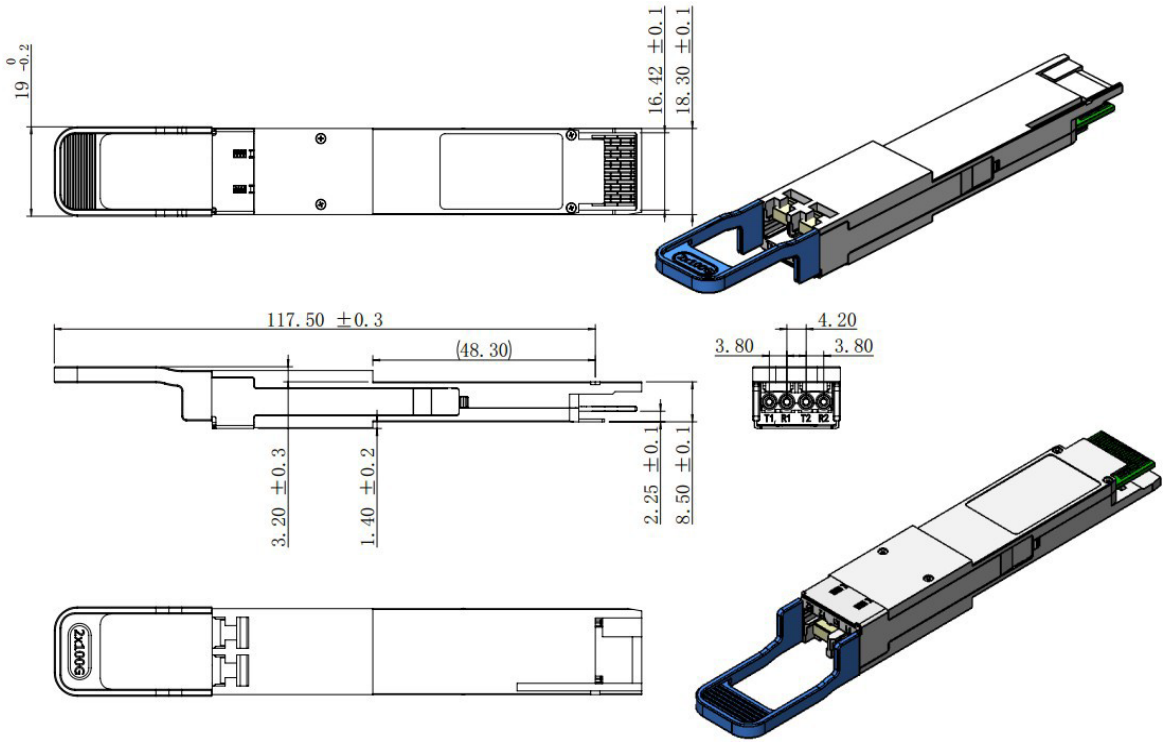
Pin	Logic	Symbol	Name/Descriptions	Plug Sequence [4]	Ref.
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	

38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Specifications



OptioConnect
Innovation for the Future of High-Speed Networking

Who We Are
OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do
At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design
Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team
Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

Our Mission
To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect
Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.
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