OSFP-QDD-400GB-AR-PDAC2-5M-C

Arista Networks® Compatible TAA 400GBase-CU OSFP to QSFP-DD Direct Attach Cable (Passive Twinax, 2.5m)

Features:

- OSFP Module Compliant to OSFP MSA
- QSFP-DD Module Compliant to QSFP-DD MSA
- Transmission Data Rate up to 53.125Gbps Per Channel
- Enable 400Gbps Transmission
- Built-In EEPROM Functions
- Operating Temperature Range: 0 to 70 Celsius
- RoHS Compliant and Lead-Free

Applications:

- 400GBase

Product Description

This is an Arista Networks® compatible 400GBase-CU OSFP to QSFP-DD direct attach cable that operates over passive copper with a maximum reach of 2.5m (8.3ft). It has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This direct attach cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Rev. 011926

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Storage Temperature	Tstg	-40		85	℃
Operating Case Temperature	Tc	0		70	℃
Relative Humidity	RH	5		85	%
Data Rate			400		Gbps

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resistance	Rcon			3	Ω
Insulation Resistance	Rins			10	MΩ
Raw Cable Impedance	Zca	95	100	110	Ω
Mated Connector Impedance	Zmated	85	100	110	Ω
Insertion Loss @13.28GHz	SDD21	8		17.16	dB
Return Loss	SDD11/22	$\text{Return_loss}(f) \geq \begin{cases} 16.5-2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{cases}$			dB
Differential to Common-Mode Return Loss	SCD11/22	$\text{Return_loss}(f) \geq \begin{cases} 22-(20/25.78)f & 0.01 \leq f < 12.89 \\ 15-(6/25.78)f & 12.89 \leq f \leq 19 \end{cases}$			dB
Differential to Common-Mode Conversion Loss	SCD21-SDD21	$\text{Conversion_loss}(f) - \text{IL}(f) \geq \begin{cases} 10 & 0.01 \leq f < 12.89 \\ 27-(29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{cases}$			dB
Minimum COM	COM	3			dB

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Length	L		2.5		M
Wire Gauge			27		AWG
Jacket Material		Plastic Braided Mesh, Silver Gray			

Pin Descriptions for OSFP

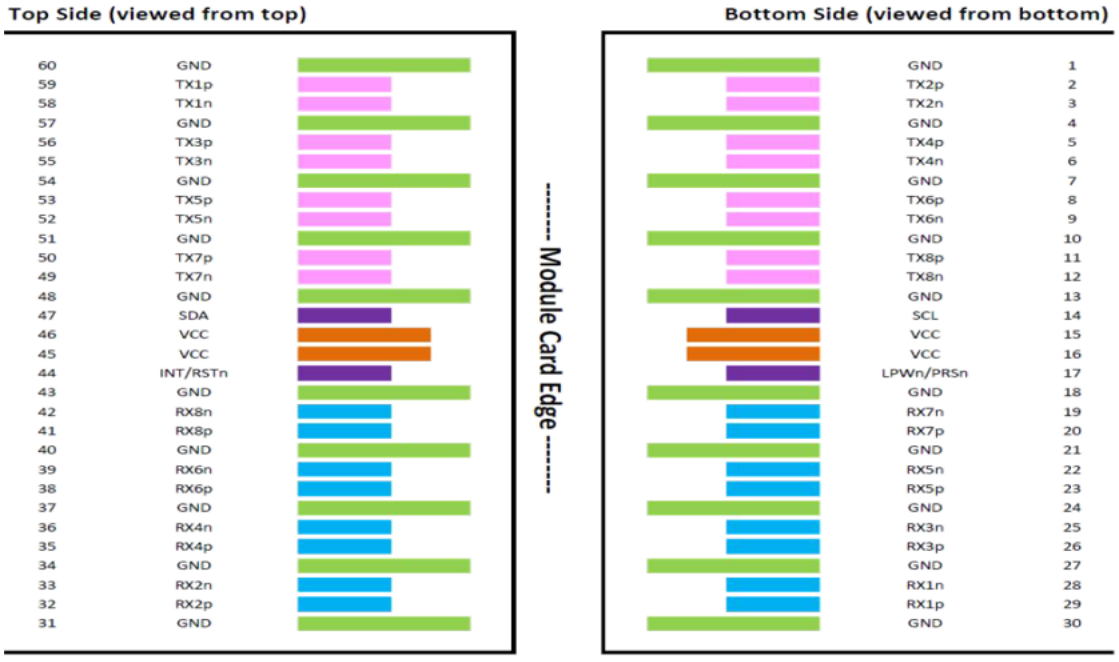
Pin	Symbol	Name/Description	Logic	Plug Sequence	Direction	Notes
1	GND	Module Ground.		1		
2	Tx2+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
3	Tx2-	Transmitter Data Inverted.	CML-I	3	Input from Host	
4	GND	Module Ground.		1		
5	Tx4+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
6	Tx4-	Transmitter Data Inverted.	CML-I	3	Input from Host	
7	GND	Module Ground.		1		
8	Tx6+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
9	Tx6-	Transmitter Data Inverted.	CML-I	3	Input from Host	
10	GND	Module Ground.		1		
11	Tx8+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
12	Tx8-	Transmitter Data Inverted.	CML-I	3	Input from Host	
13	GND	Module Ground.		1		
14	SCL	2-Wire Serial Interface Clock.	LVCMOS-I/O	3	Bi-Directional	1
15	Vcc	+3.3V Power.		2	Power from Host	
16	Vcc	+3.3V Power.		2	Power from Host	
17	LPWn/PRSn	Low-Power Mode/Module Present.	Multi-Level	3	Bi-Directional	2
18	GND	Module Ground.		1		
19	Rx7-	Receiver Data Inverted.	CML-O	3	Output to Host	
20	Rx7+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
21	GND	Module Ground.		1		
22	Rx5-	Receiver Data Inverted.	CML-O	3	Output to Host	
23	Rx5+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
24	GND	Module Ground.		1		
25	Rx3-	Receiver Data Inverted.	CML-O	3	Output to Host	
26	Rx3+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
27	GND	Module Ground.		1		
28	Rx1-	Receiver Data Inverted.	CML-O	3	Output to Host	
29	Rx1+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
30	GND	Module Ground.		1		
31	GND	Module Ground.		1		
32	Rx2+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
33	Rx2-	Receiver Data Inverted.	CML-O	3	Output to Host	
34	GND	Module Ground.		1		
35	Rx4+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
36	Rx4-	Receiver Data Inverted.	CML-O	3	Output to Host	
37	GND	Module Ground.		1		
38	Rx6+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
39	Rx6-	Receiver Data Inverted.	CML-O	3	Output to Host	
40	GND	Module Ground.		1		

41	Rx8+	Receiver Data Non-Inverted.	CML-O	3	Output to Host	
42	Rx8-	Receiver Data Inverted.	CML-O	3	Output to Host	
43	GND	Module Ground.		1		
44	INT/RSTn	Module Interrupt/Module Reset.	Multi-Level	3	Bi-Directional	2
45	Vcc	+3.3V Power.		2	Power from Host	
46	Vcc	+3.3V Power.		2	Power from Host	
47	SDA	2-Wire Serial Interface Data.	LVCMOS-I/O	3	Bi-Directional	1
48	GND	Module Ground.		1		
49	Tx7-	Transmitter Data Inverted.	CML-I	3	Input from Host	
50	Tx7+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
51	GND	Module Ground.		1		
52	Tx5-	Transmitter Data Inverted.	CML-I	3	Input from Host	
53	Tx5+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
54	GND	Module Ground.		1		
55	Tx3-	Transmitter Data Inverted.	CML-I	3	Input from Host	
56	Tx3+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
57	GND	Module Ground.		1		
58	Tx1-	Transmitter Data Inverted.	CML-I	3	Input from Host	
59	Tx1+	Transmitter Data Non-Inverted.	CML-I	3	Input from Host	
60	GND	Module Ground.		1		

Notes:

1. Open-drain with pull-up resistor on the host.
2. See pin assignments below for the required circuit.

Electrical Pin-Out Details - OSFP



Pin Descriptions for QSFP-DD

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1B	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3B	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3B	
4		GND	Module Ground.	1B	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3B	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3B	
7		GND	Module Ground.	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Receiver Power Supply.	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3B	
13		GND	Module Ground.	1B	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3B	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3B	
16		GND	Module Ground.	1B	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3B	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3B	
19		GND	Module Ground.	1B	1
20		GND	Module Ground.	1B	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3B	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3B	
23		GND	Module Ground.	1B	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3B	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3B	
26		GND	Module Ground.	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL/RxLOS	Interrupt/Optional RxLOS.	3B	
29		VccTx	+3.3V Transmitter Power Supply.	2B	2
30		Vcc1	+3.3V Power Supply.	2B	2
31	LVTTL-I	LPMode/Tx_Dis	Low-Power Mode/Optional Tx_Disable.	3B	
32		GND	Module Ground.	1B	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3B	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3B	
35		GND	Module Ground.	1B	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3B	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3B	
38		GND	Module Ground.	1B	1
39		GND	Module Ground.	1A	1
40	CML-I	Tx6-	Transmitter Inverted Data Input.	3A	

41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	3A	
42		GND	Module Ground.	1A	1
43	CML-I	Tx8-	Transmitter Inverted Data Input.	3A	
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	3A	
45		GND	Module Ground.	1A	1
46	LVCMOS/CML-I	P/VS4	Programmable/Vendor-Specific 4.	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Vendor-Specific 1.	3A	5
48		VccRx1	+3.3V Receiver Power Supply.	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Vendor-Specific 2.	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Vendor-Specific 3.	3A	5
51		GND	Module Ground.	1A	1
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	3A	
53	CML-O	Rx7-	Receiver Inverted Data Output.	3A	
54		GND	Module Ground.	1A	1
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	3A	
56	CML-O	Rx5-	Receiver Inverted Data Output.	3A	
57		GND	Module Ground.	1A	1
58		GND	Module Ground.	1A	1
59	CML-O	Rx6-	Receiver Inverted Data Output.	3A	
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	3A	
61		GND	Module Ground.	1A	1
62	CML-O	Rx8-	Receiver Inverted Data Output.	3A	
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	3A	
64		GND	Module Ground.	1A	1
65		NC	Not Connected.	3A	3
66		Reserved	For Future Use.	3A	3
67		VccTx1	+3.3V Power Supply.	2A	2
68		Vcc2	+3.3V Power Supply.	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input.	3A	6
70		GND	Module Ground.	1A	1
71	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	3A	
72	CML-I	Tx7-	Transmitter Inverted Data Input.	3A	
73		GND	Module Ground.	1A	1
74	CML-I	Tx5+	Transmitter Non-Inverted Data Input.	3A	
75	CML-I	Tx5-	Transmitter Inverted Data Input.	3A	
76		GND	Module Ground.	1A	1

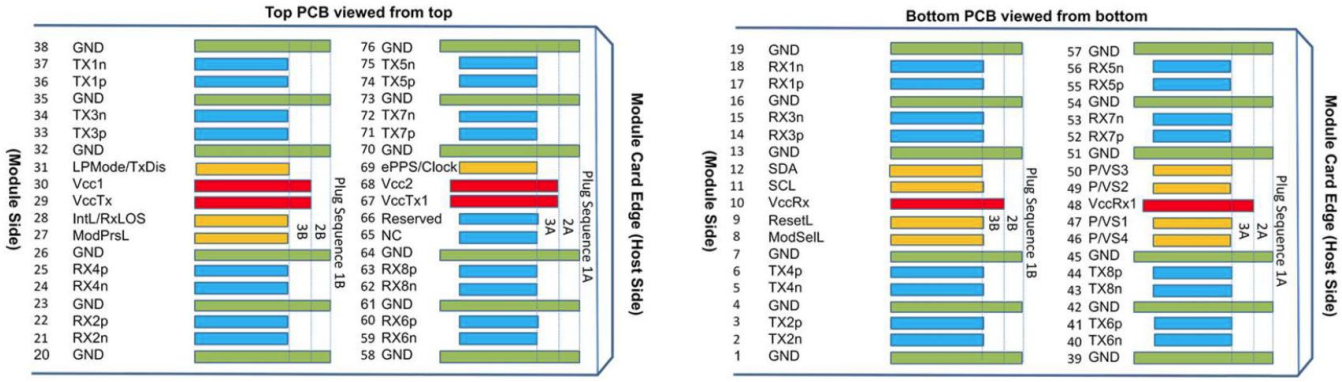
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits.

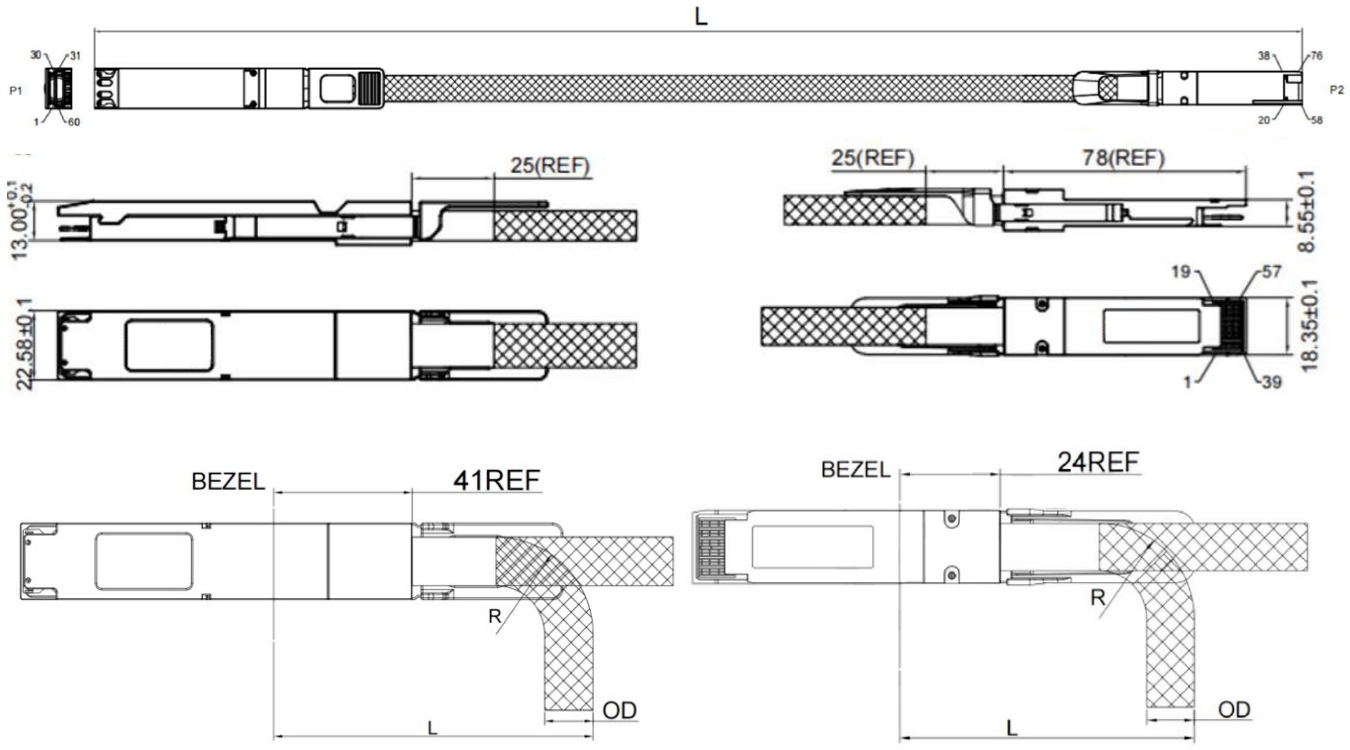
Each connector Vcc contact is rated for a maximum current of 1500mA.

3. Reserved and Not Connected pads recommended to be terminated with 10kΩ to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.
5. Full definitions of the P/VSx signals are currently under development. On new designs not used, P/VSx signals are recommended to be terminated on the host with 10kΩ.
6. ePPS/Clock, if not used, is recommended to be terminated with 50Ω to ground on the host.

Electrical Pin-Out Details – QSFP-DD



Mechanical Specifications



OSFP				QSFP-DD			
Gauge	**OD**	**Bend Radius "R"**	**Min. Bend Radius "L"**	**Gauge**	**OD**	**Bend Radius "R"**	**Min. Bend Radius "L"**
27AWG	10.7MM	22MM	75MM	27AWG	10.7MM	22MM	66MM

About ProLabs

Our extensive experience comes as standard. For over 20 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with more than 100 optical switching and transport platforms.

A Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 1.6T while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

The Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure compatible products, and immediate answers to your questions. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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