QSFP28-100G-DCO-A5-I-AR-AO

Arista Networks® Compatible (with select systems) TAA 100GBase-ZR QSFP28 Transceiver (SMF, 1528.77nm to 1567.13nm, 80km, LC, DOM, -40 to 85C) AutoTune

Features

- Hot-Pluggable QSFP28 Form Factor
- Transmission reach up to 80km unamplified (loss limited) or up to 120km amplified (dispersion limited, optionally extendable to 300km)
- IEEE 100G Ethernet (CAUI-4) Compliant Host Interface
- Operating Temperature: -40 to 85 Celsius
- Power Dissipation: 6W
- Full C-Band AutoTune, 50GHz/100GHz Spacing
- Please contact your sales representative for specific system information
- RoHS Compliant and Lead-Free
- Please contact your sales representative for specific system information

Applications

- Duplex Mux
- 100GBase Ethernet

Product Description

This Arista Networks® compatible (with select systems) QSFP28 transceiver provides 100GBase-ZR throughput up to 80km over single-mode fiber (SMF) using a wavelength of 1528.77nm to 1567.13nm via an LC connector. It can operate at temperatures between -40 and 85C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Arista Networks®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Absolute Maximum Ratings

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
DC Supply Voltage		Vcc	-0.3		3.6	V	
Low-Speed I/O Voltages			-0.3		3.6	V	
Storage Temperature		Tstg	-40		85	°C	
Operating Case Temperature	**Long-Term**	Tc	-20		85	°C	1
	Start-Up		-40		85	°C	
Operating Relative Humidity		RH	5		85	%	
Rx Input Power		PRx,in			10	dBm	
ESD Damage Threshold Human Body Model (HBM)	**DC Pins**		2000			V	
	RF Pins		1000			V	

Notes:

1. Central office applications.
2. Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the datasheet. Exposure to Absolute Maximum Ratings for extended periods of time can adversely affect device reliability. Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Host Interface Modes

Host Interface ID [18]	Host Interface Description [18]	Modulation	Forward Error Correction Code	Nominal Symbol Rate (GBd)	Supported Line Interface IDs [18]
65 [8]	CAUI-4 C2M without FEC	NRZ	None	25.78125	68, 192, 193
66 [8]	CAUI-4 C2M with RS(528,514) FEC	NRZ	RS(528,514)	25.78125	68, 192, 193

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply – General						
Power Supply Voltages		3.135	3.3	3.465	V	Including ripple, droop, and noise below 100kHz
Host RMS Noise Output				25	mV	10Hz - 10MHz
Module RMS Noise Output				15	mV	10Hz - 10MHz
Module Supply Noise Tolerance	PSNRmod			66	mV	10Hz - 10MHz, peak-to-peak
Module Inrush	Tip			50	µs	Instantaneous peak duration
	Tinit			500	ms	Initialization time
Power Supply – Low-Power Mode						
Power Dissipation	Plp			1.5	W	
Power Supply Current	Icc,ip,lp			600	mA	Instantaneous peak current
	Icc,sp,lp			495	mA	Sustained peak current
	Icc,lp			478	mA	1, Steady state current
Power Supply – High-Power Mode						
Power Dissipation	Php			6.0	W	
Power Supply Current	Icc,ip,hp			2400	mA	Instantaneous peak current
	Icc,sp,hp			1980	mA	Sustained peak current
	Icc,hp			1914	mA	1, Steady state current
Low-Speed I/O						
Clock Frequency (SCL)	f_{SCL}		400		kHz	Default
			1000			Fast-mode+
Output Voltage (SCL and SDA)	V_{OL}	0.0		0.4		Output low
	V_{OH}	Vcc-0.5		Vcc+0.3		Output high
Input Voltage (SCL and SDA)	V_{IL}	-0.3		0.3×Vcc	V	Input low
	V_{IH}	0.7×Vcc		Vcc+0.5		Input high
Capacitance for SCL and SDA I/O Signal	Ci			14	pF	
Total Bus Capacitive Load for SCL and SDA **400kHz Clock Rate**	Cb			100	pF	2, 3.0kΩ pull-up resistor, maximum
				200		2, 1.6kΩ pull-up resistor, maximum
Input Voltage/Current, LPMode/TxDis, ResetL, and ModSelL	V_{IL}	-0.3		0.8	V	Input voltage, low
	V_{IH}	2.0		Vcc+0.3		Input voltage, high
	I_{in}	-365		125	µA	Input current, 0V < VIN < Vcc
Output Voltage, ModPrsL, and IntL/RxLOSL	V_{OL}	0.0		0.4	V	Output low, I_{OL} = 2mA
	V_{OH}	Vcc-0.5		Vcc+0.3		Output high, 10kΩ pull-up resistor to Host_Vcc

Notes:

1. The module will stay within its advertised power class for all supply voltages.
2. For 1000kHz clock rate.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply – General						
Symbol Rate	Rbaud		27.95		GBd	
Modulation Format			DP-DQPSK			
Channel Frequency Range	Vc	191.4	193.7	196.1	THz	100GHz grid
	Vc	191.35	193.7	196.1	THz	50GHz grid
Channel Spacing	ΔVc		100		GHz	100GHz grid
	ΔVc		50		GHz	50GHz grid
Frequency Accuracy	δVc	-1.8		1.8	GHz	
Laser Intrinsic Linewidth	LW			500	kHz	Calculated based on FM noise Power Spectral Density (PSD) measurement
Side-Mode Suppression Ratio	SMSR	40			dB	No modulation
Relative Intensity Noise	RIN			-140	dB/Hz	Peak over 0.2GHz < f < 10GHz
Transmitter						
Tx Output Power	PTx,out	-8		-4	dBm	
Tx Output Power Monitor Range	PTx,mon	-10		-2	dBm	
Tx Output Power Monitor Accuracy	δPTx,mon	-1.5		1.5	dB	Tx optical power monitor reading relative to actual Tx output power
Tx Output Power During Tuning or When Tx is Disabled	PTx,dark			-35	dBm	
Tx Spectral Excursion		-15		15	GHz	ITU-T G.698.2 §7.2.3 [11]
Tx Output Power Imbalance Between X and Y Polarizations	ΔPX/Y			1.5	dB	
Tx XY Skew				6.0	ps	
Tx IQ Offset				-25	dB	
Tx IQ Imbalance				1.0	dB	
Tx Quadrature Error		-7.0		7.0	°	
Tx IQ Skew				1.5	ps	
Tx Error Vector Magnitude Mask Ratio				23	%	ITU-T G.698.2 §7.2.12 [11], with 24dB/0.1nm noise loading
Tx In-Band Optical Signal to Noise Ratio	OSNRin	40			dB/0.1nm	Under modulation, |Δf|<60GHz
Tx Out-of-Band Optical Signal to Noise Ratio	OSNRout	35			dB/0.1nm	Under modulation, |Δf|>60GHz, excl. side-mode peaks
Tx Reflectance				-20	dB	
Receiver						
Rx Total Input Power	$P_{Rx,tot}$	-30		3	dBm	Broadband
Rx Signal Input Power (Amplified)	$P_{Rx,sig}$	-18		1	dBm	Full Rx OSNR tolerance
		-22		3	dBm	1

Rx OSNR Tolerance	**100G DQPSK SC**		16.5			dB/0.1nm	Back-to-back, $P_{Rx,sig}$ > -18dBm
	100G DQPSK RS		21.5				
CD Tolerance					2.4	ns/nm	OSNR penalty < 0.5dB
PMD Tolerance					10	Ps	
DGD Tolerance					20	Ps	
Tolerance to Change in SOP					50	krad/s	
PDL OSNR Penalty	**1dB PDL**				0.5	dB/0.1nm	Change in principal state of polarization < 1rad/ms
	2dB PDL				1.0		
	4dB PDL				3.0		
Rx Signal Input Power Transient Amplitude			-3		3	dB	2
Rx Signal Input Power Transient Rise/Fall Time			100			µs	3
Rx Signal Input Power (Unamplified)	**100G DQPSK SC**		-30		1	dBm	OSNR > 35dB/0.1nm
	100G DQPSK RS		-24		1		
Rx Signal Input Power Monitor Range		$P_{Rx,mon(s)}$	-21		3	dBm	
Rx Signal Input Power Monitor Accuracy		$\delta P_{Rx,mon(s)}$	-2.5		2.5	dB	
Rx Total Input Power Monitor Range		$P_{Rx,mon(t)}$	-21		6	dBm	
Rx Total Input Power Monitor Accuracy		$\delta P_{Rx,mon(t)}$	-2.0		2.0	dB	
Rx Reflectance					-20	dB	

Notes:

1. Extended range. Rx signal input power range over which performance can be guaranteed with <1dB OSNR penalty relative to the Rx OSNR tolerance limit.
2. Peak excursion from steady state, transient within Rx signal input power (amplified) range, and OSNR penalty <0.5dB.
3. Rise/fall time for the above peak excursion, OSNR penalty <0.5dB.

SFF-8636 Management Interface

Parameter	Symbol	Min.	Max.	Unit	Conditions	Notes
Initialization Time			120	s	Time from power on or hot plug until the module is fully functional (assuming LPMode pulled low by the host).	2, 3
Reset Init Assert Time		10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.	
Serial Bus Hardware Ready Time			2	s	Time from power on until the module responds to data transmission over the 2-wire serial bus.	2
Monitor Data Ready Time			2	s	Time from power on to Data_Not_Ready, Byte 2 bit 0, cleared to 0, and IntL output pulled low.	2
Reset Assert Time			120	s	Time from a rising edge on the ResetL input until the module is fully functional.	3
LPMode/TxDis Mode Change Time			100	ms	Time to change between LPMode and TxDis modes of the dual-mode signal LPMode/TxDis.	
LPMode Assert Time			100	ms	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1.	
LPMode De-Assert Time			120	s	Time from when the host pulls LPMode low until the module is fully functional.	3
IntL/RxLOSL Mode Change Time			100	ms	Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL.	
IntL Assert Time			200	ms	Time from occurrence of condition triggering an interrupt until IntL is low.	
IntL De-Assert Time			500	µs	Time from clear on read operation of associated flag until module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault, and other flag bits.	4
RxLOSL Assert Time			1	ms	Time from optical loss of signal to RxLOSL signal pulled low by the module.	
RxLOSL De-Assert Time			3	ms	Time from optical signal above the LOS de-assert threshold to when the module releases the RxLOSL signal to high.	
Tx Fault Assert Time			200	ms	Time from Tx Fault state to Tx Fault bit set to 1 and IntL pulled low by the module.	
Flag Assert Time			200	ms	Time from condition triggering flag to associated flag bit set to 1 and IntL pulled low by the module.	
Mask Assert Time			100	ms	Time from mask bit set to 1 until the module is prevented from pulling IntL low when the associated flag is set high.	1
Mask De-Assert Time			100	ms	Time from mask bit cleared to 0 until module is enabled to pull IntL low when the associated flag is set high.	1
I/O Timing for Squelch & Disable						
Rx Squelch Assert Time			15	ms	Time from loss of Rx input signal until the squelched output condition is reached.	
Rx Squelch De-Assert Time			15	ms	Time from resumption of Rx input signals until normal Rx output condition is reached.	
Tx Squelch Assert Time			400	ms	Time from loss of Tx input signal until the squelched output condition is reached.	
Tx Squelch De-Assert Time			10	s	Time from resumption of Tx input signal until the normal Tx output condition is reached.	
Tx Disable Assert Time			1	ms	Time from Tx_Disable bit is set to 1 until optical output falls below 10% of nominal.	1
Tx Disable De-Assert Time			10	s	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.	1

Rx Output Disable Assert Time			100	ms	Time from Rx Output Disable bit set (value= 1b) until Rx output falls below 10% of nominal.	1
Rx Output Disable De-Assert Time			100	ms	Time from Rx Output Disable bit cleared (value= 0b) until Rx output rises above 90% of nominal.	1
Squelch Disable Assert Time			100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 1b) until squelch functionality is disabled.	1
Squelch Disable De-Assert Time			100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b) until squelch functionality is enabled.	1

Notes:

1. Measured from the rising edge of SDA during STOP sequence of write transaction.
2. "Power On" is defined as the instant when supply voltages reach and remain at or above the minimum level specified.
3. "Fully Functional" is defined as the module being ready to transmit and receive valid signals and all management interface data, including monitors, being valid. It is indicated after "Reset" or "Hot Plug" by the module releasing IntL to "high" after the host has read a 0 from the Data_Not_Ready flag bit. Rx LOS condition is defined as (a) Rx input power below threshold or (b) DSP loss of signal.
4. Measured from rising edge of the SDA during STOP sequence of read transaction.

Optical Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions	Notes
Tx Turn On Time			10	s	Warm Start	1
			120	s	Cold Start	
Rx Acquisition Time			30	ms	Warm Start	
			120	s	Cold Start	
Tx/Rx Channel Tuning Time			30	s		

Notes:

1. Assumes the Tx/Rx laser is already tuned to the correct frequency.

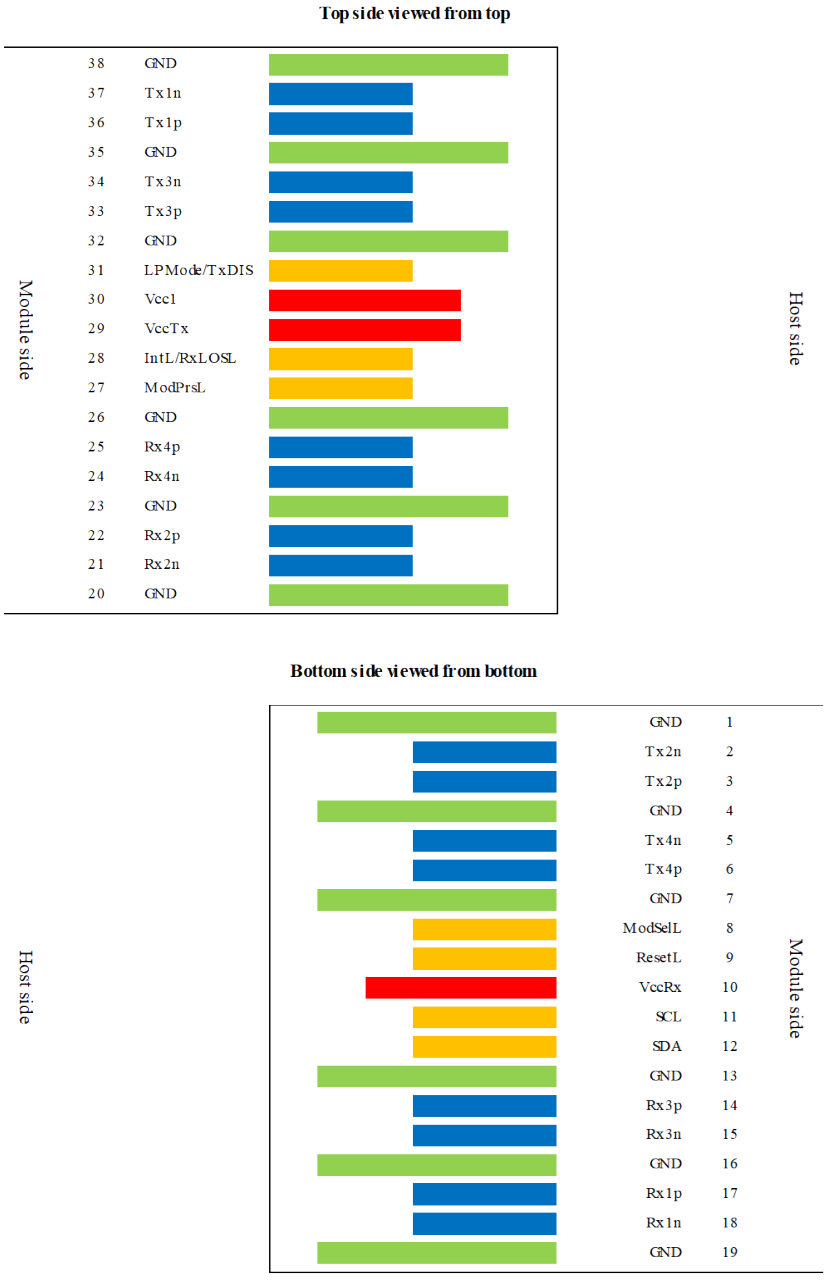
Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Receiver Power Supply.	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3-	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1-	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	3	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	3	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1
27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		VccTx	+3.3V Transmitter Power Supply.	2	2
30		Vcc1	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMode/TxDis	Low-Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Module Ground.	1	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3	
35		GND	Module Ground.	1	1
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

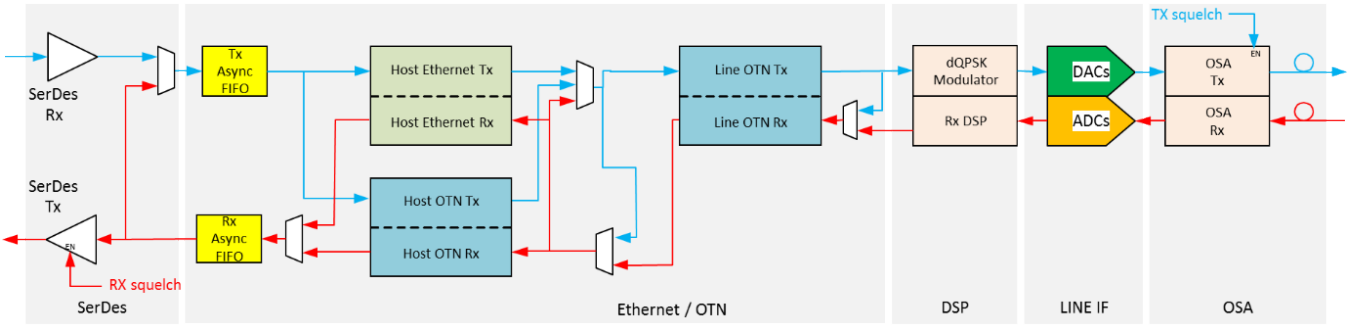
Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are applied concurrently and may be internally connected within the module in any combination.
3. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, and 3. See figure below for pad locations.

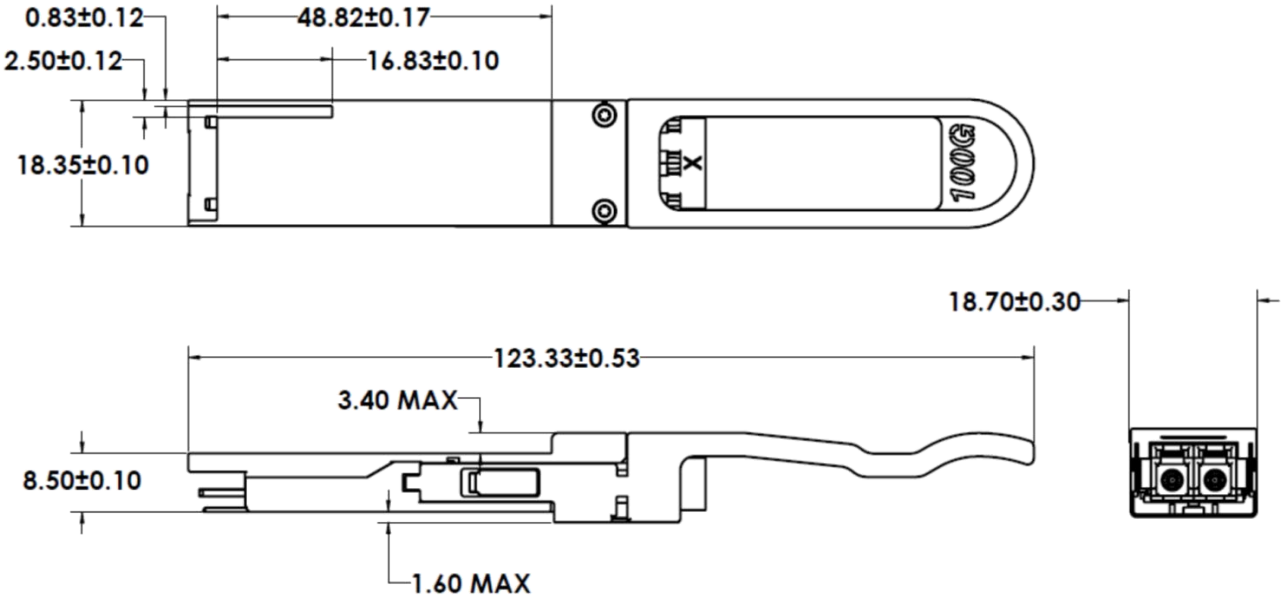
Electrical Pad Layout



Block Diagram



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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