QDD-8X25-MR-SR-E-AO

Arista Networks® QDD-8X25-MR-SR-E Compatible TAA 200GBase-SR8 QSFP-DD Transceiver (MMF, 850nm, 100m, MPO-16, CMIS 4.0)

Features

- QSFP-DD MSA Compliant
- Optical and Electrical Interface: 8x25G NRZ
- CMIS 4.0
- Up to 100m Over OM4 MMF
- Single 3.3V Power Supply
- Parallel 8 Optical Lanes
- MPO-16/APC Connector
- Power Consumption: 8W
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius

Applications

- 200GBase Ethernet
- Access and Enterprise

Product Description

This Arista Networks® QDD-8X25-MR-SR-E compatible QSFP-DD transceiver provides 200GBase-SR8 throughput up to 100m over multi-mode fiber (MMF) using a wavelength of 850nm via an MPO-16 connector. It is guaranteed to be 100% compatible with the equivalent Arista Networks® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products.")

TAA COMPLIANT

Rev. 042826

Absolute Maximum Ratings

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature		Tstg	-40		85	°C	
Operating Case Temperature		Tc	0		75	°C	
Supply Voltage		Vcc	-0.5		3.6	V	
Relative Humidity		RH	5		85	%	
Damage Threshold			5			dBm	
Link Distance	**OM3**	D1	0.5		70	m	
	OM4	D2	0.5		100	m	
Signaling Rate Per Lane			25.7815 ± 100ppm			Gbps	

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Consumption	PC			8	W	
Transmitter						
Differential Data Input Swing Per Lane	VIN,pp			900	mV	
DC Common-Mode Voltage		-350		2850	mV	1
Differential Termination Mismatch				10	%	
Differential Input Return Loss		Per Section 83E.3.3.1, IEEE 802.3bm				
Differential- to Common-Mode Input Return Loss		Per Section 83E.3.3.1, IEEE 802.3bm				
Module Stressed Input Test		Per Section 83E.3.4.1, IEEE 802.3bm				
Receiver						
Differential Data Output Swing	VOUT,pp			900	mV	
DC Common-Mode Voltage		-350		2850	mV	1
Common-Mode Noise (RMS)				17.5	mV	
Differential Termination Mismatch				10	%	
Eye Width		0.57			UI	
Differential Eye Height		228			mV	
Vertical Eye Closure				5.5	dB	
Transition Time (20-80%)		12			ps	
Differential Output Return Loss		Per Section 83E.3.1.3, IEEE 802.3bm				
Common- to Differential-Mode Conversion Return Loss		Per Section 83E.3.1.3, IEEE 802.3bm				

Notes:

1. DC common-mode voltage is generated by the host. Specification includes the effects of ground offset voltage.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λ	840		865	nm	
RMS Spectral Width				0.65	nm	
Average Launch Power Per Lane	PAVG	-7.5		4	dBm	
OMAouter Per Lane	POMA	-5.5		3	dBm	
Average Launch Power of Off Transmitter Per Lane	Poff			-30	dBm	
Extinction Ratio Per Lane	ER	2			dB	
Optical Return Loss Tolerance				12	dB	
Transmitter Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}			dB	1
Receiver						
Center Wavelength	λ	840		865	nm	
Damage Threshold		5			dBm	
Average Receiver Power Per Lane	PIN	-8.4		4	dBm	2
Receiver Power Per Lane (OMAouter)	ROMA			3	dBm	
Receiver Sensitivity (OMA) Per Lane	PSENS			-8	dBm	3
Receiver Reflectance	RR			-12	dB	
LOS Assert	LOSD	-30			dBm	
LOS De-Assert	LOSA			-13	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. Hit ratio 1.5×10^{-3} hits per sample.
2. Minimum value is informative only and not the principal indicator of signal strength.
3. Measured with a PRBS 2^{31}-1 test pattern with BER=1×10^{-12} @ 25.78Gbps.

Pin Descriptions

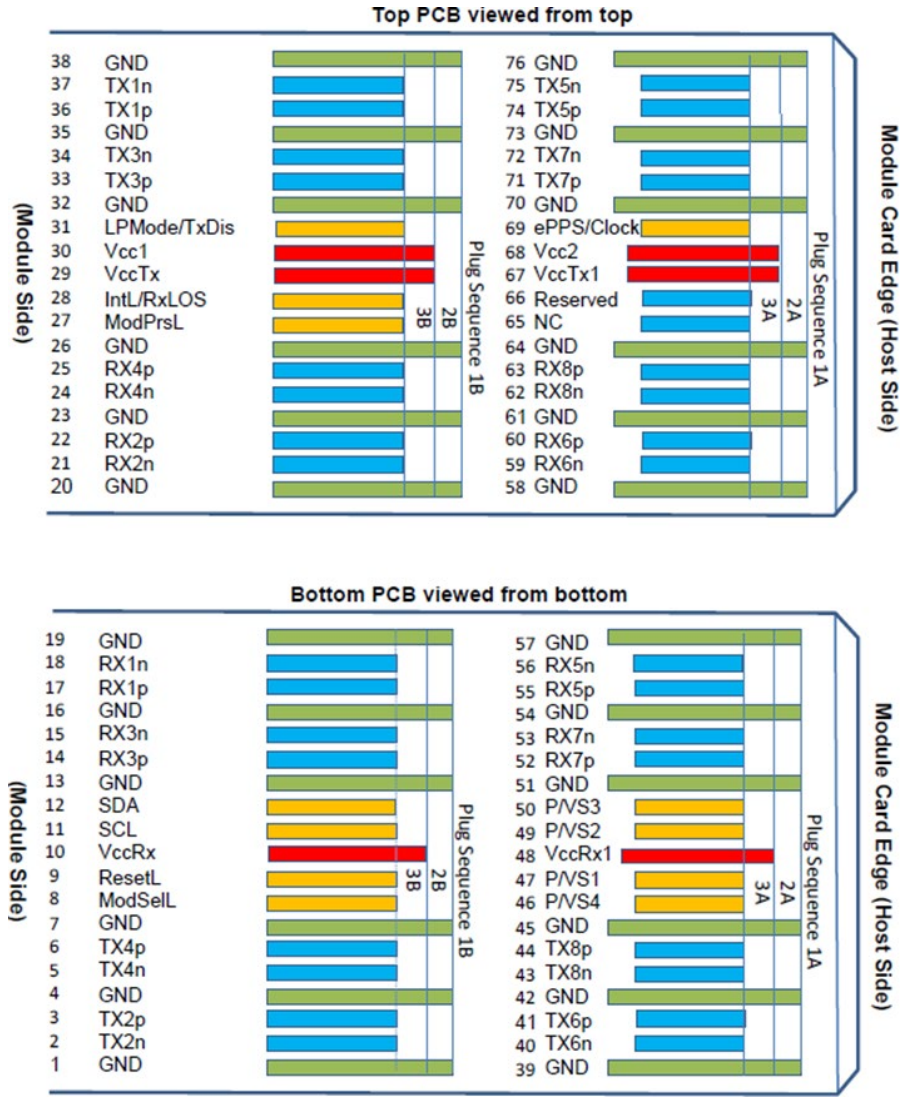
Pin	Symbol	Logic	Name/Description	Plug Sequence	Notes
1	GND		Module Ground.	1B	1
2	Tx2-	CML-I	Transmitter Inverted Data Input.	3B	
3	Tx2+	CML-I	Transmitter Non-Inverted Data Input.	3B	
4	GND		Module Ground.	1B	1
5	Tx4-	CML-I	Transmitter Inverted Data Input.	3B	
6	Tx4+	CML-I	Transmitter Non-Inverted Data Input.	3B	
7	GND		Module Ground.	1B	1
8	ModSelL	LVTTL-I	Module Select.	3B	
9	ResetL	LVTTL-I	Module Reset.	3B	
10	VccRx		+3.3V Receiver Power Supply.	2B	2
11	SCL	LVCMOS-I/O	2-Wire Serial Interface Clock.	3B	
12	SDA	LVCMOS-I/O	2-Wire Serial Interface Data.	3B	
13	GND		Module Ground.	1B	1
14	Rx3+	CML-O	Receiver Non-Inverted Data Output.	3B	
15	Rx3-	CML-O	Receiver Inverted Data Output.	3B	
16	GND		Module Ground.	1B	1
17	Rx1+	CML-O	Receiver Non-Inverted Data Output.	3B	
18	Rx1-	CML-O	Receiver Inverted Data Output.	3B	
19	GND		Module Ground.	1B	1
20	GND		Module Ground.	1B	1
21	Rx2-	CML-O	Receiver Inverted Data Output.	3B	
22	Rx2+	CML-O	Receiver Non-Inverted Data Output.	3B	
23	GND		Module Ground.	1B	1
24	Rx4-	CML-O	Receiver Inverted Data Output.	3B	
25	Rx4+	CML-O	Receiver Non-Inverted Data Output.	3B	
26	GND		Module Ground.	1B	1
27	ModPrsL	LVTTL-O	Module Present.	3B	
28	IntL	LVTTL-O	Interrupt.	3B	
29	VccTx		+3.3V Transmitter Power Supply.	2B	2
30	Vcc1		+3.3V Power Supply.	2B	2
31	InitMode	LVTTL-I	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	3B	
32	GND		Module Ground.	1B	1
33	Tx3+	CML-I	Transmitter Non-Inverted Data Input.	3B	
34	Tx3-	CML-I	Transmitter Inverted Data Input.	3B	
35	GND		Module Ground.	1B	1
36	Tx1+	CML-I	Transmitter Non-Inverted Data Input.	3B	
37	Tx1-	CML-I	Transmitter Inverted Data Input.	3B	
38	GND		Module Ground.	1B	1
39	GND		Module Ground.	1A	1
40	Tx6-	CML-I	Transmitter Inverted Data Input.	3A	
41	Tx6+	CML-I	Transmitter Non-Inverted Data Input.	3A	
42	GND		Module Ground.	1A	1

43	Tx8-	CML-I	Transmitter Inverted Data Input.	3A	
44	Tx8+	CML-I	Transmitter Non-Inverted Data Input.	3A	
45	GND		Module Ground.	1A	1
46	Reserved		For Future Use.	3A	3
47	VS1		Module Vendor-Specific 1.	3A	3
48	VccRx1		+3.3V Receiver Power Supply.	2A	2
49	VS2		Module Vendor-Specific 2.	3A	3
50	VS3		Module Vendor-Specific 3.	3A	3
51	GND		Module Ground.	1A	1
52	Rx7+	CML-O	Receiver Non-Inverted Data Output.	3A	
53	Rx7-	CML-O	Receiver Inverted Data Output.	3A	
54	GND		Module Ground.	1A	1
55	Rx1+	CML-O	Receiver Non-Inverted Data Output.	3A	
56	Rx1-	CML-O	Receiver Inverted Data Output.	3A	
57	GND		Module Ground.	1A	1
58	GND		Module Ground.	1A	1
59	Rx6-	CML-O	Receiver Inverted Data Output.	3A	
60	Rx6+	CML-O	Receiver Non-Inverted Data Output.	3A	
61	GND		Module Ground.	1A	1
62	Rx8-	CML-O	Receiver Inverted Data Output.	3A	
63	Rx8+	CML-O	Receiver Non-Inverted Data Output.	3A	
64	GND		Module Ground.	1A	1
65	NC		Not Connected.	3A	3
66	Reserved		For Future Use.	3A	3
67	VccTx1		+3.3V Transmitter Power Supply.	2A	2
68	Vcc2		+3.3V Power Supply.	2A	2
69	ePPS	LVTTL-I	Precision Time Protocol (PTP) Reference Clock Input (N/C Within Module).	3A	3
70	GND		Module Ground.	1A	1
71	Tx7+	CML-I	Transmitter Non-Inverted Data Input.	3A	
72	Tx7-	CML-I	Transmitter Inverted Data Input.	3A	
73	GND		Module Ground.	1A	1
74	Tx5+	CML-I	Transmitter Non-Inverted Data Input.	3A	
75	Tx5-	CML-I	Transmitter Inverted Data Input.	3A	
76	GND		Module Ground.	1A	1

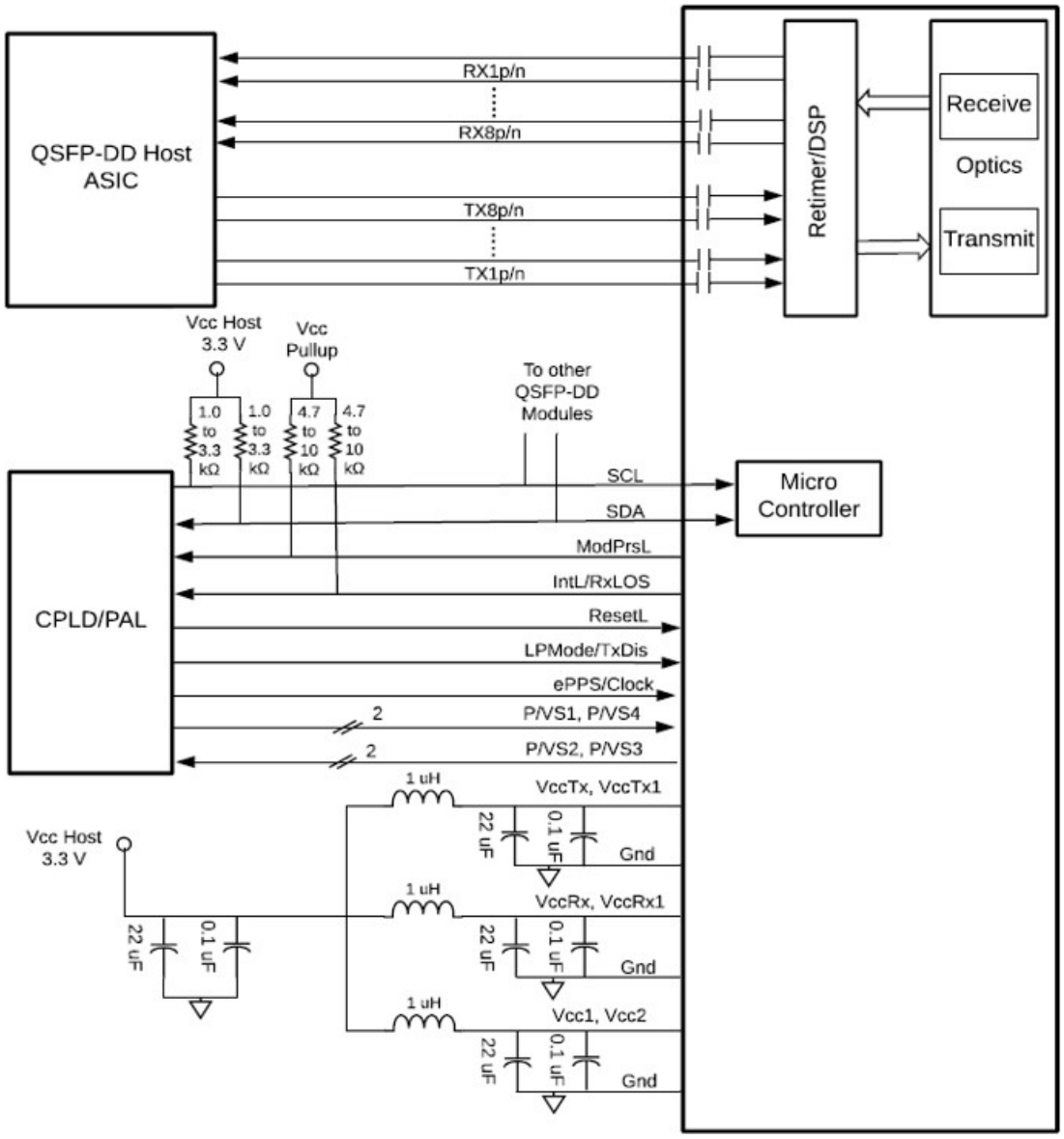
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor-Specific, Reserved, and Not Connected pins may be terminated with 50Ω to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to the GND that is greater than 10kΩ and less than 100pF.

Electrical Pad Layout

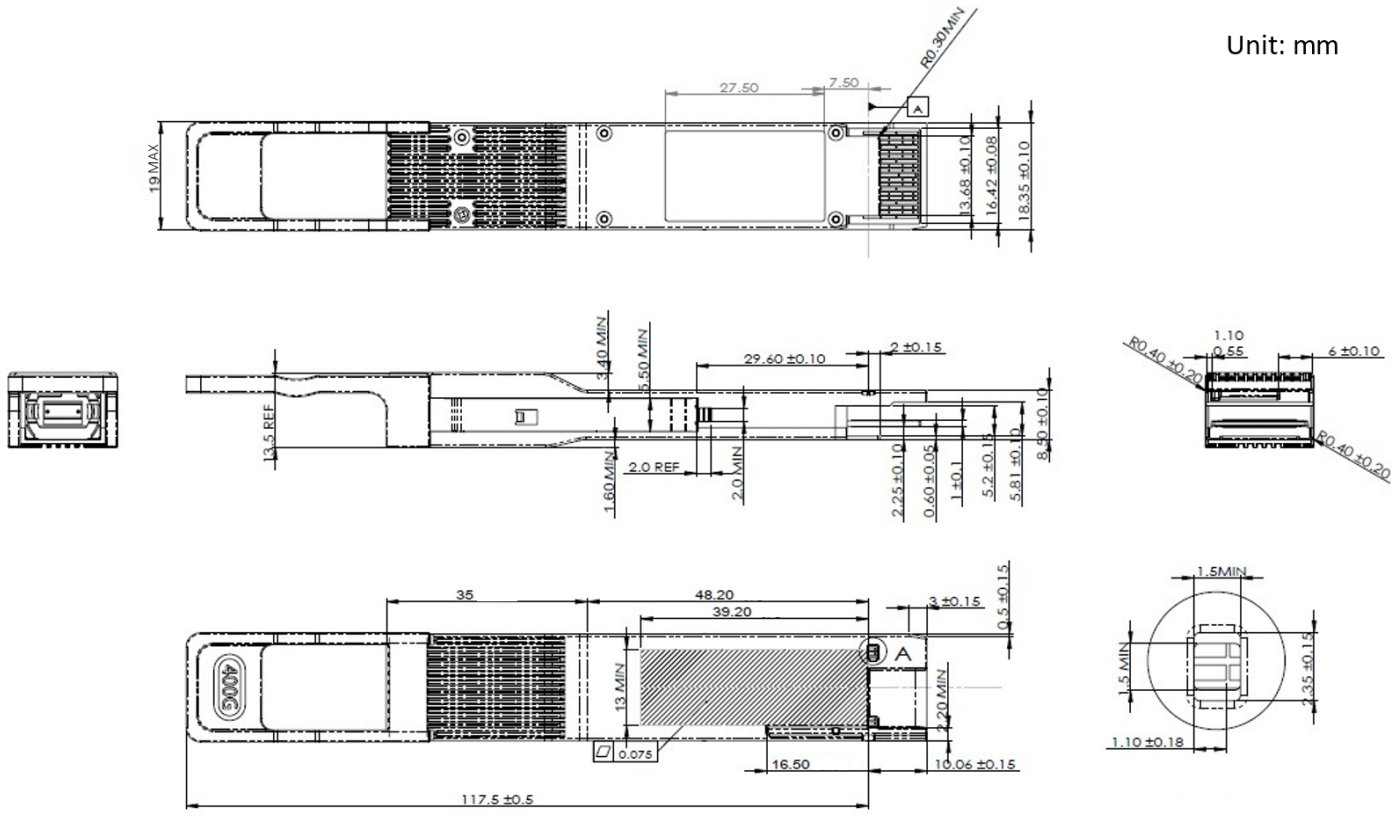


Recommended Interface Circuit

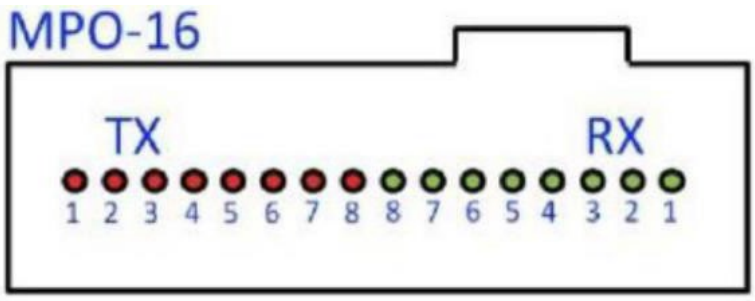


Mechanical Specifications

Unit: mm



Optical Interface Lanes and Assignment



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.

U.S. Headquarters

Email: sales@addonnetworks.com

Telephone: +1 877.292.1701

Fax: 949.266.9273

Europe Headquarters

Email: salesemea@addonnetworks.com

Telephone: +44 1285 842070